Design Considerations for a Slotted OTDM Ring-LAN

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Abstract. In this paper, two different node architectures for a high-speed packet-switched ring LAN based on the optical time-division multiplexing technique are proposed. Due to the incorporated low-speed packet headers the presented ring can be viewed as an optically (bit rate) transparent network. In both cases, the node can be implemented by using the current opto-electronic technology. Moreover, access protocols based on these proposed architectures are introduced employing the Slotted Ring scheme with destination release. Thereby, the specific processing delay requirements of the nodes are taken into account. Additionally, simulation results are shown for both configurations evaluating throughput and access delays as main performance measures. The paper reveals whether the deployment of additional (and expectably costly) OTDM multiplexers/demultiplexers at each ring node is really justified considering the system performance.

1. Introduction

New bandwidth-intensive applications such as supercomputer interconnections, interactive TV and multimedia banks will place severe demands on the network bandwidth available from a single-mode optical fiber in local and metropolitan area networks. Therefore, future photonic LANs are supposed to provide transmission speeds in the upper Gbit/s range on instantaneous demand with high medium efficiency and minimal delay. A very promising technique in this field is Optical Time Division Multiplexing (OTDM) which yields aggregate transmission rates beyond the reach of high-speed electronics. Used within LANs, the OTDM technique guarantees flexible and fast access to the medium.

However, at present, it is not possible in a medium access node located at the end-user to keep an optical signal completely in optical form. It has to be converted into the electrical domain, processed, saved and interpreted by electronics. For point-to-point connections between end-users within high-speed optical LANs, the payload must be converted to lower data rates for processing at the nodes. Therefore, by employing the optical packet switching technique implying that optical packets of constant duration consist of variable bit rate payloads and headers with fixed data rates, an optical transparent LAN may be developed [3].

In this paper, we present two different node architectures for such a high-speed packet-switched ring-LAN employing optical packet compression and decompression (bit-rate conversion) and also using OTDM multiplexer/demultiplexer units. Additionally, in a first step, we introduce static Medium Access Control (MAC) protocols based on these architectures. These fixed-assignment access protocols are based on the Slotted Ring scheme with destination release using several virtual channels and are appropriately taking the processing overhead of the considered node configurations into account.

2. Network Architecture

The proposed ultra high-speed OTDM ring-LAN is based on the slotted single-ring architecture. For saving costs, a single ring is considered in this paper, in contrast to the previous works [3,4], where counter-rotating double rings were analyzed.

In Fig. 1, the considered network architecture is demonstrated. The ring network operates at a medium rate of up to 100 Gbit/s and all attached nodes are supposed to be capable of attaining this data rate for payload transmission (differing from [4], where a heterogeneous network has been considered) by means of approaches given in section 3 below.
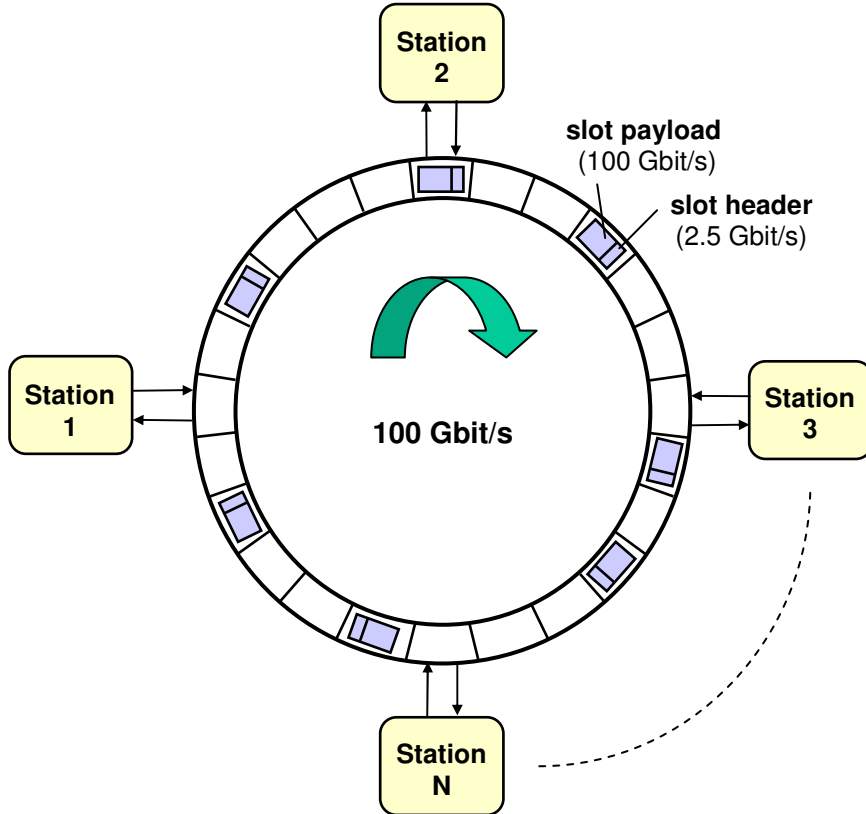

Figure 1: Network architecture of the proposed high-speed ring LAN

Fixed-period slots with duration T_s separated by guard bands circulate permanently on the ring and may carry data packets. Each slot consists of a *header* and a *payload* section, as depicted in Fig. 2. The slot header consists of an empty/full flag, destination address, source address, and additional protocol control flags. It may also contain information about the format, bit-rate, and type of the payload. The payload itself is bit-rate variable and may be transmitted at any data-rate up to 100 Gbit/s.

Transmission rate transparency is achieved by implementing a fixed lower bit-rate packet header. In this specific case, it is assumed to be 2.5 Gbit/s, which makes it possible to realize fully electronical header processing without need for data rate conversion. This feature makes a node cheaper and easier to realize. Moreover, the nodes without data rate conversion facilities can also read the packet header. Consequently, the packets can pass through the network transparently and can be routed not only by all-optical switches in a packet-switched all-optical network but also by electronic switches with optical interfaces [5].
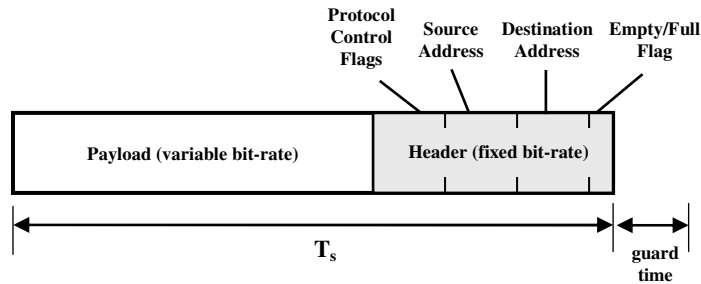
Figure 2: Slot format for the proposed high-speed ring LAN

In this paper, two design strategies for a high-speed (100 Gbit/s) node deploying optical packet payload compression and decompression for a high-speed packet-switched ring-LAN based on the OTDM technique are compared. In addition, we design and analyze a MAC (medium access control) protocol for the proposed ring network, in which the specific processing delay requirements given by the node architectures are considered.

3. Node Design

A slotted system with empty/full slot markers allows a design of a very simple high performance MAC protocol. It permits concurrent access to the media by multiple, geographically separated nodes. This principle advantage of slotted systems can be achieved only by medium access at the full media rate, but current limitations by electronics make a processing of a 100 Gbit/s bit-stream infeasible.

However, the existence of optical buffers and optical rate conversion systems enable the access nodes to receive a packet of a data stream at the media rate and convert it down to the acceptable rate for electronically processing and interpreting. As a consequence, the down conversion delay must also be taken into account. Two possible node architectures for a slotted high-speed ring LAN with 100 Gbit/s medium access are shown in Fig. 3.

In Fig. 3(a), nodes providing only one service type at a data rate of 2.5 Gbit/s and require optical packet compression (and decompression) in order to achieve a target transmission speed of 100 Gbit/s (and convert back to 2.5 Gbit/s) for an one-channel signal is presented. Indeed, it is possible to generate and process a 2.5 Gbit/s bit-stream electronically. There are customary components available for that (e.g., a synchronous FIFO memory with an access time less than 8 ns [6]). For serial/parallel and parallel/serial conversion, a 2.5 Gbit/s 20 bit transceiver [7] can be used.

Several methods of optical rate conversion (compression and decompression) have been proposed to date [8,9,11]. Most of these schemes are based on an optical buffer (optical storage loop) and a sampling technique. However, there are some restrictions concerning bit-rate and packet size. In [10], the storage of 9-kbit packets at 80 Gbit/s for over 30 seconds is reported along with the prediction that by using optical modulation, the operating rates of these fiber loop memories may be extended to 100 Gbit/s.

The optical packet compression scheme in [11] is based on the idea of rational harmonic mode-locking. The relation between the fundamental frequency of the storage ring f_0, the sampling clock frequency f_1, and the target high bit-rate f_2 is as follows:

$$f_2 = m \cdot f_1 = (m \cdot h - 1) f_0 ,$$

where m represents the required number of round-trips in the loop to obtain the desired bit rate and h denotes the number of bits entering the storage loop in each round-trip yielding the packet size $mh - 1$. In our case, we assume $h \leq 213$ and $m = 40$, so that the maximal slot size can be set to $l_{s,max} = (mh - 1) = (213 \cdot 40 - 1) = 8519$ bits (corresponding to 20 ATM cells encapsulated in one slot plus 39 bits reserved for additional control information exchange or a error-control method, e.g. CRC32).
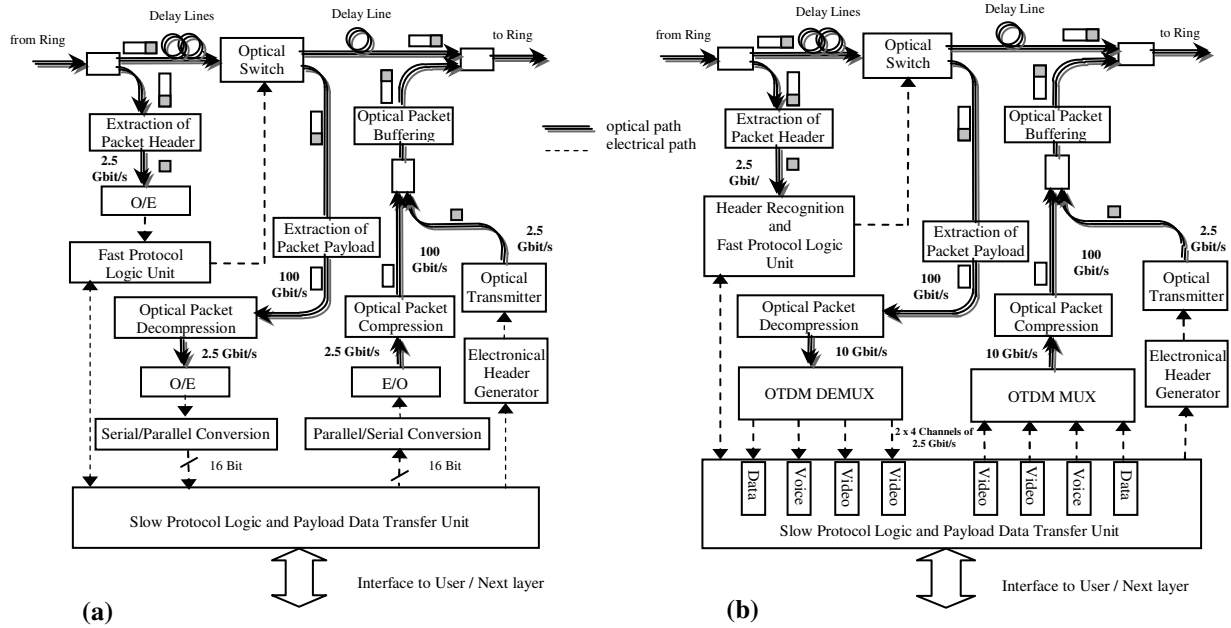

Figure 3: Two possible node architectures for a high-speed ring LAN with 100 Gbit/s medium access by use of the optical packet compression and decompression method

The functionality of the high-speed MAC node can be described as follows: the arriving slot is split into the *optical delay line path* and the *header processing path*. After the header has been recognized and extracted, the Fast Protocol Logic Unit processes it on the fly. The header processing, or its pipeline stage, must be fast enough so that it is able to finish header processing before the next header arrives. With a customary electronic technology it could be feasible to extract and process the main header information within the duration of 50 ns.

By the use of a LiNbO$_3$ or a Y-SOA switch (with a switching speed of the order 1 ns) we can design delay lines resulting in a header processing latency T_{hp} between 50 and 60 ns, corresponding to a packet length of 5kbit – 6kbit at 100 Gbit/s. Alternatively, by deploying a silica-based thermo-optic switch the delay lines must be larger than 1 ms.

If the destination address in the slot header matches the address of the node, the payload is extracted and converted down to 2.5 Gbit/s. If it is not the case, the packet simply propagates through the node. The Optical Packet Decompression Unit converts 100 Gbit/s (HDR-High Data Rate) packets to the lower bit rate 2.5 Gbit/s (LDR-Low Data Rate) for electronically saving and processing. Consequently, a new packet cannot be received until the previous packet has been completely converted. Due to this restriction, every 40th (100/2.5) slot of the slotted ring may be received. Note that the data rate conversion time is given by: $T_{cv} = l_s/\text{LDR} = l_s/2.5$.

Inserting a new packet into the ring-LAN can be realized by synchronically unloading the optical packet buffer if an empty slot arrives. The optical packet must be prepared (payload compressed and attached to its own header) and loaded into the optical packet buffer. Since

optical buffers (optical storage loops) can store a full packet size for more than hundreds of microseconds, the insertion time T_{in} could be simply determined by the header processing time and the synchronization constraints, i.e., $T_{hp} - l_s \leq T_{in} \leq T_{hp} + l_s$.

Alternatively, in Fig. 3(b), the nodes' traffic is composed of four distinct service classes (channels), which have to be time-division multiplexed in a *bit-interleaved* manner (besides the packet interleaving on the ring). Due to the shorter data conversion time, $T_{cv} = l_s/\text{LDR} = l_s/10$ in this case, the time constraints for the corresponding access protocols can be relaxed. Consequently, each 10th slot is accessible for reception here.

4. Access Control Design

The medium access of the considered ring network is based on the Slotted Ring protocol employing *destination release* and *spatial slot reuse*. By allowing destination release and reuse of slots, the network throughput significantly exceeds the line rate of the medium. In contrast to alternative multiplexing methods such as WDM or bit-interleaved OTDM, the slotted OTDM scheme enables sharing a fast medium by access nodes capable of operating at maximally 100 Gbit/s rates.

However, due to the strict time constraints associated with the presented node architectures, the basic Slotted Ring scheme is not applicable any more. The limitations in terms of the packet reception given in section 3 lead to a static (fixed-assignment) Slotted Ring based access protocol, where each node is assigned a certain slot (or slots) for the reception of packets. In the case of node architecture (a), i.e. without OTDM facilities, a node can use every 40th slot for reception, whereas concerning the node configuration (b) deploying OTDM multiplexer/demultiplexer every 10th slot is available for reception.

Therefore, in our proposed access control scheme, the slots are successively numbered in the ring initialization phase and assigned to the individual nodes in an interleaved manner. That means, that for instance slots having the numbers 1, $k + 1$, $2k + 1$, ... are uniquely dedicated to node 1, slots with the numbers 2, $k + 2$, $2k + 2$, ... to node 2 and so forth, given that every kth slot can be emptied. As a result, we may speak of k virtual channels on the ring.

Consequently, a source node willing to send a packet to a specific destination node waits for the appropriate slot to arrive in order to ensure that the corresponding packet can safely be received by the destination node. In order to increase the efficiency of this protocol, i.e. to alleviate the head-of-line blocking problem in case of a single transmit buffer, k transmit buffers are deployed at each node equaling the number of virtual channels in the network. Thereby, the incoming packets are placed into those buffers according to their destination addresses, i.e. a packet destined to node d is put into buffer b, where

$$b = d \text{ modulo } k \qquad (b = 0, 1, \ldots, k-1 \,; d = 1, 2, \ldots, N)$$

Thus, when a backlogged node detects an empty slot with slot number s it then checks whether there is a packet awaiting transmission in the buffer corresponding to the current slot number, meaning in buffer $b = s$ modulo k. The considered buffer configuration is shown in Fig. 4.

In summary, this access protocol guarantees that the destination nodes meet their reception requirements, however, it suffers from the fact that some slots are wasted when there is nothing to send to a certain destination node. In order to make the medium access more flexible, a *dynamic* channel (slot) allocation may be envisaged where destination node occupancies could be recorded at each node via tables and accordingly different channels can be used for reception.
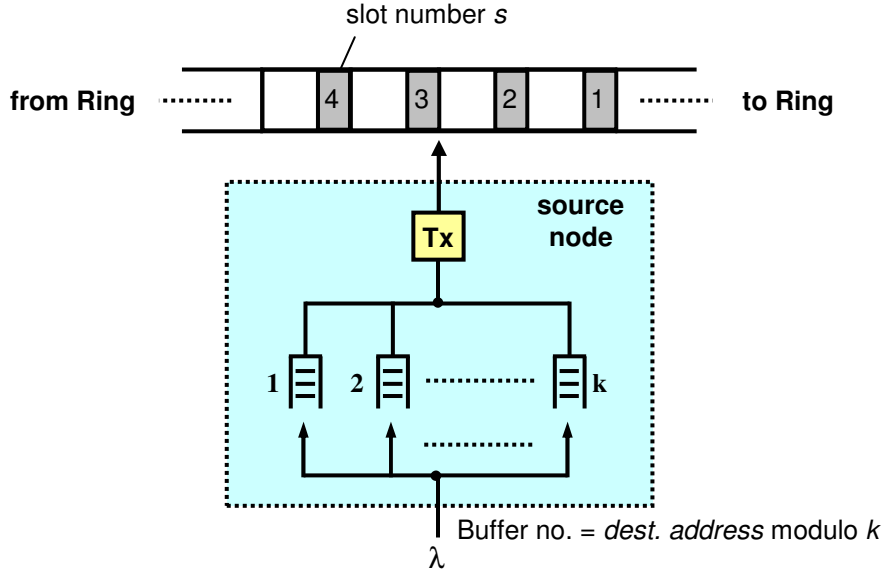
Figure 4: Buffer configuration for the proposed fixed-assignment access protocol

4. Performance Study

A performance study is carried out by means of discrete-event simulation in order to gain deeper insight into the behaviour of the discussed protocol. The network throughput, the message transfer delay, and the packet transfer delay have been taken as performance measures. The *message transfer delay* is defined as the time period between the message generation and the moment when the packet has been completely received by the destination. The *packet transfer delay* is defined as the amount of time elapsed since a packet (acquired from a message) has reached the first place of the transmit queue until the packet has been completely received at the destination.

Concerning the traffic pattern we assumed a homogeneous load derived from a Poisson process with mean arrival rate λ. The message length is exponentially distributed and its mean value is here set to $l = 5$ slots. Furthermore, the nodes attached to the network are equidistantly spaced along the ring. In terms of the node parameters, we have adopted the values derived in section 3, i.e., the slot period T_s is set to 86 ns (corresponding to a payload length of 8.5 kbit and a header length of 64 bits for 100 Gbit/s), while assuming the header processing latency to be $T_{hp} = 55$ ns. Additionally, the number of nodes was chosen to $N = 20$ for our considerations.

In this performance study, particular attention is paid to the comparison of the 100 Gbit/s ring with a system operating at a medium rate of 2.5 Gbit/s in order to find out whether the implementation of the 100 Gbit/s access nodes with the processing delays as bottlenecks is justified regarding the additional costs in terms of the optical packet compression/decompression and OTDM multiplexer/demultiplexer units.

Fig. 5 illustrates the delay/throughput behaviour for both considered delay types and a number of slots on the ring being $n = 150$ (corresponding to a ring length of $L \approx 2.6$ km). Four different scenarios are considered here, namely the proposed ring network with the processing restrictions corresponding to $k = 40$ and $k = 10$, respectively, compared to a conventional Slotted Ring scheme, where each empty slot can be used for reception, i.e. $k = 1$, operating at 100 Gbit/s (assuming that the attached nodes could achieve 100 Gbit/s without processing overhead) and 2.5 Gbit/s. Concerning the packet transfer delay, which is particularly decisive for real-time transmission it can be observed that the system with $k = 10$, i.e. the node configuration (b), behaves close to the "ideal" schemes with $k = 1$, whereas the node

architecture (a) leads to significant degradations compared to the other cases. Apparently, the processing overhead associated with deploying solely optical compression at the nodes is too large to obtain an efficient access scheme.

In terms of the message transfer delays, where the queuing delay is included, it may be clearly seen that a 100 Gbit/s slotted ring shows a superior behavior compared to a 2.5 Gbit/s ring network only when node architecture (b), i.e. $k = 10$, is considered (partly deviations of about 200 slots !) even though the situation slightly changes for heavy loads. Therefore, it can be claimed that the implementation of an access node operating at 100 Gbit/s by means of optical packet compression and optical time division multiplexing is really justified compared to its 2.5 Gbit/s counterpart. A similar behavior can be observed in Fig. 6, when $n = 300$ ($L \approx$ 5 km) is considered while keeping the remaining parameters unchanged.
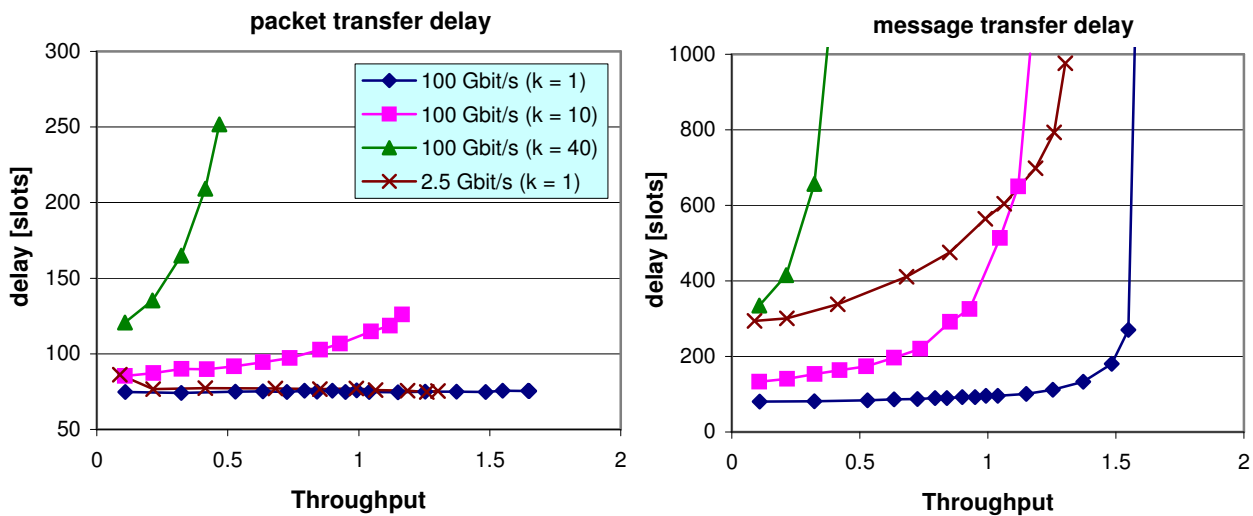

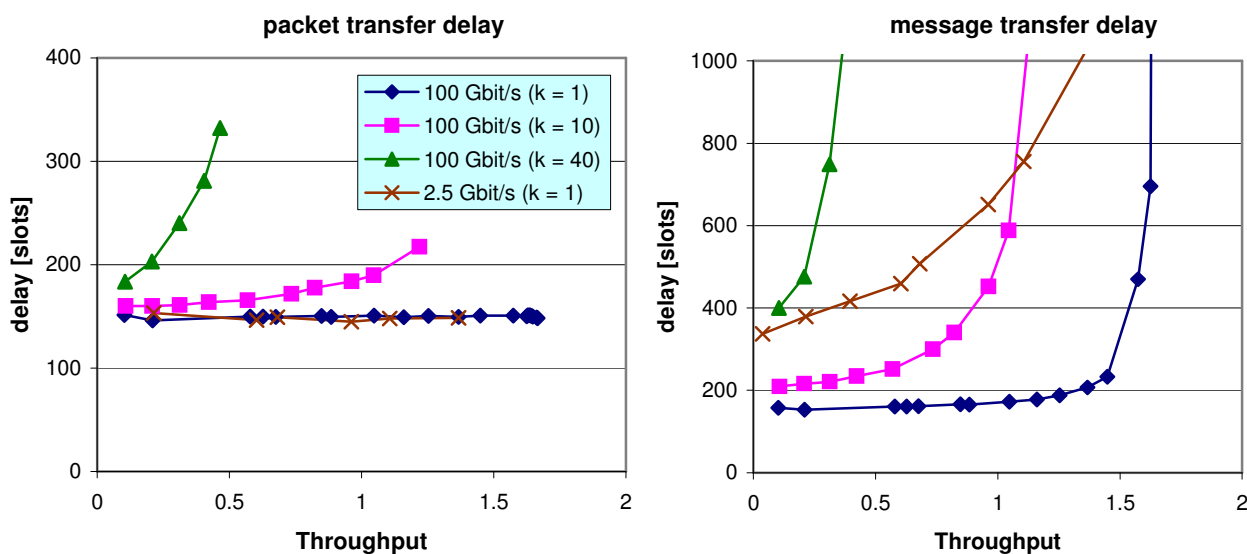**Figure 5:** Delay-throughput behavior for $N = 20$ and $n = 150$

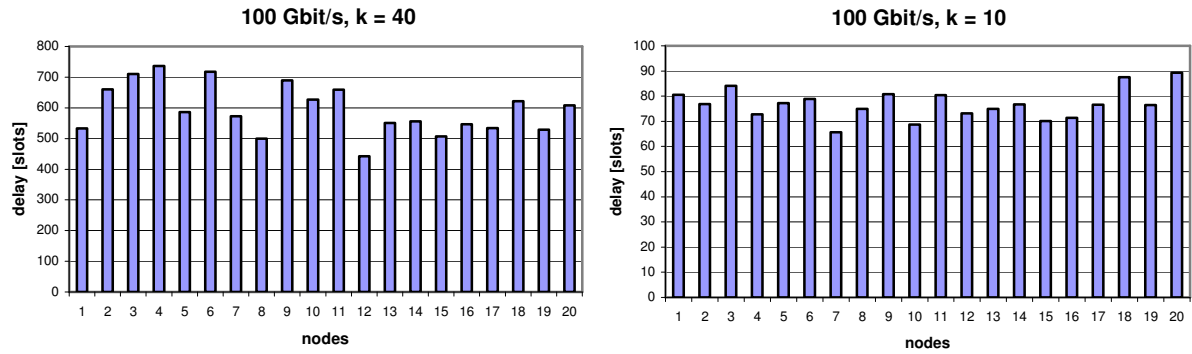**Figure 6:** Delay-throughput behavior for $N = 20$ and $n = 300$

Figure 7: Access delays of the individual nodes for $N = 20$, $n = 150$, and $\lambda = 0.003$

Furthermore, the individual mean message access delays (excluding the propagation delay) are plotted against the nodes in Fig. 7, in which an almost fair access among the nodes (maximum difference ≈ 20 slots) under the above mentioned assumptions can be recognized for the $k = 10$ case, in contrast to $k = 40$.

5. Conclusion

In this paper, we proposed two different node architectures for a high-speed packet-switched ring-LAN employing optical packet payload compression and decompression. Taking the processing overheads of these architectures into account a fixed-assignment access protocol based on the Slotted Ring scheme with destination release has been designed using several virtual channels. The performance study clearly revealed that the implementation of such a 100 Gbit/s ring network with access nodes also operating at 100 Gbit/s speed at the expense of additional processing latency is justified compared to its 2.5 Gbit/s counterpart without this processing bottleneck.

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