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Analysis of Geometric Charge-Pumping Components in a Thin-Film SOI Device

Otto Heinreichsberger, Predrag Habaš and Siegfried Selberherr

Institute for Microelectronics, Gußhausstraße 27–29, A-1040 Vienna, Austria

Abstract

A numerical analysis of the charge-pumping experiment in thin-film SOI *pin*-diodes is presented. The approach is based on the self-consistent two-dimensional numerical solution of the time-dependent semiconductor equations including the interface trap dynamic equations, which are solved for interface traps on the front and on the back interface of the SOI device. We can identify two distinct mechanisms of parasitic recombination on the back interface which show up for steep edges of the front gate pulse train. The influence of accumulation or inversion of the back interface on the appearance of these parasitic effects is analyzed numerically and comparisons of simulation results with measurement data are shown.

1. INTRODUCTION

Interface-trap characterization by the charge-pumping method has become a reliable and fast measurement technique in silicon MOSFET's [1]. This technique can be extended for application to thin-film SOI devices by either providing a separate sidewall contact on the substrate [2] or by using *pin*-structures [3]. The charge-pumping experiment in a thin-film SOI *pin*-diode, to which our analysis is restricted, is carried out by pumping the front interface while the buried back interface is held in accumulation or inversion. The accumulation or inversion layer on the back interface is needed to prevent an unwanted potential coupling of the back interface to the front interface. Similarly, by holding the front interface in inversion or accumulation and applying a pulse train on the substrate contact, charge can be pumped through the interface traps on the back interface. Thus, the interface trap densities on the front interface as well as on the back interface may be determined separately [4]. Ideally, supply of electrons to and removal from the inversion layer comes from the n^+-region. Analogously, holes from the accumulation layer are supplied and removed from the p^+-region. Note that the electrons flow across a *pn*-junction, while the holes do not.

A limitation on the applicable rise- and fall-times of the front gate pulse train is the appearance of geometric, also called *dimensional*, components in the charge-pumping signal [4] which contain no direct information of interface-state densities. These components have recently been accounted for by parasitic recombination processes of carriers on the inverted or accumulated back interface [4]. In this work we present an interpretation of these parasitic charge-pumping components in thin-film double-gated SOI *pin*-diodes by two-dimensional transient simulations using the device simulator MINIMOS.

2. MODEL

We have implemented a numerical model which is described in [5] and [6]. Fig. 1 shows the geometry of the thin-film device. The relevant device parameters which have been extracted from [4] and which are used throughout the calculations are summarized in the table below. Due to the low bulk doping N_B and the small film thickness T_{soi}, the silicon film is fully depleted. We have assumed a spatially homogenous density N_{ss}^F of acceptor-like traps at the front interface corresponding to the line $\overline{AB}$ in Fig. 1, linearly distributed in the energy gap. A considerably higher density of interface states N_{ss}^B has been assumed on the back interface, corresponding to the line $\overline{CD}$ in Fig. 1. A fixed positive oxide charge on the back interface N_{ox}^B has been used to adjust the peak in the charge-pumping current I_{cp} to U_{G2}=0V, i.e. when the back interface is in depletion and both interfaces contribute to I_{cp} (see [4]). This is due to the potential coupling of both interfaces in fully depleted devices.

3. GEOMETRIC COMPONENTS

Figs. 3 and 4 show the dependence of the charge-pumping current I_{cp} on the rise/fall times (t_r=t_f) of the front gate voltage $U_{G1}(t)$. Fig. 3 shows the case of an inverted back interface (U_{G2} = 15V), Fig. 4 the case of an accumulated back interface (U_{G2} = $-15V$). Assuming a linear distribution of interface states in the scanned portion of the energy gap these curves should be linear in the semilogarithmic scale. However a strong departure from linearity is clearly visible in both cases for $L_G \geq 4\mu m$ which is attributed to an additional (parasitic) recombination current caused by the interface traps on the back interface.

To understand the physical mechanisms leading to these effects the rise- and fall-times $t_{r,f}$ of the front gate pulse train are varied separately: Keeping t_r fixed at 1μs and varying t_f a nonlinear increase in I_{cp} is visible only for an *accumulated* back interface (Fig. 2). Conversely, keeping t_f fixed and varying t_r, a nonlinear increase in I_{cp} is visible only for an *inverted* back interface (Fig. 2). This suggests that the parasitic components are generated by two distinct mechanisms which depend on the state of the back interface:

1. Electrons from the inversion layer at the front interface diffuse into the silicon film during the falling edge of the front gate voltage. If the back interface is in *accumulation*, a small portion of these electrons can reach the back interface where

Parameter	Value		Unit	Meaning
L_G	2/4/6/9/20		μm	Geometric Gate Lengths
W_G	200		μm	Geometric Gate Width
T_{ox}	50		nm	Front Gate Oxide Thickness
T_{soi}	150		nm	Silicon Film Thickness
T_{ins}	380		nm	Buried Oxide Thickness
N_B	1.00	10^{16}	cm^{-3}	Homogenous Bulk Doping Concentration
N_{ss}^F	1.62	10^{10}	$cm^{-2}eV^{-1}$	Front Interface Trap Density (Acceptor-like)
N_{ss}^B	9.00	10^{11}	$cm^{-2}eV^{-1}$	Back Interface Trap Density (Acceptor-like)
$\sigma_{n,p}$	2.30	10^{-15}	cm^2	Capture Cross-Sections
N_{ox}^F	1.00	10^{10}	$cm^{-2}eV^{-1}$	Fixed Positive Oxide Charges on Front Interface
N_{ox}^B	3.08	10^{11}	cm^{-2}	Fixed Positive Oxide Charges on Back Interface

they immediately recombine with holes from the back interface accumulation layer, thus contributing to I_{cp}. However, if the back interface is in *inversion*, no parasitic component can occur in the range of fall times shown, since these electrons are absorbed completely in the back interface inversion layer from where they flow back to the n^+-region. Note that this charge-pumping component is quite analogous to the so-called geometric component found in bulk MOSFET's [6].

2. Holes from the front interface accumulation layer diffuse into the silicon film during the rising edge of the front gate voltage. If the back interface is in *inversion* a small portion of these holes surmounts the back interface depletion layer and reaches the back interface where they immediately recombine with electrons, thus contributing to I_{cp}. However, if the back interface is in *accumulation* no parasitic component occurs in the range of rise times shown, since these holes are absorbed in the accumulation layer and subsequently flow back to the p^+-region.

Furthermore, we have analyzed the influence of several device parameters (L_G, N_{ss}^B, $\mu_{n,p}^{BULK}$, $\mu_{n,p}^{SURF}$) and gate bias conditions ($\Delta U_{G1}(t)$, U_{G2}) on both parasitic components. Large values of $\pm|U_{G2}|$ lead to a decrease of the parasitic components, since the repulsive field of the accumulation/inversion layer at the back interface increases. A decrease in the bulk and back surface mobility, or an increase in the channel length respectively leads to a sharp increase in I_{cp}, since it becomes more difficult for the carriers to leave the silicon film. Finally, the parasitic recombination currents are roughly proportional to the density of the interface states on the back interface N_{ss}^B.
Fig. 5 (falling edge of $U_{G1}(t)$, $U_{G2} = -15V$) and Fig. 6 (rising edge of $U_{G1}(t)$, $U_{G2} = 15V$) show the time-evolution of the front and back interface generation currents. The appearance of an electron recombination current (I_n-B) is observable on the accumulated back interface in Fig. 5, whereas a hole recombination current (I_p-B) is observable on the inverted back interface in Fig. 6.

4. CONCLUSION

A two-dimensional transient numerical model has been developed to simulate the charge-pumping experiment in thin-film SOI *pin*-diodes directly. We have applied this new method to explain the anomalous increase of the charge-pumping current which arises for short gate pulse edges and channel lengths larger than $2\mu m$. This increase in I_{cp} is explained by the appearance of so-called geometric or dimensional components in I_{cp} which are a consequence of the proximity of the back interface, where a large number of interface traps is located, to the front interface. The influence of the rise/fall times of the front gate voltage pulses, the back gate voltage and the channel length has been demonstrated. A good agreement between the proposed model and experimental data has been achieved.

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REFERENCES

1 G.Groeseneken *et al.*,*IEEE ED 31*, p.42-53.
2 D.J.Wouters *et al.*, *IEEE ED 36*, p.1746-1750.
3 T.Elewa *et al.*,*ESSDERC 1988*, p.137-140.
4 T.Ouisse *et al.*, *IEEE ED 38*, p.1432-1444.
5 O.Heinreichsberger, Dissertation, Tech.Univ.Vienna, 1992.
6 P.Habaš *et al.*, in these proceedings.

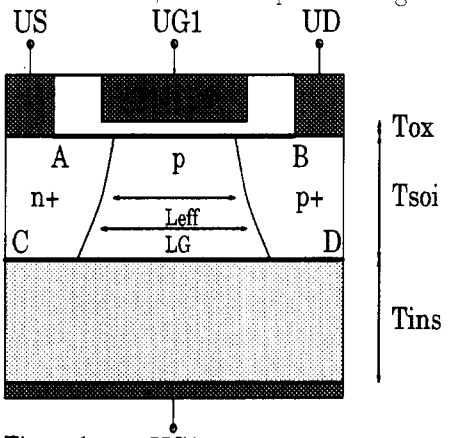
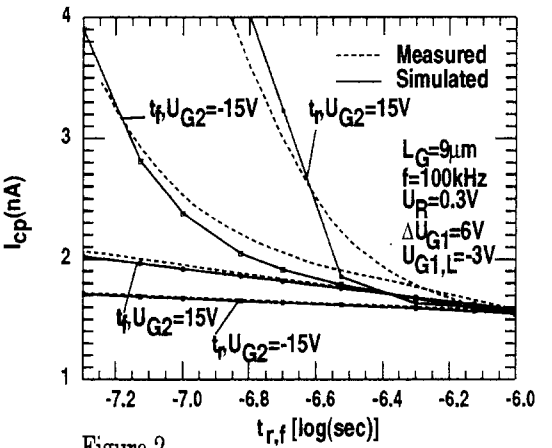


Figure 1



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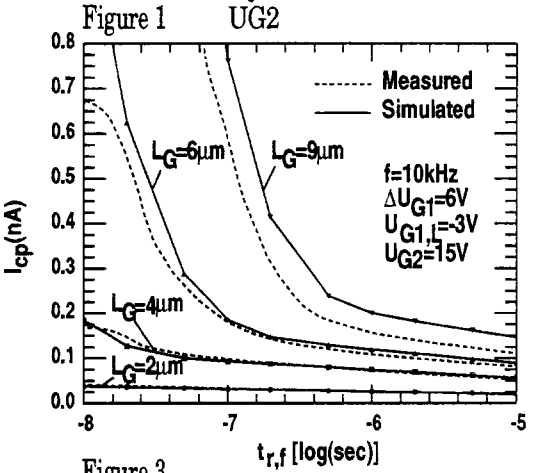

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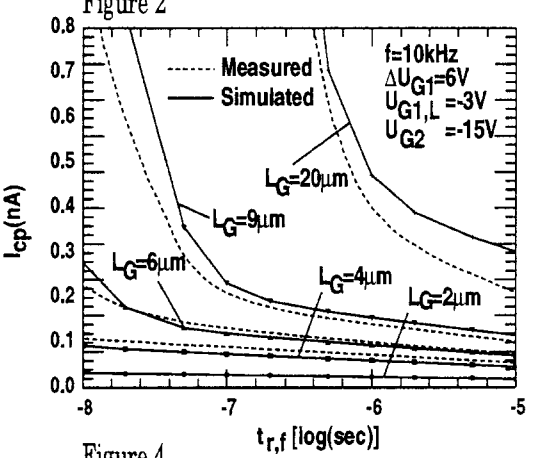

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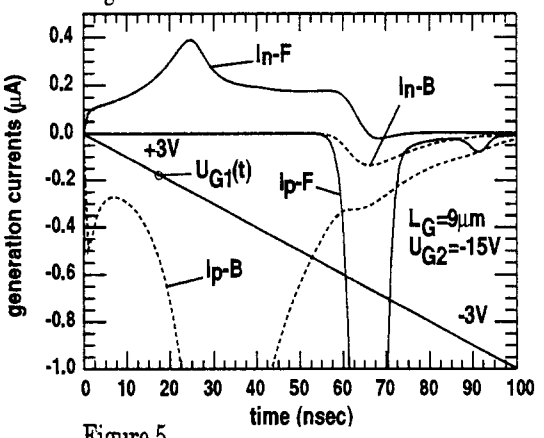

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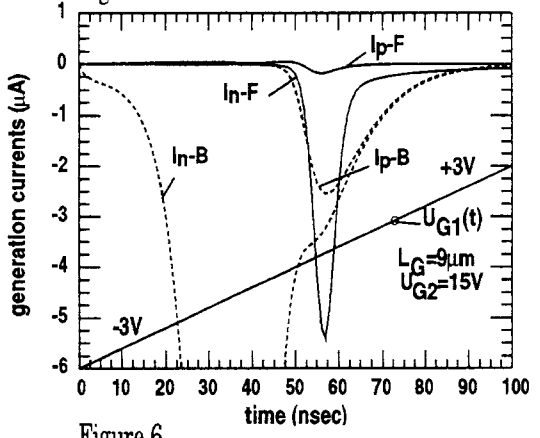

Figure 6