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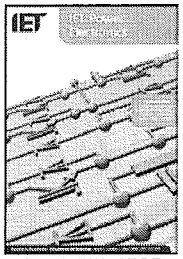

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Comparative evaluation of modulation methods of a three-phase buck + boost PWM rectifier. Part II: Experimental verification

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Abstract: This paper presents experimental results of a comparative evaluation of two different modulation methods for a three-phase buck + boost PWM rectifier. The measurements, which are performed on a 5 kW digital signal processor controlled prototype, verify the analytical calculations and simulations in part I and identify one modulation method to be clearly superior regarding the input filter capacitor voltage ripple and the DC link inductor ripple values. Finally, also the EMC noise emission levels are comparatively analysed for the modulation methods.

1 Introduction

In this paper the theoretical considerations in [1] are verified by measurements on a 5 kW prototype of the three-phase buck + boost PWM rectifier. The local and global time behavior of the input filter capacitor voltage ripple Δu_{C_1} and of the DC link inductor current ripple Δi is shown for different modulation methods. As for the theoretical considerations in [1], the measurements are carried out for the following operating points:

Buck operating point: $P_0 = 5\,\text{kW}$, $U_{N,ll} = 400\,\text{V}$, $U_0 = 400\,\text{V}$, $M = 0.82$, $\delta = 0$

Buck + Boost operating point: $P_0 = 5\,\text{kW}$, $U_{N,ll} = 230\,\text{V}$, $U_0 = 400\,\text{V}$, $M = 0.90$, $\delta = 0.37$

and for the following operating parameters:

$f_N = 50\,\text{Hz}$, $C_1 = 8.2\,\mu\text{F}$, $L_1 = 240\,\mu\text{H}$,
$L = 2 \times 1\,\text{mH}$, $f_{p1} = 28\,\text{kHz}$, $f_{p2} = 16.2\,\text{kHz}$.

The power semiconductors of one bridge leg of the buck input stage are integrated in a power module VUI 31-12N1 [2] in order to achieve a higher power density. The prototype is designed as a stand-alone system including auxiliary power supply, a DSP (digital signal processor) control board and an EMC (electromagnetic compatibility) input filter (Fig. 1*a*). For active boost output stage, the on-state of the boost power transistor is centered to the free-wheeling state of the buck input stage, that is, modulation method 1.1 (cf. Fig. 9*c* in [1]) is applied. The mains behavior showing unity power factor operation is given in Fig. 1*b*.

2 Experimental results for input filter capacitor voltages

Since the behaviour of the input filter capacitor voltage ripple is dependant only on the operation of the buck input stage (i.e. on the modulation index M) and independent on the operation of the boost output stage, the results are shown only for the buck operating point with $M = 0.82$.

In Fig. 2 experimental results and simulation results of the global time behaviour of the input filter capacitor voltage ripple $\Delta u_{C_1,R}$ in phase R are given for half a

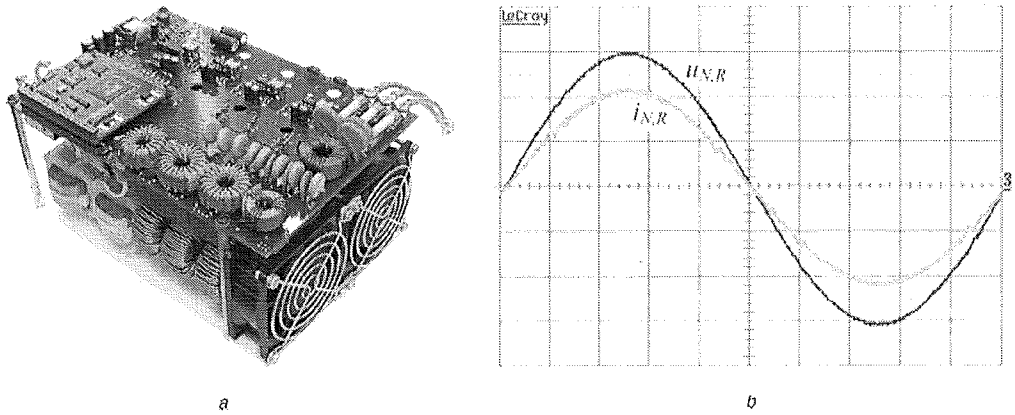

Figure 1 *Mains behaviour showing unity power factor operation*
a Prototype of the three-phase buck + boost PWM rectifier including DSP control board, auxiliary power supply and EMC input filter Overall dimensions: (240 × 160 × 120 mm^3)
b Measured rectifier mains current and mains phase voltage for the operating parameters
Scales: $i_{N,R}$: 5 A/div, $u_{N,R}$: 100 V/div, t: 2 ms/div

mains period. The ripple values are very small ($\Delta u_{C_1,i} < 10$ V) as compared with the 50 Hz components ($\hat{U}_{C_1,i} = 326$ V) therefore the resolution of this measurement is not sufficient to accurately display the ripple waveform. However, the measured amplitudes of the ripple components equal the simulation results. A very good conformity is given if the analytically derived envelopes of the input filter capacitor voltage ripple

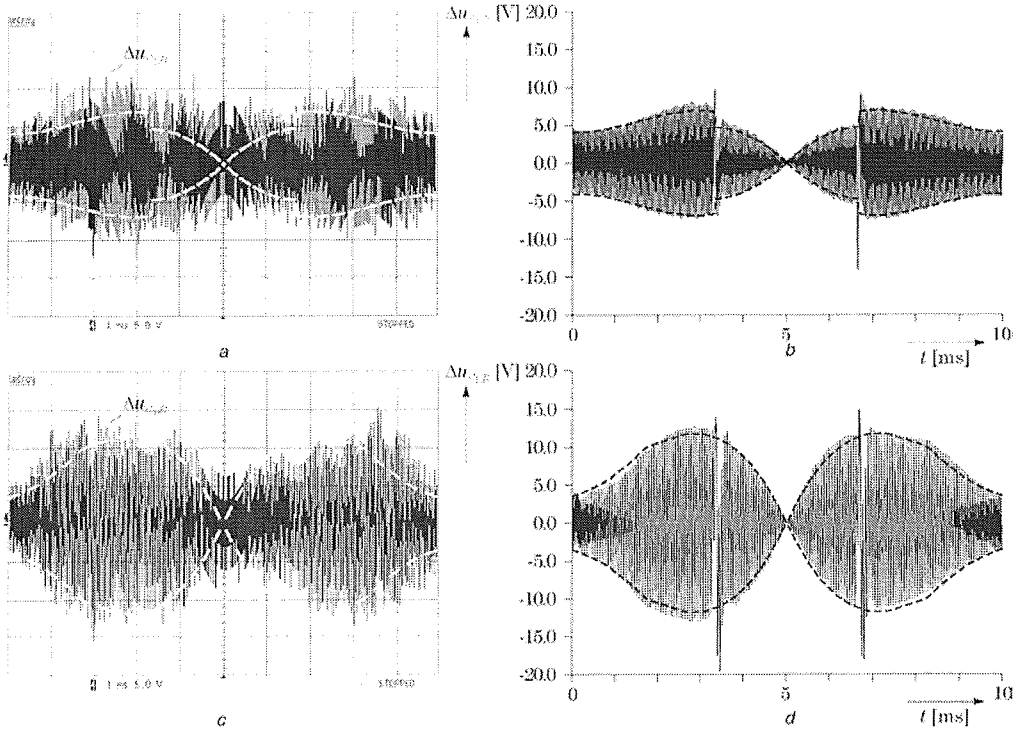

Figure 2 *Input filter capacitor voltage ripple $\Delta u_{C1,R}$ in phase R within half a mains period*
a Experimental results and analytically calculated envelopes (dashed curves, cf. Fig. 8 in [1]) for modulation method 1
b Related simulation results and analytically calculated envelopes (dashed curves, cf. Fig. 8 in [1]) for modulation method 1
c Experimental results and analytically calculated envelopes (dashed curves, cf. Fig. 8 in [1]) for modulation method 2
d Related simulation results and analytically calculated envelopes (dashed curves, cf. Fig. 8 in [1]) for modulation method 2
Scales: $\Delta u_{C1,R}$: 5 V/div; t: 1 ms/div

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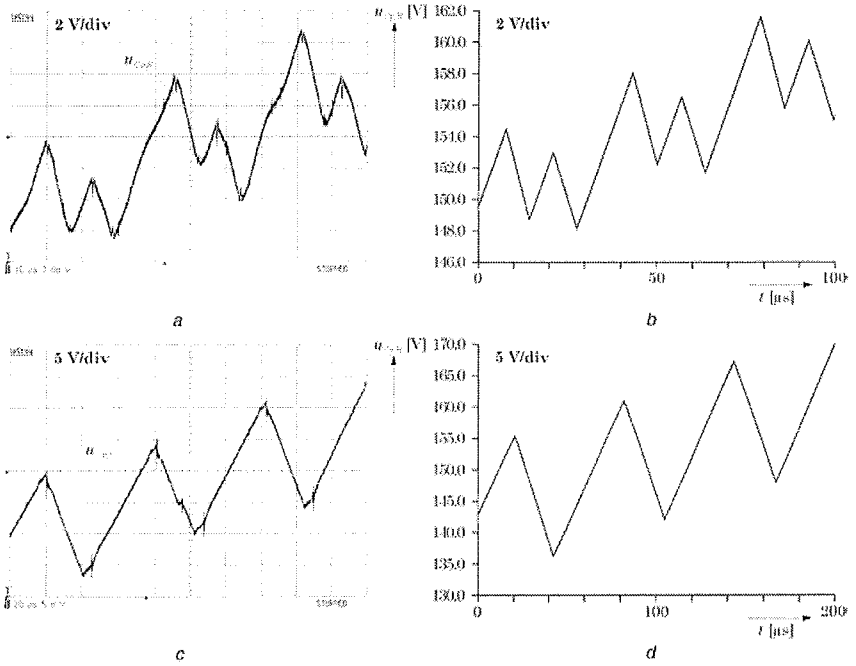

Figure 3 *Input filter capacitor voltage$u_{C1,R}$ in phase R within approximately three pulse periods*
a Experimental results for modulation method 1 (scales: $u_{C1,R}$: 2 V/div; *t*: 10 μs/div)
b Related simulation results for modulation method 1 (scales: $u_{C1,R}$: 2 V/div; *t*: 10 μs/div)
c Experimental results for modulation method 2 (scales: $u_{C1,R}$: 5 V/div; *t*: 20 μs/div)
d Related simulation results for modulation method 2 (scales: $u_{C1,R}$: 5 V/div; *t*: 20 μs/div)

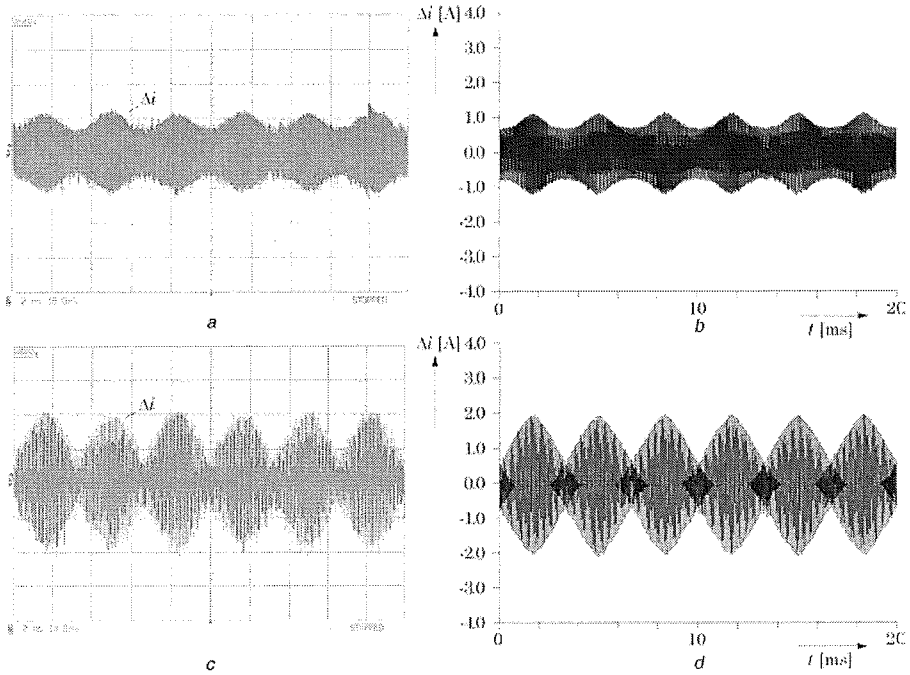

Figure 4 *DC link current ripple Δi within one mains period*
a Experimental results for disabled boost stage for modulation method 1
b Related simulation for disabled boost stage for modulation method 1
c Experimental results for disabled boost stage for modulation method 2
d Related simulation for disabled boost stage for modulation method 2
Scales: Δ*i*: 1 A/div; *t*: 2 ms/div

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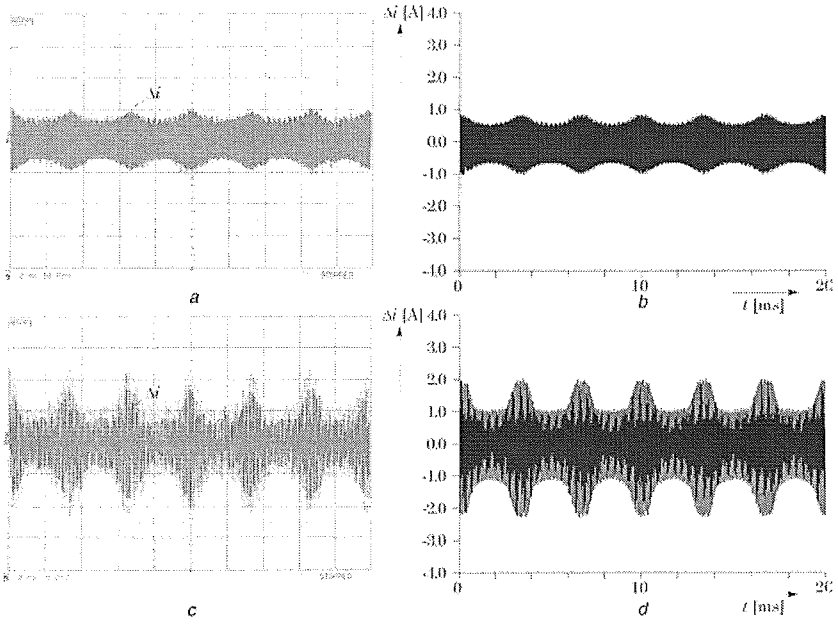

Figure 5 *DC link current ripple Δi within one mains period*
a Experimental results for active boost stage for modulation method 1
b Related simulation results for active boost stage for modulation method 1
c Experimental results for active boost stage for modulation method 2
d Related simulation results for active boost stage for modulation method 2
Scales: Δ*i*: 1 A/div; *t*: 2 ms/div

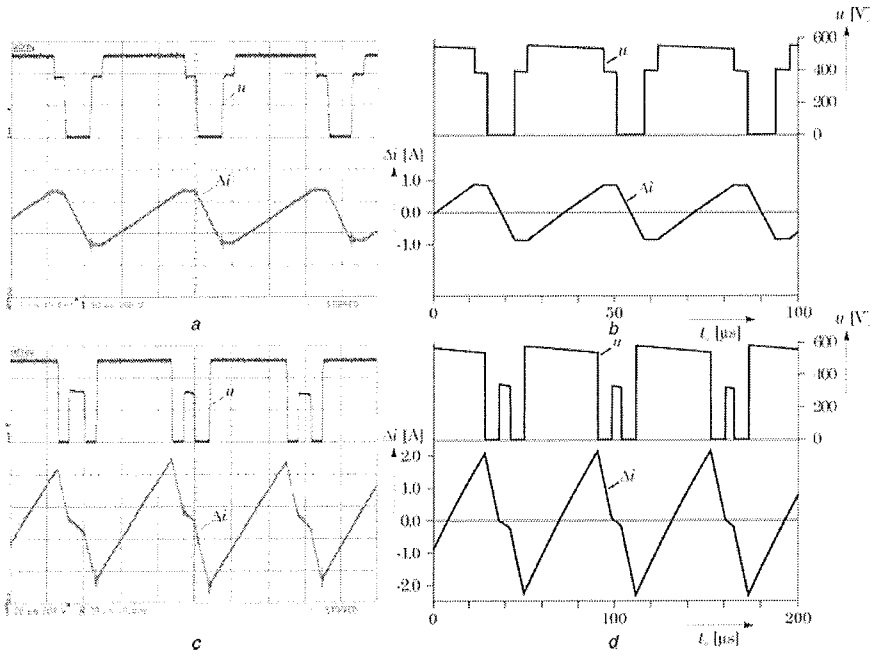

Figure 6 *Buck stage output voltage u and DC link current ripple Δi for disabled boost stage within approximately three pulse periods*
a Experimental results for modulation method 1 (*t*: 20 μs/div)
b Related simulation results for modulation method 1 (*t*: 20 μs/div)
c Experimental results for modulation method 2 (*t*: 10 μs/div)
d Related simulation results for modulation method 2 (*t*: 10 μs/div)
Scales: *u*: 200 V/div; Δ*i*: 1 A/div

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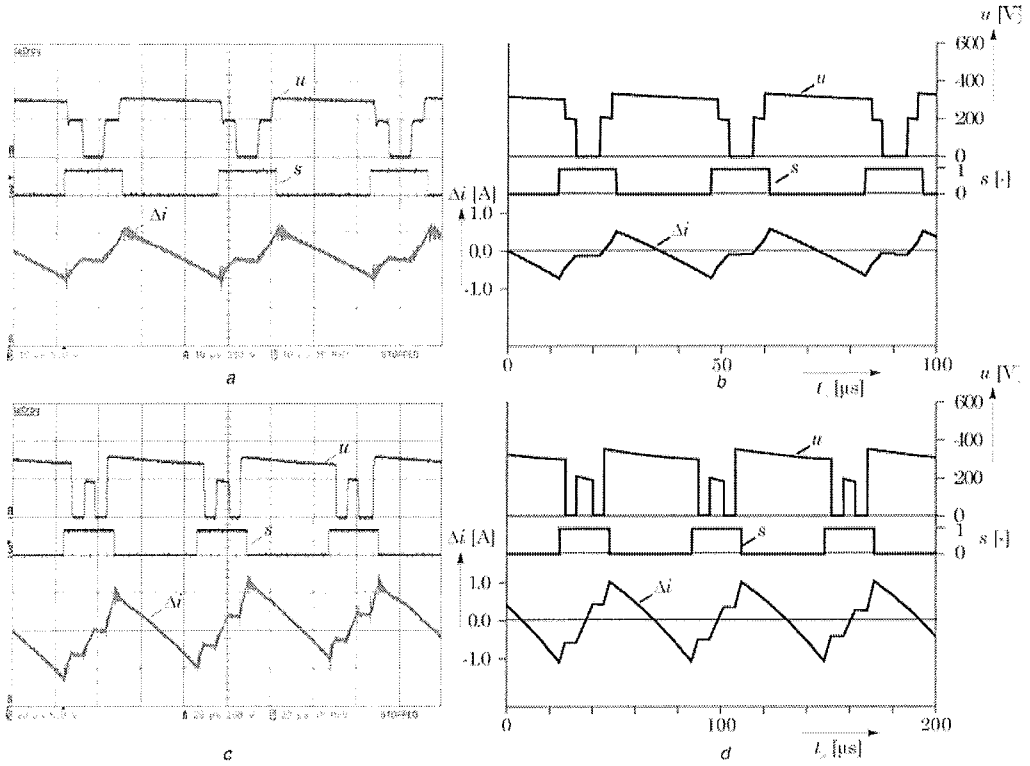

Figure 7 *Buck stage output voltage u, switching signal s of the boost IGBT and DC link current ripple Δi for active boost stage within approximately three pulse periods*
a Experimental results for modulation method 1 (*t*: 20 μs/div)
b Related simulation results for modulation method 1 (*t*: 20 μs/div)
c Experimental results for modulation method 2 (*t*: 10 μs/div)
d Related simulation results for modulation method 2 (*t*: 10 μs/div)
Scales: *u*: 200 V/div; *Δi*: 1 A/div

shown in Fig. 8 in [1] are compared with the simulation results neglecting the distortion at the sector boundaries at $\varphi_{rec} = \pi/3$ and $\varphi_{rec} = 2\pi/3$. For modulation method 1 these distortions can be eliminated by simply adding an overlapping time between the active switching states [3], for example, for $\varphi_{rec} \in (0;\ \pi/6)$ between switching states $j = (101)$ and $j = (110)$ switching state $j = (111)$ is added during an short overlapping time.

The local behaviour of the input filter capacitor voltage $u_{C_1,R}$ in phase R within approximately three pulse periods is shown in Fig. 3 for both modulation methods 1 and 2. Considering the different voltage scales (2 V/div for modulation method 1 and 5 V/div for modulation method 2) one can see immediately that modulation method 1 provides a substantially smaller voltage ripple.

3 Experimental results for DC link current

The DC link inductor, which is realised by an iron alloy core [4], shows a slight dependency on the DC link current: we have $L = 2 \times 0.9$ mH at the buck operating point and $L = 2 \times 0.75$ mH at the boost operating point. These values are implemented in the simulation.

In Figs. 4 and 5 the global time behaviour of the DC link current ripple is shown for both modulation methods and for both operating points. There, a good conformity between experimental results and simulation results is given. Furthermore, the results depicted in Fig. 4 can be compared with the analytical results for the envelope of the DC link current in Fig. 12 in [1], where the reduced inductance value of $L = 0.9$ mH has to be taken into account. If the analytically calculated envelopes of Fig. 12 in [1] are multiplied with a factor $1/0.9$ mH $= 1.1$, a good conformity is shown too.

Experimental results and simulation results of the local time behaviour within approximately three pulse periods of buck stage output voltage u, switching signal s of the boost power transistor (for $s = 1$ the insulated gate bipolar transistor (IGBT) is in the on-state) and local time behaviour of the DC link current ripple Δi are shown in Figs. 6 and 7. Again, the results show a very good conformity. Therefore it is proved by experimental results

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that the theoretical considerations and simulations provide an accurate description of the actual circuit behaviour and that the modulation method 1 is clearly superior regarding ripple values and switching losses.

4 EMC aspects

Finally, the effect of the two modulation methods on the electromagnetic compatibility (EMC) filter requirements shall be investigated experimentally. Since the common mode (CM) filter is strongly depending on the PCB layout and is usually much smaller than the differential mode (DM) filter, only the DM part is considered here.

In Figs. 8*a* and 9*a* the distribution of harmonics of the input rectifier current around the pulse frequencies ($f_{p1} = 28$ kHz and $f_{p2} = 16.2$ kHz) is shown for the two modulation methods for the operating parameters given in Section 5.4 in [1]. As can be seen, the modulation has an influence on the amplitudes of the

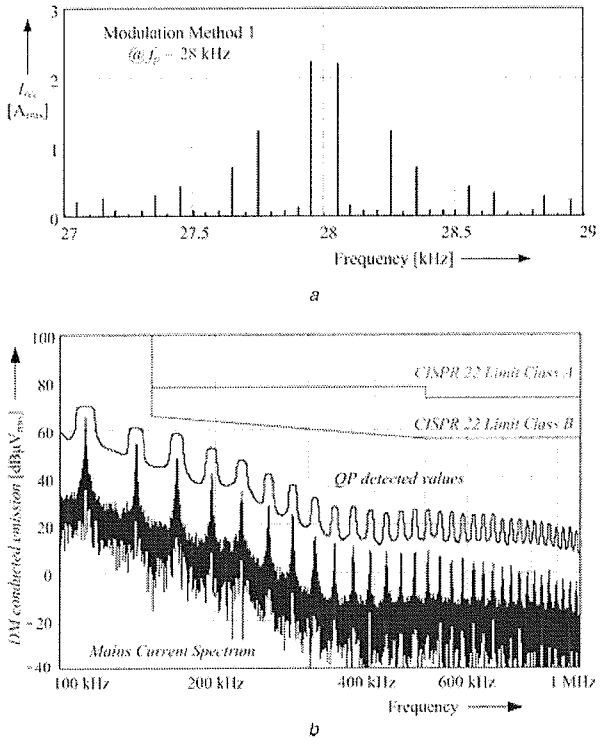

Figure 8 *Input rectifier current spectrum and simulated EMC QP measurement result and mains current spectrum for a two-stage input filter topology with C1 = 8.2 µF, L1 = 240 µH, C2 = 470 nF (zoom for the frequency range of 100 kHz − 1 MHz)*

a Input rectifier current spectrum (zoom around the pulse frequency) for modulation method 1

b Simulated EMC QP measurement result and mains current spectrum

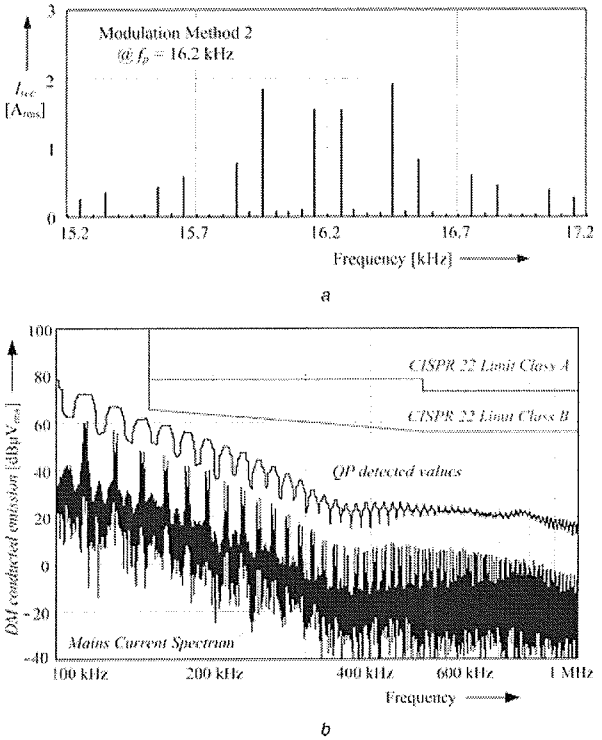

Figure 9 *Input rectifier current spectrum and simulated EMC QP measurement result and mains current spectrum for a two-stage input filter topology with C1 = 8.2 µF, L1 = 240 µH, C2 = 330 nF (zoom for the frequency range of 100 kHz − 1 MHz)*

a Input rectifier current spectrum (zoom around the pulse frequency) for modulation method 2

b Simulated EMC QP measurement result and mains current spectrum

harmonics (and also the phases that are not shown), which in consequence changes the noise emission detected by the EMC test receiver. For fulfilling the CISPR 22 standards [5], the quasi-peak (QP) detection method has to be utilised [6], and the detected values have to lie below the limits shown in Figs 8*b* and 9*b*.

Following the DM filter design procedure [6], a two-stage filter has been designed based on the simulation of the noise emission because of the rectifier input currents for the two modulation methods. It has been found that a two-stage filter is necessary in both cases to sufficiently suppress the noise emission. For modulation method 1, a filter attenuation of 87.8 dB is required, which translates to the following filter elements.

$$\begin{aligned} C_1 &= 8.2\,\mu\text{F} \\ L_1 &= 240\,\mu\text{H} \\ C_2 &= 470\,\text{nF} \end{aligned} \tag{35}$$

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The filter capacitor C_2 forms the second filter stage together with the mains inductance or with the line impedance stabilisation network impedance for the measurement process, respectively. With these values, a 6 dB margin is kept from the CISPR 22 Class B limit over the whole measurement range as can be seen in Fig. 8*b*.

For modulation method 2 (at a pulse frequency of 16.2 kHz), a lower filter attenuation of 81.5 dB is required, which results in slightly smaller filter elements

$$\begin{aligned} C_1 &= 8.2\,\mu\text{F} \\ L_1 &= 240\,\mu\text{H} \\ C_2 &= 330\,\text{nF} \end{aligned} \tag{36}$$

The simulated EMC QP measurement with these values is shown in Fig. 9*b*. Again, a 6 dB margin is kept from the CISPR 22 Class B limit. By comparing the two designed filters, it can be stated that they are practically identical and only slightly differing in the capacitance value for C_2.

5 Conclusions

In this paper the local and global time behavior of the input filter capacitor voltage ripple and of the DC link inductor current ripple has been evaluated experimentally for two different modulation methods on a 5 kW hardware prototype. The measurement results verify the theoretical considerations, which have been carried out in [1], and prove the superior performance of modulation method 1 in terms of ripple values.

This optimum modulation method is characterised by the free-wheeling state of the buck input stage being placed at the beginning/at the end of one pulse half period, and by a turn-on interval of the boost stage power transistor being centered in the free-wheeling interval of the buck stage [1]. The switching frequencies have been adapted accordingly to maintain the same switching losses for both cases.

Furthermore, it has been shown that the choice of modulation method has insignificant influence on the size of the input filter that is required for compliance with EMC noise emission standards.

6 References

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