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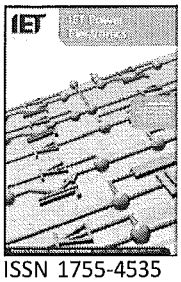

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Comparative evaluation of modulation methods of a three-phase buck + boost PWM rectifier. Part I: Theoretical analysis

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Abstract: Different switching state sequences of a three-phase three-switch buck-type unity power factor PWM rectifier with integrated DC/DC boost output stage are presented. They are analysed concerning switching losses and ripple components at the input (filter capacitor voltage ripple) and at the output (DC link current inductor ripple). For a fair comparison, pulse frequencies of different modulation methods are adopted in order to achieve the same switching losses. The rms value and envelopes and time behaviour of the ripple components are analysed analytically and by simulation, and one advantageous modulation method is determined. The paper provides the basis for a subsequent experimental verification, which is performed in part II.

1 Introduction

For the realisation of the rectifier input stage of three-phase telecommunications power supply modules with sinusoidal input current, there are basically two possibilities: (i) a buck-type rectifier (conventionally six-switch topologies [1, 2]) or (ii) a boost-type rectifier (e.g. Vienna rectifier [3]). Dependant on this, the amplitude of the mains line-to-line voltage defines a lower or an upper limit of the input voltage of the DC/DC converter output stage being fed by the rectifier. Therefore designing the power supply module for world-wide applicability, that is, for a mains voltage range of 208–400 V line-to-line results in a high blocking voltage and high current stress and/or low utilisation of power semiconductors and passive components [4]. Moreover, this results in a relatively low efficiency of the energy conversion and high realisation costs of the rectifier system.

In [4, 5] a combination of three single-phase buck-type rectifiers with integrated boost-type output stage has been proposed, which gives the possibility of controlling the input voltage of the DC/DC converter stage to 400 V within the entire wide input voltage range. This results in an advantageous design of the power semiconductors of the rectifier input stage and allows the application of a DC/DC converter technology being well known from systems with single-phase AC supply. Furthermore, an auxiliary start-up circuit as required for rectifier systems with boost characteristic can be omitted, and in contrast to standard buck-type systems, a sinusoidal input current shape can be guaranteed also in the case of a failure of one phase of the mains. However, employing three single-phase units for the realisation of the three-phase system results in a high complexity, that is, comprises in total six turn-off power semiconductors and driver stages, three inductors and three output capacitors and requires special means for achieving a synchronised operation and equal distribution of the total output power to the individual units.

In [6], a novel three-phase three-switch buck-type unity power factor PWM rectifier [7] with integrated DC/DC boost output stage (three-phase buck + boost PWM rectifier) has been presented (Fig. 1), which shows a

significantly lower complexity while maintaining the basic advantages of the combination of a single phase system [8]. A high efficiency (up to $\eta = 95.1\%$) and a high power densitiy ($\rho \simeq 1.09\ \mathrm{kW/dm^3}$ or $17.8\ \mathrm{W/in.^3}$, for a 5 kW setup; Section 7) can be achieved for the proposed system structure.

However, efficiency and power density are partly dependant on switching losses and size of filter components, which are both influenced by the PWM pattern applied to the rectifier stage for forming the mains phase currents and the DC output voltage. Hence, the PWM pattern shows a possibility to optimise the rectifier system.

There are different PWM patterns available, which were implemented in different simulations and various experimental setups [7, 9–13]. The PWM patterns differ concerning the arrangement of active switching states (where current is drawn from the mains) and the free-wheeling state (where the DC link current free-wheels via the buck-stage free-wheeling diode D_F), which influences the local behaviour of voltage and current across passive components. Therefore an optimisation of the operation of the rectifier system is possible by selecting the most advantageous modulation method.

In this paper, the modulation of the three-phase buck + boost PWM rectifier system is analysed concerning

- switching losses [6],
- ripple components at the input (input filter capacitor voltage ripple) [14] and
- ripple components at the output (buck + boost inductor current ripple) [15],

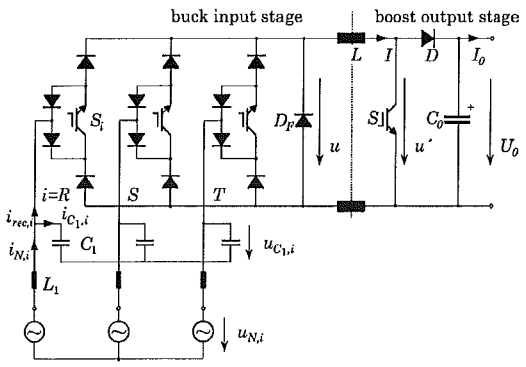

Figure 1 *Structure of the power circuit of the three-phase buck + boost PWM rectifier*

where the pulse frequencies of different modulation methods are adopted in order to achieve the same switching losses for a fair comparison of different modulation methods [16, 17]. All theoretical considerations are verified by simulations and by measurements on a digital signal processor (DSP)-controlled 5 kW prototype of the system. In Section 2, the basic principle of operation of the rectifier system is briefly described. Section 3 treats the different modulation methods wthat are available for controlling the buck input stage and the boost output stage. Based on this, the switching losses are calculated analytically in Section 4, and the ripple components at input and output are analysed in Sections 5 and 6. There, the time behaviour of the ripple components and of their envelopes and, furthermore, the rms values of the ripple components are calculated analytically. In Part II of this paper, the theoretical considerations are verified by digital simulations and by experimental investigations in Section 7. Finally, based on a two-stage filter design, the EMC filtering requirements according to noise emission standards are analysed briefly for the modulation methods in Section 8.

2 Basic principle of operation

In the following, the basic principle of operation of the system depicted in Fig. 1 is briefly explained. On the basis of the investigation of the conducting states, the related current space vectors are calculated and the formation of the rectifier input current space vector is described.

2.1 Assumptions and definitions

For the sake of simplicity, we assume for the further considerations:

- a purely sinusoidal shape of the filter capacitor voltage and/or $u_{C_1,i} \simeq u_{N,i}$, $i = R,S,T$, where the mains voltage $u_{N,i}$ is defined as

$$u_{N,R} = \hat{U}_N \cos(\omega_N t)$$
$$u_{N,S} = \hat{U}_N \cos\left(\frac{\omega_N t - 2\pi}{3}\right) \qquad (1)$$
$$u_{N,T} = \hat{U}_N \cos\left(\frac{\omega_N t + 2\pi}{3}\right)$$

and/or in space vector notation as

$$\underline{u}_N = \hat{U}_N \exp(J\varphi_N) \qquad (2)$$

with $\varphi_N = \omega_N t$, where ω_N denotes the mains angular frequency and

- the inductor current I to be constant and impressed.

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According to $u_{C_1,i} \simeq u_{N,i}$, we will neglect

- the fundamental voltage drop $J\omega_N L_1 \underline{i}_N$ across the input filter inductors L_1, and furthermore, we do neglect

- the mains current ripple, that is, we will consider the mains current $i_{N,i}$ as being equal to the fundamental of the rectifier input current, $i_{\text{rec},(1),i} \simeq i_{N,i}$.

Remark: The space vector related to a triple of phase quantities is calculated according to the defining equation (shown for the example of the buck-stage input current)

$$\underline{i}_{\text{rec}} = \frac{2}{3}(i_{\text{rec},R} + \underline{a} i_{\text{rec},S} + \underline{a}^2 i_{\text{rec},T}) \qquad \underline{a} = \exp\left[\frac{J2\pi}{3}\right] \tag{3}$$

In summary, for an ideally sinusoidal shape of the mains phase voltage, we would like to form a fundamental of the rectifier input current lying in phase with the mains phase voltage ($\varphi_{\text{rec}} \simeq \varphi_N$)

$$\underline{i}^*_{\text{rec},(1)} = \hat{I}_{\text{rec},(1)} \exp[J\varphi_{\text{rec}}] \simeq \underline{i}_N \tag{4}$$

where the index (1) denotes the fundamental component; the switching frequency components of rectifier input phase currents $i_{\text{rec},i}$ are largely suppressed by the input filter (L_1, C_1 in Fig. 1).

2.2 Conduction states, current space vectors and formation of the mains current

Because of the phase symmetry of the converter structure and because of the (assumed) symmetry of the mains voltage system, the investigation can be constrained to a $\pi/6$-wide interval of the mains period. For the case at hand, we will consider the interval $\varphi_{\text{rec}} \in (0;\pi/6)$ being characterised by a relation of the mains phase voltages of $u_{N,R} > 0 > u_{N,S} > u_{N,T}$.

The characterisation of the switching state of the buck rectifier is given by the combination $j = (s_R\, s_S\, s_T)$ of the phase switching functions. For the denomination of the switching states of the insulated gate bipolar transistors (IGBTs) S_i, $i = R,S,T$, switching functions s_i are used in the following, where $s_i = 0$ denotes the off state, and $s_i = 1$ denotes the on state of one power transistor. If a power transistor S_i is in the on-state, the bridge leg i corresponds to a bridge leg of a conventional diode bridge [6]. The conduction states of the rectifier system used in the considered mains interval are

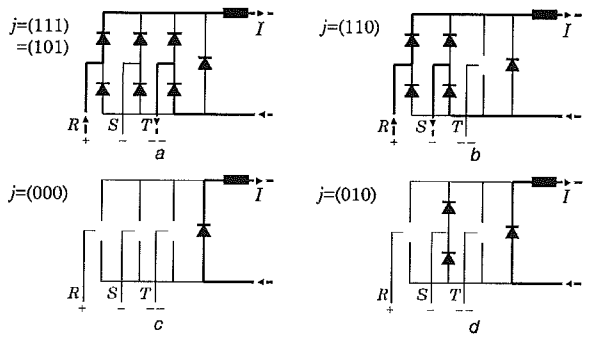

Figure 2 *Conduction states of the buck rectifier valid for $u_{N,R} > 0 > u_{N,S} > u_{N,T}$*
a and *b* Active switching states
c and *d* Free-wheeling states
Current flow is indicated by a bold line
IGBTs are not shown explicitly for the sake of clarity

shown in Fig. 2. Fig. 3 shows the related input current space vectors, that are calculated based on (3).

For switching state $j = (111)$, there follows $i_{\text{rec},R} = +I$, $i_{\text{rec},S} = 0$ and $i_{\text{rec},T} = -I$ due to $u_{N,R} > u_{N,S} > u_{N,T}$ (Fig. 2*a*); the same input current condition is achieved by switching state $j = (101)$. For switching state $j = (110)$, one receives $i_{\text{rec},R} = +I$, $i_{\text{rec},S} = -I$ and $i_{\text{rec},T} = 0$. The free-wheeling state can be achieved by switching all power transistors in the off-state (Fig. 2*c*) or one power transistor can be kept in the on-state, for example, power transistor S_S in Fig. 2*d*; however, because of the higher forward

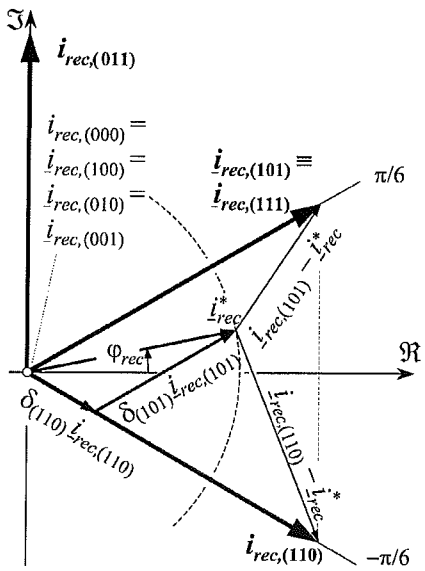

Figure 3 *Input current space vectors $i_{\text{rec},j}$ according to Fig. 2 and (3), valid for $u_{N,R} > u_{N,S} > u_{N,T}$, approximation of the reference vector i^*_{rec} via neighbouring current space vectors, and deviation between reference and actual space vectors*

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voltage drops in the bridge leg, the free-wheeling path will always lead via the free-wheeling diode D_F.

Switching state $j = (011)$ resulting in input current space vector i_{rec}, $(011) = (2/\sqrt{3})jI$ is not used in the considered mains interval, because for the formation of a given reference value i^*_{rec} of the input current and/or of a related mains current $i_N \simeq i^*_{rec}$, only the space vectors lying in immediate neighbourhood of i^*_{rec} are incorporated into the switching state sequence in order to achieve a deviation as small as possible between reference and actual space vectors (Fig. 3). In general, the switching states valid within one pulse (half) period have to be arranged in such a manner that a minimum number of switching transitions of the power transistors and/or minimum switching losses do occur. Different possibilities for arranging the switching states within one pulse period are presented in Section 3.

2.3 Active boost output stage

For symmetric mains, the buck-stage modulation index M has been defined in [6] as

$$M = \frac{\hat{I}_N}{I} = \frac{\sqrt{2}}{\sqrt{3}} \cdot \frac{U}{U_{N,ll}}, \quad M \in (0;\ 1) \tag{5}$$

where $\hat{I}_N$ is the peak value of the mains phase currents, I the DC link current, U the global average value of the buck stage output voltage and $U_{N,ll}$ the rms value of the mains line-to-line voltages. To decide whether the boost ouput stage has to be activated or not, the maximum local average value $\bar{u}_{max}$ of the buck-stage output voltage is used. This formal value can be calculated via

$$\bar{u}_{max} = \frac{\sqrt{3}}{\sqrt{2}} \cdot M_{max} \cdot \sqrt{u^2_{C_1,R} + u^2_{C_1,S} + u^2_{C_1,T}} \tag{6}$$

where M_{max} is the maximum modulation index of the buck input stage [18]. For output voltages $U_0 < \bar{u}_{max}$, the buck input stage operates at a modulation index $M < M_{max}$ and the boost output stage is not active, that is, the duty cycle δ of the boost output stage is $\delta = 0$. To achieve an output voltage $U_0 > \bar{u}_{max}$, the boost stage has to be activated ($\delta > 0$, Section 7). The duty cycle δ of the boost IGBT has to be set according to

$$\delta = 1 - \frac{\bar{u}_{max}}{U_0} \quad \delta \in (0;\ 1) \tag{7}$$

3 Modulation methods

One possibility for arranging the switching states is to place the active switching states at the beginning and the free-wheeling state at the end of one pulse half-period. In the subsequent pulse half-period, the switching states are arranged in reverse order, that is, symmetrical to the middle of the pulse period; cf. method 1 in Fig. 4*a*. There, the voltage u switched to

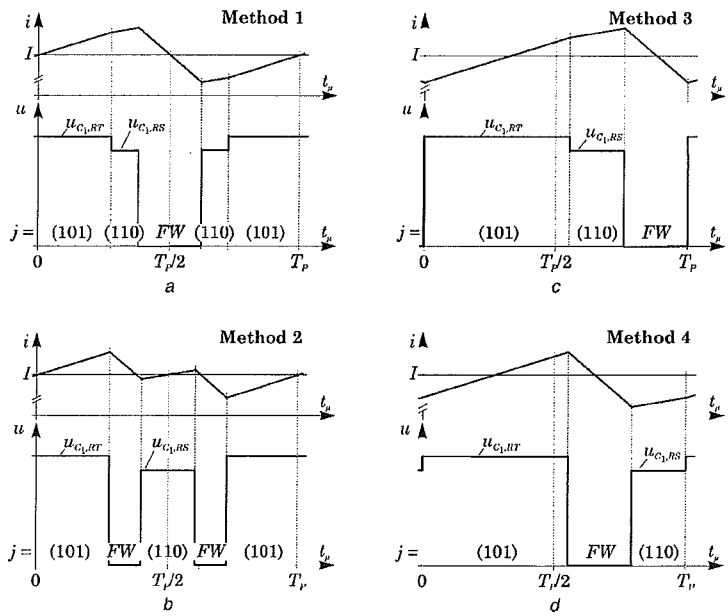

Figure 4 *DC link current I, global average value I, voltage U across the buck-stage free-wheeling diode and related switching states j for different modulation methods*

a and *b* Symmetric methods (triangular carrier signal) *c* and *d* Asymmetric methods (sawtooth carrier signal)
Valid for $\varphi_{rec} \in (0;\ \pi/6)$

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the output of the buck stage (forward voltage drops of the power semiconductors are neglected) and the resulting DC link current i (together with its global average value I) are shown together with the switching states j. Another possibility for a symmetric switching state sequence is to place the free-wheeling state between the two active switching states; cf. method 2 in Fig. 4*b*, whereby probably a reduction in the ripple components of the input filter capacitor voltages and/or the DC link inductor current can be achieved. Both methods 1 and 2 are symmetrical sequences, which can be realised by intersecting proper phase reference signals with a triangular carrier signal with pulse frequency f_p. Alternatively, asymmetrical sequences can be realised by employing a sawtooth carrier signal with pulse frequency f_p, and the resulting modulation methods 3 and 4 are depicted in Figs. 4*c* and 4*d*.

In this paper, the asymmetrical sequences will not be analysed because of the following reasons.

- There is no improvement regarding switching losses, that is, the switching losses for methods 3 and 4 are the same as for method 1 for the same pulse frequency f_p (Section 4).

- There is no significant reduction in the DC link inductor current ripple and input filter capacitor voltage ripple if the pulse frequency f_p is the same. In [19], it has been shown that the harmonic spectrum of the input currents for sawtooth and triangular reference signals is nearly identical. Although the shape and the amplitudes of the ripple waveform envelopes slightly differ over the modulation range, this result is true for all ripple values.

- At the beginning of each pulse half-period ($t = 0$, $T_P/2$, T_P,...) all ripple values are exactly equal to zero for symmetrical sequences (Figs. 4*a* and 4*b*), that is, a ripple-free value of the DC link current and the filter capacitor voltages can be sampled at these time instants [20]. This reduces the filtering effort of the control quantities noticeably and is therefore an important advantage when compared with asymmetrical sequences, where there is no defined ripple-free time instant.

- Furthermore, several signal processor PWM outputs do not support asymmetrical sequences.

Hence, in this paper, only the symmetrical sequences (methods 1 and 2) will be analysed and compared.

Both modulation methods 1 and 2 presented here do not show a difference regarding the number of switching transitions, if those occurring at zero voltage/current are neglected. However, as shown in the following section, both switching state sequences result in different switching losses.

The conduction losses of the power semiconductors show practically the same values for the different modulation methods, since they are mainly dependant on the on-times of the power switches being defined by the input current reference value and the DC link current (Section 2). However, the DC link inductor current ripple Δi has different time behaviours for both modulation methods (Section 6), which causes a slightly different rms value of the currents in the IGBTs and diodes of the rectifier. This consequently influences the conduction losses of the power semiconductors, for example, the IGBTs according to

$$P_{\mathrm{Cond},S} = U_{CE0} \cdot I_{S,\mathrm{avg}} + r_{CE} \cdot I_{S,\mathrm{rms}}^2 \tag{8}$$

If the current ripple Δi originating from the DC link inductor is neglected, according to [21] the transistor rms current is given by

$$I_{S,\mathrm{rms}}^2 = \frac{2M}{\pi} \cdot I^2 \tag{9}$$

considering a current ripple Δi would result in

$$I_{S,\mathrm{rms}}^2 = \frac{2M}{\pi} \cdot \left(I^2 + \frac{\Delta i^2}{3}\right) \tag{10}$$

under the assumption of a linear increase in the inductor current during the transistor turn-on period. Therefore the influence of the current ripple on $I_{S,\mathrm{rms}}^2$ is given by $\Delta i^2/3I^2$. Typically, a DC link inductor is selected in order to allow a maximum ripple of $\pm 20\%$, that is, $\Delta i = 0.2I$, in order to maintain continuous conduction mode (CCM) operation also for light load operation. With (10), this results in a transistor current rms value of $I_{S,\mathrm{rms}}^2 = 1.013I^2 \cdot 2M/\pi$, hence an influence of only 1.3% of the current ripple when compared with (9). Taking into account also the forward voltage drop of the IGBT in (8), the influence of the current ripple on the total conduction losses is typically significantly lower than 1%. Consequently, the conduction losses do not have to be considered for a comparative study of the modulation methods.

4 Switching losses

For the sake of simplicity, we assume: (i) the switching energy loss w to be proportional to the switched voltage $u(t)$ (the proportional relationship is represented by a constant of proportionality k) and (ii) a constant switched current I (as impressed by the DC link inductor L).

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The average value of the global switching energy loss (related to a mains period T_N) can then be calculated from the sum of the local switching energy losses $w(t)$ (related to a pulse period T_P) of all IGBTs S_i incorporated into the switching actions via

$$W = \frac{1}{T_N}\int_0^{T_N} \sum_i w_{S_i}(t)\mathrm{d}t \tag{11}$$

Investigating, for example, sequence 1 in Fig. 4*a*, we have: at the transition from switching state $j = (101)$ to $j = (110)$, power transistor S_S has to be turned on (in order to be available for current conduction during the subsequent switching state) at zero current/voltage for a short overlapping time t_d [22]; subsequently, power transistor S_T has to be turned off at a voltage u_{C_1,S_T}. At the following transition $j = (110) \rightarrow j = (100)$, power transistor S_S has to be turned off at a voltage u_{C_1,R_S}. In the subsequent pulse half-period, power transistors S_S and S_T have to be switched on (or off) again at the same voltages, but in reverse order. The calculation of the average value of the global switching power loss P within one mains period can be constrained to an interval $\varphi_{\mathrm{rec}} \in (0; \pi/6)$; because of the symmetry of the feeding AC mains and the rectifier topology, one has

$$\begin{aligned} P &= Wf_{\mathrm{p}} \\ &= \frac{1}{\pi/6}\int_0^{\pi/6} kf_{\mathrm{p}} I(u_{C_1,S_T}(t) + u_{C_1,R_S}(t))(\varphi_{\mathrm{rec}})\,\mathrm{d}\varphi_{\mathrm{rec}} \\ &= \frac{1}{\pi/6}\int_0^{\pi/6} kf_{\mathrm{p}} I u_{C_1,R_T}(\varphi_{\mathrm{rec}})\,\mathrm{d}\varphi_{\mathrm{rec}} = \frac{3\sqrt{3}}{\pi} kf_{\mathrm{p}} I\hat{U}_N \end{aligned} \tag{12}$$

with $k = k_{\mathrm{on}} + k_{\mathrm{off}}$. The switching power losses for switching sequence 2 can be calculated in an analogue manner, the result is given in Table 1. One can see immediately that the modulation method with the free-wheeling state lying at the beginning and/or at the end of one pulse half-period, respectively, is advantageous over sequence 2 by a factor of $\sqrt{3}$ regarding switching losses.

Since the modulation method takes influence not only on the switching losses but also on the ripple components on AC and DC sides, this does provide another basis to optimise the modulation methods. In the following sections, the time behaviour and the rms value of the input filter capacitor voltage ripple and of the DC link current ripple are investigated.

Table 1 Average value of the switching power losses for the switching states sequences given in Figs. 4*a* and 4*b*

Sequence	$P/(f_{\mathrm{p}}\, k\, I\, \hat{U}_N)$
1	$3\sqrt{3}/\pi$
2	$9/\pi$

5 Ripple of the input filter capacitor voltage

In this section, the voltage ripple across the input filter capacitors $C_{1,i}$ is investigated, which is relevant for the dimensioning of the input filter capacitors concerning their voltage stress.

5.1 Analytically closed calculation

As a quality functional, the integral (related to a mains period) of the square of the deviation between the input capacitor voltage actual and reference value $\Delta\underline{u}_{C_1} = \underline{u}_{C_1} - \underline{u}^*_{C_1}$ (or the rms value of the input filter capacitor voltage, respectively) is selected [23]

$$Q = \Delta U^2_{C_1,RST,\mathrm{rms}} = \frac{1}{T_N}\int_{T_N} \Delta u^2_{C_1,RST,\mathrm{rms}}(t)\,\mathrm{d}t \tag{13}$$

To calculate the quality functional Q, one can choose a simple equivalent circuit of the system (Fig. 5), and the space vector of the input filter capacitor voltage ripple $\Delta\underline{u}_{C_1}$ can be calculated via

$$\frac{\mathrm{d}\Delta\underline{u}_{C_1}}{\mathrm{d}t} = \frac{1}{C_1}(\underline{i}_{\mathrm{rec}} - \underline{i}^*_{\mathrm{rec}}) \tag{14}$$

Incorporating the neighbouring current space vectors with proper on-time δ_j in the formation of the input current reference value (Fig. 3), one has

$$\underline{i}^*_{\mathrm{rec}} = \underline{i}_{\mathrm{rec},(110)}\delta_{(110)} + \underline{i}_{\mathrm{rec},(101)}\delta_{(101)} \tag{15}$$

with

$$\begin{aligned} \delta_{(101)} &= M\sin\left(\frac{\pi}{3} + \varphi_{\mathrm{rec}}\right) \\ \delta_{(110)} &= M\sin\left(\frac{\pi}{3} - \varphi_{\mathrm{rec}}\right) \\ \delta_{FW} &= 1 - \delta_{(101)} - \delta_{(110)} \end{aligned} \tag{16}$$

With this, the local rms value [related to a pulse (half)

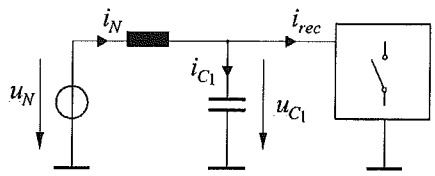

Figure 5 *Space vector equivalent circuit of the system AC side*

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period] of the input capacitor voltage ripple can be calculated via [23]

$$\Delta u^2_{C_1,RST,\mathrm{rms}}(t) = \frac{2}{T_P}\int_{t_\mu=0}^{t_\mu=(1/2)T_P} (\Delta u^2_{C_1,R}(t_\mu) + \Delta u^2_{C_1,S}(t_\mu) + \Delta u^2_{C_1,T}(t_\mu))\,\mathrm{d}t_\mu = \frac{2}{T_P}\int_{t_\mu=0}^{t_\mu=(1/2)T_P} \frac{3}{2}|\Delta \underline{u}_{C_1}|^2\,\mathrm{d}t_\mu \quad (17)$$

To calculate the global rms value (being set equal to the quality functional Q) related to a mains period we have with sufficiently good approximation for high pulse frequency

$$Q = \Delta U^2_{C_1,RST,\mathrm{rms}} = \frac{1}{T_N}\int_{T_N}\frac{2}{T_P}\int_{t_\mu=0}^{t_\mu=(1/2)T_P}\frac{3}{2}|\Delta \underline{u}_{C_1}|^2\,\mathrm{d}t_\mu\,\mathrm{d}t = \frac{1}{T_N}\int_{T_N}\Delta u^2_{C_1,RST,\mathrm{rms}}(t)\,\mathrm{d}t \quad (18)$$

which allows a simple analytically closed calculation of the rms value of input filter capacitor voltage ripple.

5.2 Trajectory of the voltage space vector

In the following, for one characteristic input current space vector i^*_{rec}, the trajectories of the space vector of the input filter capacitor voltage ripple $\Delta \underline{u}_{C_1}(t_\mu)$ are given for the two switching state sequences according to Figs. 4*a* and 4*b*.

5.2.1 Modulation method 1: For the voltage space vectors $\Delta \underline{u}_{C_1,t_{\mu i}}$ depending on the global time t one receives for sequence 1

$$\Delta \underline{u}_{C_1,t_{\mu_1}}(t) = \delta_{(101)}[\underline{i}_{\mathrm{rec},(101)} - \underline{i}^*_{\mathrm{rec}}(t)]\frac{T_P}{2C_1}$$

$$\Delta \underline{u}_{C_1,t_{\mu_2}}(t) = \delta_{(110)}[\underline{i}_{\mathrm{rec},(110)} - \underline{i}^*_{\mathrm{rec}}(t)]\frac{T_P}{2C_1} + \Delta \underline{u}_{C_1,t_{\mu_1}}(t) \quad (19)$$

or, respectively, with (14), (15) and Fig. 3

$$\frac{1}{u_n}\Delta \underline{u}_{C_1,t_{\mu_1}} = \Delta u_{C_1,t_{\mu_1},\alpha} + j\Delta u_{C_1,t_{\mu_1},\beta} = \delta_{(101)}[\sqrt{3}\delta_{\mathrm{FW}} + j(1-\delta_{(101)}+\delta_{(110)})] \quad (20)$$

$$\frac{1}{u_n}\Delta \underline{u}_{C_1,t_{\mu_2}} = \Delta u_{C_1,t_{\mu_2},\alpha} + j\Delta u_{C_1,t_{\mu_2},\beta} = \delta_{\mathrm{FW}}[\sqrt{3}(\delta_{(101)}+\delta_{(110)}) + j(\delta_{(101)}-\delta_{(110)})] \quad (21)$$

with the normalisation basis

$$u_n = \frac{I}{2\sqrt{3}C_1 f_{p1}} \quad (22)$$

In Fig. 6*a* the trajectory of the space vector of the input capacitor voltage ripple $\Delta \underline{u}_{C_1}(t_\mu)$ is shown with reference to a current reference value i^*_{rec} as given in Fig. 3 for modulation method 1.

5.2.2 Modulation method 2: For sequence 2, one obtains for the voltage space vectors $\Delta \underline{u}_{C_1,t_{\mu i}}$ depending on the global time t

$$\Delta \underline{u}_{C_1,t_{\mu_1}}(t) = \delta_{(101)}[\underline{i}_{\mathrm{rec},(101)} - \underline{i}^*_{\mathrm{rec}}(t)]\frac{T_P}{2C_1}$$

$$\Delta \underline{u}_{C_1,t_{\mu_2}}(t) = (1-\delta_{(101)}-\delta_{(110)})[-\underline{i}^*_{\mathrm{rec}}(t)] \times \frac{T_P}{2C_1} + \Delta \underline{u}_{C_1,t_{\mu_1}}(t) \quad (23)$$

or, respectively

$$\frac{1}{u_n}\Delta \underline{u}_{C_1,t_{\mu_1}} = \Delta u_{C_1,t_{\mu_1},\alpha} + j\Delta u_{C_1,t_{\mu_1},\beta} = \delta_{(101)}[\sqrt{3}\delta_{\mathrm{FW}} + j(1-\delta_{(101)}+\delta_{(110)})] \quad (24)$$

$$\frac{1}{u_n}\Delta \underline{u}_{C_1,t_{\mu_2}} = \Delta u_{C_1,t_{\mu_2},\alpha} + j\Delta u_{C_1,t_{\mu_2},\beta} = \delta_{(110)}[-\sqrt{3}\delta_{\mathrm{FW}} + j(1+\delta_{(101)}-\delta_{(110)})] \quad (25)$$

In Fig. 6*b*, the trajectory is depicted for modulation method 2 showing the same shape but a different position when compared with the trajectory of

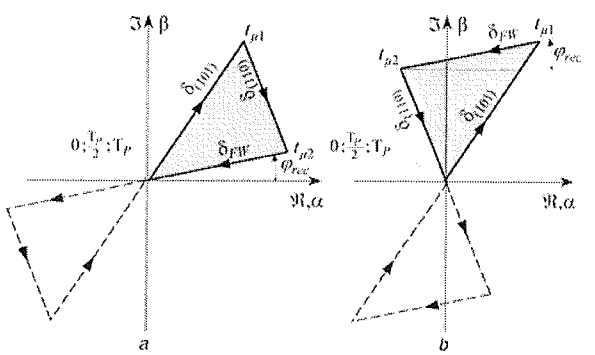

Figure 6 *Trajectory of the space vector $\Delta \underline{u}_{C_1}(t_\mu)$ within one pulse period*

a Modulation method 1
b Modulation method 2

modulation method 1, which results in different time behaviours of the input filter capacitor voltage ripple.

5.3 RMS value of the input filter capacitor voltage ripple

In the following, the rms value of the input voltage ripple for the two modulation schemes according to Figs. 4*a* and *b* is calculated via (18). To denote the results, the numbers of the switching states sequences are given as indices, for example, index 1 for modulation method 1

$$\Delta U^2_{C_1,RST,\mathrm{rms},1} = \frac{M^2}{32\pi}(9M^2(4\pi+\sqrt{3}) - 8M(15\sqrt{3}+8)+48\pi)\cdot u_n^2 \quad (26)$$

$$\Delta U^2_{C_1,RST,\mathrm{rms},2} = \frac{M^2}{32\pi}(9M^2(4\pi-3\sqrt{3}) - 160M+72(\pi-\sqrt{3}))\cdot u_n^2\cdot\left(\frac{f_{p1}}{f_{p2}}\right)^2 \quad (27)$$

In the sense of making a fair comparison of the different modulation schemes, the pulse frequency f_P has to be adjusted in such a manner that the average value of the switching power losses (Section 4) related to a mains period is the same for both modulation methods [16, 17]. According to Table 1, one has to reduce the pulse frequency for modulation method 2 by a factor of $\sqrt{3}$ in order to achieve the same switching power loss when compared with modulation method 1, $f_{p2} = f_{p1}/\sqrt{3}$. The corrected rms values of the input filter capacitor voltage ripple depending on the modulation index M of the buck rectifier are given in Fig. 7. With this, the value of the input filter capacitor can be selected as being necessary for obtaining a given (maximum) rms value of the input voltage ripple.

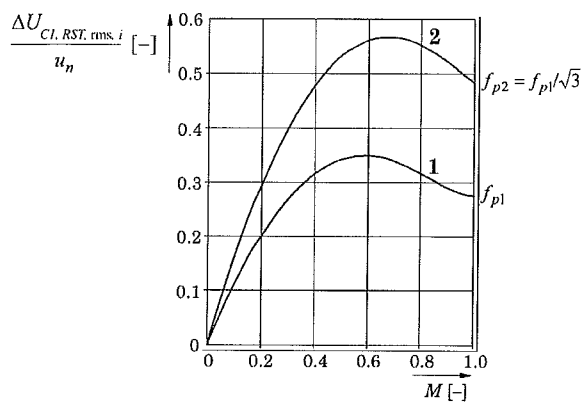

Figure 7 *Normalised rms value of the input capacitor voltage ripple $\Delta U_{C_1,RST,\mathrm{rms},i}/u_n$ depending on the modulation index M for modulation methods 1 and 2 for equal switching losses*

5.4 Time behaviour and envelope of the input filter capacitor voltage ripple

The knowledge about the time behaviour and the envelope of the input filter capacitor voltage ripple is useful in connection with the dimensioning of the input filter, because the rms value $\Delta U_{C_1,RST,\mathrm{rms}}$ only provides an integral information about the ripple voltage time behaviour. In Fig. 8, the envelopes of the input filter capacitor voltage ripple in phase R within an angle interval $\varphi_{\mathrm{rec}} \in (0;\ \pi/2)$ (For the angle interval $\varphi_{\mathrm{rec}} \in (\pi/2;\ \pi)$, the envelopes are mirrored at $\varphi_{\mathrm{rec}} = \pi/2$.) are given for both modulation methods 1 and 2 for the following operating points

buck operating point: $P_0 = 5$ kW, $U_{N,ll} = 400$ V, $U_0 = 400$ V, $M = 0.82$, $\delta = 0$

buck+boost operating point: $P_0 = 5$ kW, $U_{N,ll} = 230$ V, $U_0 = 400$ V, $M = 0.90$, $\delta = 0.37$

and for the following operating parameters: $f_N = 50$ Hz, $C_1 = 8.2$ μF, $L_1 = 240$ μH, $L = 2 \times 1$ mH, $f_{p1} = 28$ kHz and $f_{p2} = 16.2$ kHz.

Remark: The time behaviour of the input filter capacitor voltage ripple is shown in Section 7 together with experimental results.

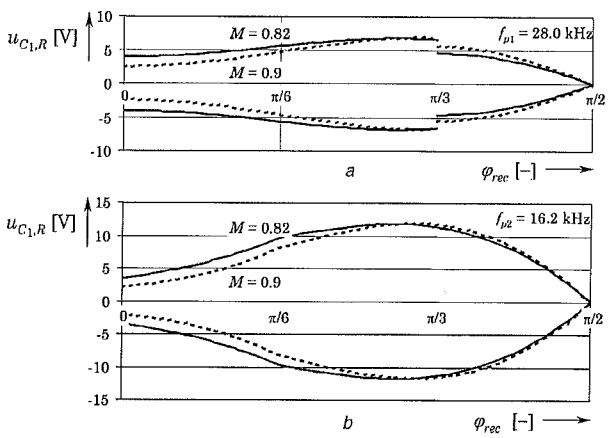

Figure 8 *Envelopes of the input filter capacitor voltage ripple*

a $\Delta u_{C_1,R}$ in phase R for different modulation indices M = 0.82 and M = 0.9 for modulation methods
a Method 1
b Method 2

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The comparison of the results clearly shows that modulations method 1 is advantageous over modulation method 2 concerning the rms value of the ripple component, as well as concerning the envelope and/or the time behaviour of the voltage ripple.

6 Ripple of the DC link current

For dimensioning the DC link inductor, the time behaviour of the DC link current ripple is of interest, since the ripple component should be limited to a maximum value, for example, $\Delta i_{max} = \pm 0.2I$. This value defines the value of the load at which a transition between continuous DC link current (CCM) to discontinuous DC link current [discontinuous conduction mode (DCM)] occurs. The voltage u_L across the DC link inductor, and hence the DC link current ripple, is influenced by the selected modulation method, and furthermore, the modulation of the boost output stage takes influence on the voltage u_L, which is analysed in the following section.

6.1 Modulation of the boost output stage

If the boost stage has to be activated, that is, if $\delta > 0$ is valid (Section 2.3), there are different possibilities of placing the switching function of the boost IGBT within the pulse period, what takes influence on the voltage applied to the DC link inductor and hence on the DC link current ripple. The boost power transistor can be activated either during the free-wheeling state of the buck input stage (modulation method 1.1) or during the active state of the buck stage (modulation method 1.2). This effect is clearly shown in Figs. 9*b* and 9*c*: turning the boost IGBT on during the active switching states of the buck stage results in a significantly higher current ripple of the DC link current when compared that in Fig. 9*c*, where the boost IGBT is turned on while the buck input stage is operating in the free-wheeling state.

Therefore the time behaviour of the ripple of the DC link inductor current is strongly dependant on the coordination of the modulation of the buck and of the boost stages. The ripple time behaviour and the ripple rms value are calculated analytically in the following section.

6.2 Analytically closed calculation of the DC link inductor current ripple

The current in the DC link inductor is determined by the voltage u at the output of the buck stage and by the voltage across the boost power transistor u' (which equals the system output voltage U_0 for

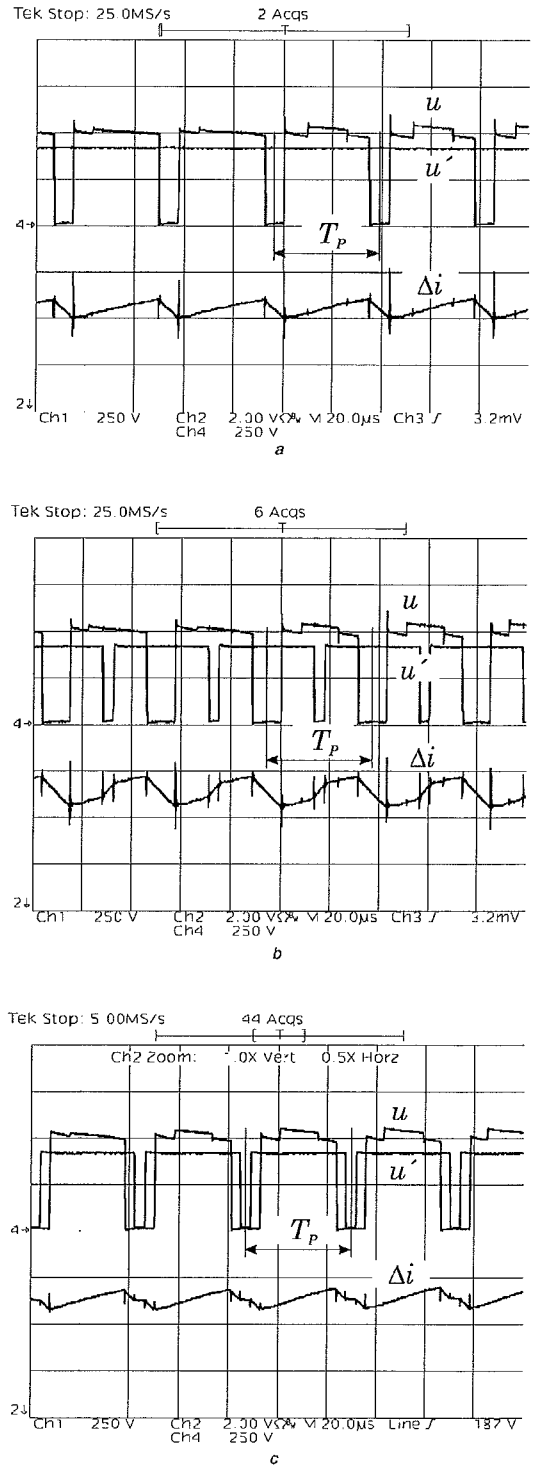

Figure 9 *Buck-stage output voltage U, voltage u′ across the boost IGBT and DC link inductor current ripple*

Scales: *u*, *u′*: 250 V/div; Δ*i*: 2 A/div, t_μ: 20 µs/div
Δ*i for* $P_0 = 2.5$ *kW at* $U_{N,ll} = 440$ *V.*
a Operation for disabled boost stage, $\delta = 0$, modulation method 1
b Boost operating during active state of buck stage, modulation method 1.2
c Boost operating during free-wheeling state of buck stage, modulation method 1.1

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disabled boost stage). One obtains for the current ripple in the DC link inductor

$$\Delta i(t_{\mu,2}) = \frac{1}{L}\int_{t_{\mu,1}}^{t_{\mu,2}} [u(t_\mu) - u'(t_\mu)],\, \mathrm{d}t_\mu + \Delta i(t_{\mu,1}) \tag{28}$$

The local rms value of the current ripple in depending on the position φ_{rec} of the pulse interval considered within the mains period can be calculated via

$$\begin{aligned}\Delta i^2_{\mathrm{rms}}(\varphi_{\mathrm{rec}}) &= \frac{1}{T_{\mathrm{P}}/2}\int_{t_\mu=0}^{t_\mu=(1/2)T_{\mathrm{P}}} [\Delta i(t_\mu)]^2\,\mathrm{d}t_\mu \\ &= \frac{2}{3T_{\mathrm{P}}}\Big[t_{\mu,1}(\Delta i_0^2 + \Delta i_0 \Delta i_{t_{\mu,1}} + \Delta i^2_{t_{\mu,1}}) \\ &\quad + (t_{\mu,2} - t_{\mu,1})(\Delta i^2_{t_{\mu,1}} + \Delta i_{t_{\mu,1}}\Delta i_{t_{\mu,2}} + \Delta i^2_{t_{\mu,2}}) \\ &\quad + \left(\frac{T_{\mathrm{P}}}{2} - t_{\mu,2}\right)(\Delta i^2_{t_{\mu,2}} + \Delta i_{t_{\mu,2}}\Delta i_{T_{\mathrm{P}}/2} + \Delta i^2_{T_{\mathrm{P}}/2})\Big]\end{aligned} \tag{29}$$

The global rms value of the DC link current ripple within the mains period can be calculated by summation of the local rms values within one pulse half-period; however, if the pulse frequency is substantially larger than the mains frequency (which is fulfilled in the case at hand), the summation can be replaced by an integration with sufficiently good approximation

$$\Delta I^2_{\mathrm{rms}} = \frac{1}{2\pi}\int_0^{2\pi} [\Delta i_{\mathrm{rms}}(\varphi_{\mathrm{rec}})]^2 \mathrm{d}\varphi_{\mathrm{rec}} \tag{30}$$

which allows an analytically closed calculation of the global rms value of the DC link current ripple.

For examples, consider modulation method 1 for deactivated boost stage (Fig. 9*a*), one obtains for the DC link inductor current ripple at the time instants $t_{\mu,i}$ within one pulse half-period for a mains interval $u_{C_1,R} > 0 > u_{C_1,S} > u_{C_1,T}$

$$\begin{aligned}\Delta i_0 &= 0 \\ \Delta i_{t_{\mu,1}} &= \frac{1}{L}(u_{(101)} - U_0)\delta_{101}\frac{T_{\mathrm{P}}}{2} \\ \Delta i_{t_{\mu,2}} &= \frac{1}{L}(u_{(110)} - U_0)\delta_{110}\frac{T_P}{2} + \Delta i(t_{\mu,1}) \\ \Delta i_{T_P/2} &= 0\end{aligned} \tag{31}$$

The global rms value of the DC link current ripple within one mains period can now be calculated incorporating the relative on-times δ_j and the output voltages u_j (where u_j is the line-to-line voltage switched to the output of the buck stage during switching state j), as well as (29) and (30). There the integration (30) can be limited to a $\pi/6$-wide mains interval and yields

$$\Delta I_{\mathrm{rms},1} = \frac{1}{8\sqrt{5\pi}} \sqrt{240\pi - M(600\sqrt{3} + 352) + M^2(45\sqrt{3} + 180\pi)} \cdot i_n \tag{32}$$

with the normalisation basis

$$i_n = \frac{U_0}{3Lf_{\mathrm{p1}}} \tag{33}$$

For modulation method 2, one obtains for the global rms value of the DC link current ripple

$$\Delta I_{\mathrm{rms},2} = \frac{1}{8\sqrt{5\pi}} \sqrt{180\pi - 90\sqrt{3} - 736M + M^2(180\pi - 135\sqrt{3})} \cdot i_n \cdot \frac{f_{\mathrm{p1}}}{f_{\mathrm{p2}}} \tag{34}$$

considering the adjusted pulse frequency $f_{P2} = f_{P1}/\sqrt{3}$ for equal switching losses. In Fig. 10, the results of the analytical calculations are compiled and compared with simulation results using CASPOC© [24], where an excellent conformity is given. Therefore the very complex results of an analytical calculation of the global ripple current rms value for active boost output stage ($\delta > 0$) are omitted here for the sake of brevity. To determine the rms value of the DC link current ripple for this case, we refer to simulation results given in Fig. 11. There, for modulation method 1, boost operating during the free-wheeling state

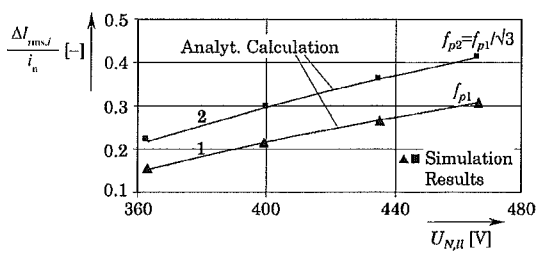

Figure 10 *Comparison of the results of simulation and analytical calculation of the normalised rms value of the DC link current ripple $\Delta I_{rms,i}/i_n$ for modulation methods 1 and 2 in case of deactivated boost output stage ($\delta = 0$)*

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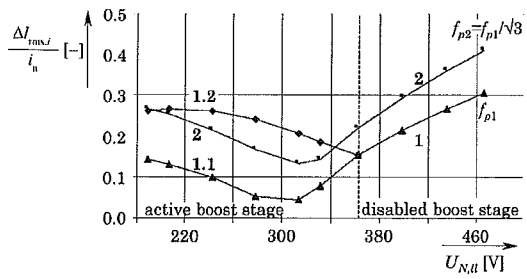

Figure 11 *Simulation results of the normalised rms value of the DC link current ripple $\Delta I_{rms,i}/i_n$ for different modulation methods within a wide input voltage range*

[modulation method 1.1; Fig. 9*c*] and that during the active state (modulation method 1.2; Fig. 9*b*) are compared.

Incorporating (28), one can derive the local time behaviour of the current ripple in the buck + boost inductor and its envelope for the different modulation methods; Fig. 12 shows the envelopes $\Delta i_{\max,i}$ for the buck operating point specified in Section 5.4 within a $\pi/3$-wide mains interval. One can see immediately that modulation method 1 does provide a lower DC link current ripple in almost the whole mains interval.

The minimum load at which a transition between CCM and DCM occurs can be easily derived employing Fig. 12: in order to ensure CCM, the average value of the DC link inductor current I has to remain above the maximum amplitude of the current ripple $\Delta i_{\max,i}$ occurring within one mains period. In case of boost converter operation ($\delta > 0$), the current ripple does decrease for modulation methods 1.1 and 2; hence DCM will not occur at the lower input voltage range for the same load condition [15].

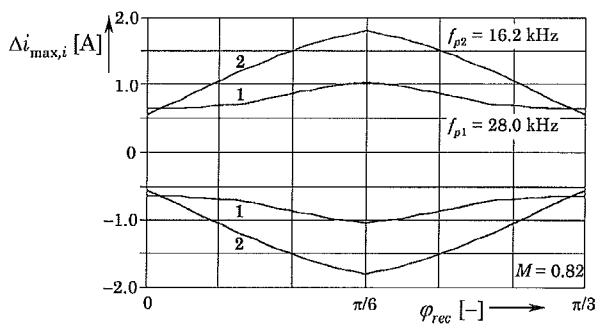

Figure 12 *Envelopes $\Delta i_{max,i}$ of the local DC link inductor current ripple Δi_i for modulation methods 1 and 2 for a modulation index $M = 0.82$ within a $\pi/3$-wide mains interval (pulse frequencies f_{p1} and f_{p2} are set according to equal switching losses Boost stage is not active, $\delta = 0$)*

7 Conclusions

In this paper different modulation methods of a three-phase buck + boost unity power factor PWM rectifier are investigated concerning switching losses, time behavior as well as concerning rms values of the input filter capacitor voltages and the DC link inductor current ripple. The modulation methods do differ concerning the arrangement of active and passive switching states of the buck input stage and the coordination of the switching of the buck input stage and the boost output stage within a pulse interval.

The comparisons show that there exists one modulation method which does provide simultaneously:

- minimum switching losses and/or maximum pulse frequency,
- a minimum input filter capacitor voltage ripple and
- a minimum DC link current ripple.

This optimum modulation method is characterised by the free-wheeling state of the buck input stage being placed at the beginning/at the end of one pulse half period, and by a turn-on interval of the boost stage power transistor being centered in the free-wheeling interval of the buck stage (modulation method 1.1).

The optimum modulation scheme can be further improved preventing sliding intersection of the input filter capacitor voltages by simply adding an overlapping time when switching over between two active switching states, whereby no distortion of the mains currents at sector boundaries occurs [22].

Modulation scheme 1 can also be applied advantageously in case of a parallel connection of two buck input stages. There it is advantageous to keep the power transistor of that phase showing the lowest absolute value of the phase voltage during the free-wheeling state in the on-state to have a possibility for active symmetrisation of the DC link currents. Moreover, interleaving is advantageously applied for further reduction of ripple components [25].

Experimental results on a 5 kW hardware prototype verifying the correctness of the theoretical considerations are carried out in a subsequent paper in [26].

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