Proceedings

The Third International Conference on Sensor Technologies and Applications

SENSORCOMM 2009

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An ultra low power Wakeup Receiver for Wireless Sensor Nodes

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Abstract

An ultra-low power 2.4 GHz RF Wakeup Receiver is designed for wireless sensor networks nodes. The receiver demodulates On-Off Keying at 100 kbps. A 120 nm CMOS chip includes the analog front-end and consumes only 7.5 µW from a single 1.5 V supply. The digital signal processing is implemented in an FPGA. The results of measures and simulations are evaluated for the use of this receiver in wireless sensor networks.

Keywords*: Wakeup Receiver, OOK, ultra low power, Wireless Sensor Networks*

1. Introduction

Nearly 75% [[1]] of the total power consumed from a typical WSN node is attributed to the radio transceiver. One main cause is the receiver which has to be turned on frequently in order to listen to possible incoming messages and to avoid high latency communication. The channel is sampled using intelligent strategies in the MAC layer such as described in [[1]] or [[3]] in order to synchronize communications and optimize power consumption. By using these strategies, very low power consumption is only achieved at cost of data throughput and latency, because communication occurs only during small time windows at low periods (e.g. once per second). In such situations packets have a worst case end-to-end delay equivalent ideally to the period of the cycle multiplied by number of hops.

The main task of this work was to realize a lower performance but very efficient receiver (called Wakeup Receiver or WUR) that consumes as little power as possible (the goal is 10 µW), so that it can be always active, detecting incoming wakeup messages (a few bytes) without compromising the lifetime of the node which can be of some years. The WUR acts as a remote control to activate the main transceiver for data communication. The biggest advantage of a WUR is that no synchronization between nodes is required for the communication, simplifying the MAC strategy and lowering the end-to-end delay of packets. Integrated Wakeup Receiver front-end designs have only been published by the Berkeley wireless research group [[4], [5]]. To a minor extent a concept can also be found in [[7]].

The work presented in [[4]] has a slightly different architecture: the RF signal is amplified by 10 dB (requiring 48 µW), the output is fed to the envelope detector that is sampled from a 6 bit ADC (requiring 13.8 µW). The additional energy needed from the digital baseband is not estimated at all.

The architecture of [[5]] differentiates from this work by mixing the RF signal to a lower frequency by the means of an imprecise local oscillator. The down-mixed signal is then fed to the envelope detector that has looser requirements, because the operating frequency is much lower. This results in higher sensitivity (-72 dBm) because of mixing gain, although 28 µW are needed from the oscillator and mixer.

This work is divided in four sections. Section two explains the architecture of the wakeup receiver in its details. Section three presents the results of measures and simulations of this work. Section four gives an outlook on the work and presents its future developments.

2. Receiver architecture

In order to reach the goal of <10 µW in power consumption of the receiver, one has to simplify the design and to get rid of the power hungry components of typical radio receivers (like the superheterodyne receiver), such as the mixer or the low noise amplifiers that are found on the RF signal path. On-Off Keying (OOK) modulation is chosen because it allows

simplification of the RF demodulation and also because the short wakeup message with low bit count does not require highly precise synchronization. Together with a forward error correction (FEC) based correlation receiver, a better robustness of the wakeup link can be achieved with minimum power overhead.

The proposed block diagram of the WUR is shown in Fig. 1. The external matching builds a filter for the desired RF band as found in common receiver designs. The analog front-end (realized on-chip) converts the 2.4 GHz RF input signal into baseband signals, which are decoded by the correlation receiver realized on an FPGA.

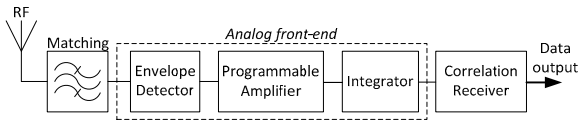

Fig. 1. WUR block diagram

2.1. Analog front-end

The front-end converts the OOK signal directly to baseband from the 50 Ω input eliminating the need of oscillators and PLLs using a simple envelope detector. This technique is also exploited in RFID tags and needs little other blocks to demodulate the incoming signal. Fig. 2 shows the schematic of the envelope detector as also described in [[6]] and [[8]].

The envelope detector is realized in two versions: on-chip with a MOS detector and off-chip with Schottky diodes and completely passive. Unfortunately, on-chip shottky diodes are not available in the given technology. Envelope detectors have the disadvantage that their exponential and quadratic nonlinearity means at least a factor two drop in efficiency that is a drop of 20 dB in the demodulated amplitude for each drop of 10 dB in the input RF amplitude.

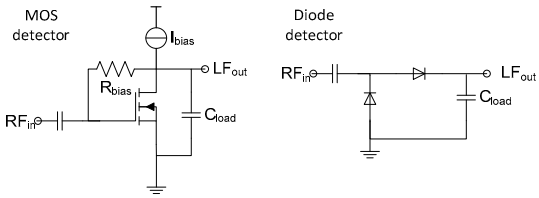

Fig. 2. MOS and Schottky envelope detectors

This limits particularly the sensitivity of the detector and of the overall receiver. This behavior can be seen in Fig. 3, which shows measured values of the output amplitude versus input amplitude modulating the 100% AM RF carrier. The chart shows little difference between MOS and Schottky, because the external matching was trimmed to give equivalent results between the detectors. The 1:1 curve shows the ideal efficiency of the envelope detector. For a given matching, the MOS detector performs worse because the quadratic nonlinearity is lower than the exponential nonlinearity of the diode.

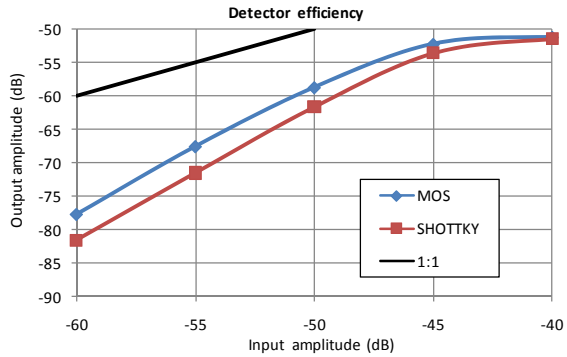

Fig. 3. Detector efficiency

In a second stage, the signal produced from the envelope detector is amplified with programmable gain (54 dB maximum gain) and variable bandwidth (0.1-10 KHz to 1 MHz). A programmable integrator is needed to reduce noise of the system adding only 1.5 µW in power consumption. The output of the integrator is then level shifted and processed from the correlation receiver.

2.2. Correlation receiver

For reasons of flexibility in implementation, the decoding of the signal in the digital domain is realized in an FPGA and will be realized on-chip in a future version. The first stage of the decoder is a state machine correlating the output of the integrator to one symbol and taking a decision on the value of the bit. The second stage decodes the bits if a synchronization sequence is detected. The decoded bit sequence is then used to extract data for the upper communication layers. Extensive use of Forward Error Correction (FEC) is done to lower the required Signal to Noise Ratio (SNR) at the input of the correlation receiver. The block diagram in Fig. 4 shows the architecture of the correlation receiver. The symbols must be zero-DC because the programmable amplifier is AC coupled. For the tests Manchester coding is chosen because of its self-synchronization feature although it is not as bandwidth efficient as other codes and halves the possible data rate to 100 kbps.

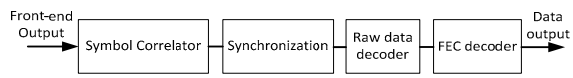

Fig. 4. Correlation receiver block diagram

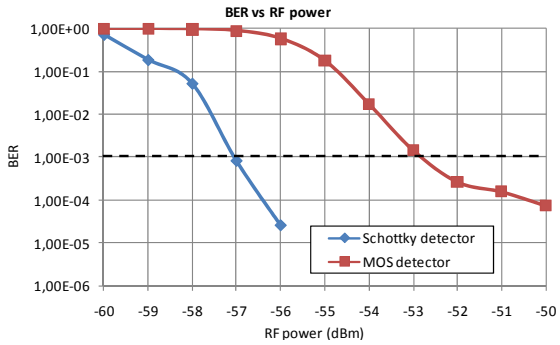

Fig. 5. BER in function of RF input power

The whole correlation receiver is implemented with low gate count (around 1000) and needs a clock frequency of around 400 KHz. This allows the signal processor to be implemented with state-of-the-art standard cell libraries adding a simulated maximum of 5 µW of power consumption for the given 120 nm CMOS technology. The required SNR at the input of the correlation receiver is 2.8 dB, under which a Bit Error Rate (BER) of 10^{-3} is achieved. BER measures are shown in Fig. 5.

3. Test setup and chip and performance

Before a test chip was implemented, a discrete setup with a Schottky diode detector, amplifier and integrator (without taking power consumption into consideration) has been built to verify the principle of the architecture. In a second stage a test chip has been designed incorporating two distinct setups one being the setup shown in Fig. 1. The second setup was realized without the envelope detector so that an external detector could be used and compared to the internal one and to characterize the programmable amplifier. A microscope photograph of the chip can be seen in Fig. 6. The reason for choosing the standard 120 nm low power CMOS process was its wide availability and low cost as well as the fact that leakage at this feature size is still limited compared to a 90 nm or smaller feature size process.

The WUR front-end draws only 7.5 µW from the single 1.5 V supply using the internal envelope detector. Using the external passive envelope detector reduces the power by 1.5 µW. The reason for this is the internal bias of the MOS detector transistor. The measured sensitivity does not relate to the data rate and is around -53 dBm using the internal envelope detector. The external envelope detector shows better sensitivity and reaches -57 dBm thanks to the higher nonlinearity and lower noise achieved. These sensitivity figures are measured at the reference BER of 10^{-3}. Table 1 resumes the performance of the WUR.

Table 1. Key parameters of the WUR

Supply Voltage	1.5 V
MOS Envelope detector power	1.5 µW
Amplifier Chain	Power: 4.5 µW Max Gain: 54 dB Bandwidth: 1 MHz
Integrator	1.5 µW
CMOS 120nm simulated power of the Correlation receiver	5 µW
Overall performance of the WUR based on the MOS detector	
Power (estimation)	12.5 µW
Data Rate	100 kbps
Sensitivity	-53 dBm
Overall performance of the WUR based on the Schottky detector	
Power (estimation)	11 µW
Data Rate	100 kbps
Sensitivity	-57 dBm

4. Conclusion and future work

This work presents the first complete implementation of a WUR with power consumption in the order of 10 µW. The architecture can be successfully adopted by wireless sensor node applications where short range wakeup capability is of advantage. In this way the overall power consumption of communication and communication latency can be reduced simultaneously.

Table 2. Performance comparison (analog front-end)

Reference	Sensitivity (dBm)	Power (µW)
Berkeley 2007 [[4]]	-50	65
Berkeley 2008 [[5]]	-72	52
This work (int. detector)	-53	7.5
This work (ext. detector)	-57	6.5

The presented results power consumption and sensitivity are compared to other works in Table 2. The proposed work is comparable in sensitivity to [[4]] by requiring much less power. The work proposed in [[5]] shows promising figures in matter of sensitivity but has still higher power consumption. All the results shown represent the front-end only. The total power consumption of the proposed solution accounting also

for the fully integrated correlation receiver, would then consume about 12.5 µW in the worst case. The value is calculated synthesizing the digital part in the same technology as the front-end, with a low leakage standard cell library.

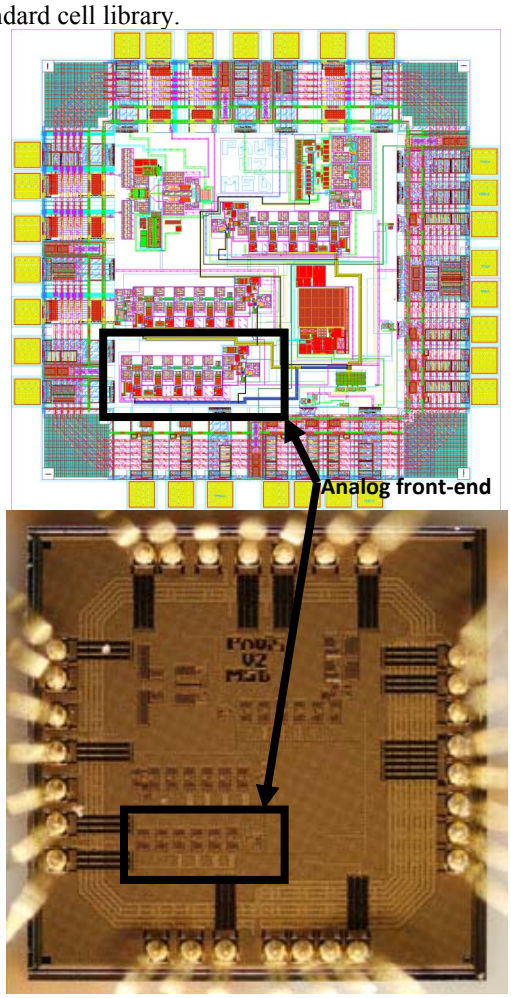

Fig. 6. Layout plot and microscope photograph of the 120 nm test chip (1.2mm by 1.2mm)

A good strategy to lower power consumption even further could be to duty cycle the Wakeup receiver in the order of milliseconds or even less thus not compromising delay and keeping the wakeup message short. This could be done very efficiently; since there is no significant turn-on time of the receiver other than in an oscillator based design where the turn-on times are of at least a few hundred µs.

In an already initiated follow-up project we intend to improve the envelope detector sensitivity and to integrate the complete receiver including clock generation in a single chip without increasing power consumption significantly.

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