

Dual Filter Stage for EMI-Optimized Solar Inverter Array

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Abstract

In the field of electrical solar power conversion efficiency is the most important topic. Also the elimination of high frequency ripple on input- and output side is an increasingly important topic. In common single-phase inverter applications the current of the solar array shows a remarkable ripple due to power pulsation on the grid. This entails two significant disadvantages: Reduced over-all efficiency due to dynamic maximum power point mismatch and reduced lifetime of the panels due to additional component stress. Furthermore in environments with several solar strings operating in parallel to reach the goal of a very close MPP operation, a distributed current source arrangement has to be chosen. On the other hand, several measurements have also to be taken into consideration to keep the output-harmonics in an acceptable range. The proposed topology discussed in this paper uses separated active filters to fulfil the given requirements: Minimized input current ripple of the cells, string-optimized maximum power point tracking and optimal power quality of the supplying grid. The topology presented in this paper shows a remarkable improvement of the over-all efficiency as well as a significantly enhanced EMC. Consequently, it is well suited for solar power inverter applications.

1. Introduction

State-of-the-art switching mode solar converters arrangements for parallel string operation (c.f. Fig. 1) are industrial standard in the field of power conversion for renewable energy applications. The starting point of our investigations was a multi-string solar array with common current sourced DC-link and a mains coupling inverter operating at the European power grid (230V). As shown in practice, the input current ripple requires a huge filter capacitor in each string to reach the goal of a satisfactory efficiency. In this paper a new concept, using an additional energy storage element is shown, which increases the efficiency and the converter output voltage quality to meet high mains quality and reduce EMC problems. To overcome the problem of energy storage in each input cell, an improved topology with shared storage elements was derived based on Figure 1.

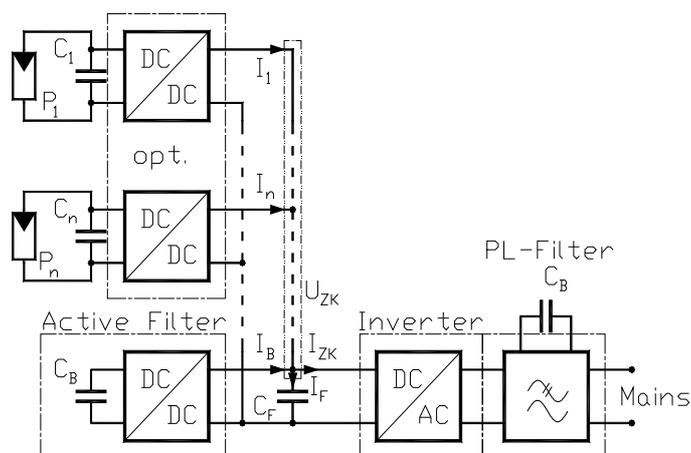


Fig. 1. Conventional solar inverter array with active input ripple compensation and power-line filter for mains (M)-interfacing

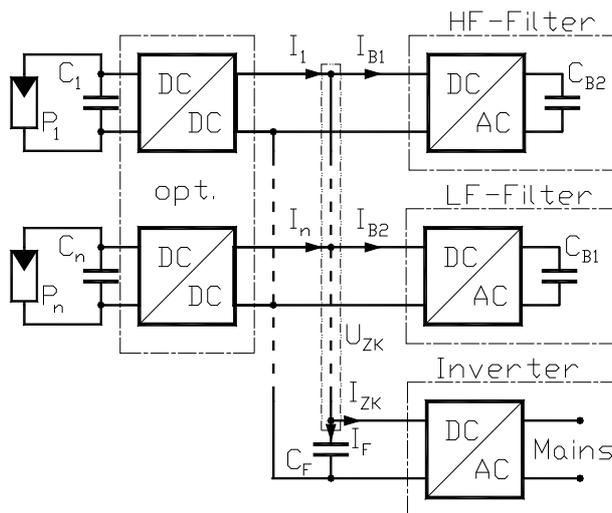


Fig. 2. Suggested Topology with two active filters on the DC-link

A further concept can see in Fig. 2: an active filter for low frequency distortion (LF) was used to keep the input current ripple of the solar strings in a tolerable range. In addition, another active filter (HF) was added to furthermore reduce the power-line harmonics and eliminate the ripple injected by the LF-filter, so that all EMC requirements can be fulfilled. In case of active power-line filtering a bi-directional paralleled current source or a series connected bi-directional voltage source is required.

2. The Basic Problem

Solar arrays can be realized in two modes: hard-wired (series-parallel connection of solar strings) and inverter coupled (each string uses its own MPP-tracking inverter), as depicted in Figs. 1 & 2. In this paper a simple hard wired arrangement was used for better demonstration. In most other cases well-known buck current source converters were used to supply the DC-link. Each stage has to be operated on its own MPP to maximize the over all system efficiency [1,2]. The result is the same as of the used simple arrangement.

In each case, due to the varying array-current, a respectively large averaging energy buffer (C_n) is needed to smoothen the solar arrays current. A standard gauge of approximately $5000\mu\text{F} / \text{kW-peak}$ at 200V solar voltage range is a good starting point to keep the voltage ripple within the recommended 2% of the MPP-voltage [3].

For mains-interfacing a simple current sourced push-pull inverter topology was used. In our application a transformer isolated main interface is chosen.

2.1. The Basic Filter Topology

The advantage of this topology is the simplified filter structure for both filters, the low-frequency input-ripple buffer and the medium-frequency ripple filter. A topology as depicted in Fig. 3 will be chosen for both filters. The simple principle of current summation is used in combination of an energy storage at higher voltage levels (in our case 400V) (ref.: $W_c=C \cdot U^2/2$). Also a much higher voltage ripple across the filter capacitor can be used without any disadvantage to the circuit behavior. (ref.: $\Delta W_c=C \cdot U \cdot \Delta U$).

To reach the goal of mains ripple elimination in the solar string, optimal efficiency and minimal costs the two filter stages have to be optimized separately. In case of the mains ripple compensator (LF-filter) a rather low switching frequency of 2.5kHz with a resulting ripple current of 15% was chosen leading to nearly negligible switching losses.

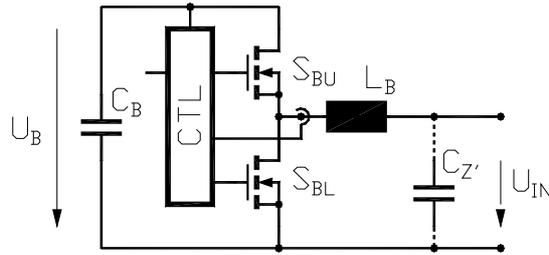


Fig. 3. Proposed active filter circuitry

The resulting “AC-ripple” injected by this stage has to be maintained by the second filter (HF-Filter) stage operating at 25kHz. Here a significantly reduced current has to be maintained. For both stages the simple current mode regulator control principle can be used leading to an easy to handle solution. Figure 4 depicts the control loops for the demonstration single solar string arrangement with direct load interface (no adapting DC-to-DC converter for the solar stings).

The two control loops formed by S1 and S2 have different specifications:

- [S1] forms the primary mains ripple cancellation loop operating at a rather low switching frequency, feed from the average solar current given by the MPPT-predictor.
- [S2] is used to minimize the switching ripple injected by S1. Its goal is also to keep the high-frequency switching noise in an acceptable range which can be filtered in the mains stage. In our case a simple bang-bang control concept was used

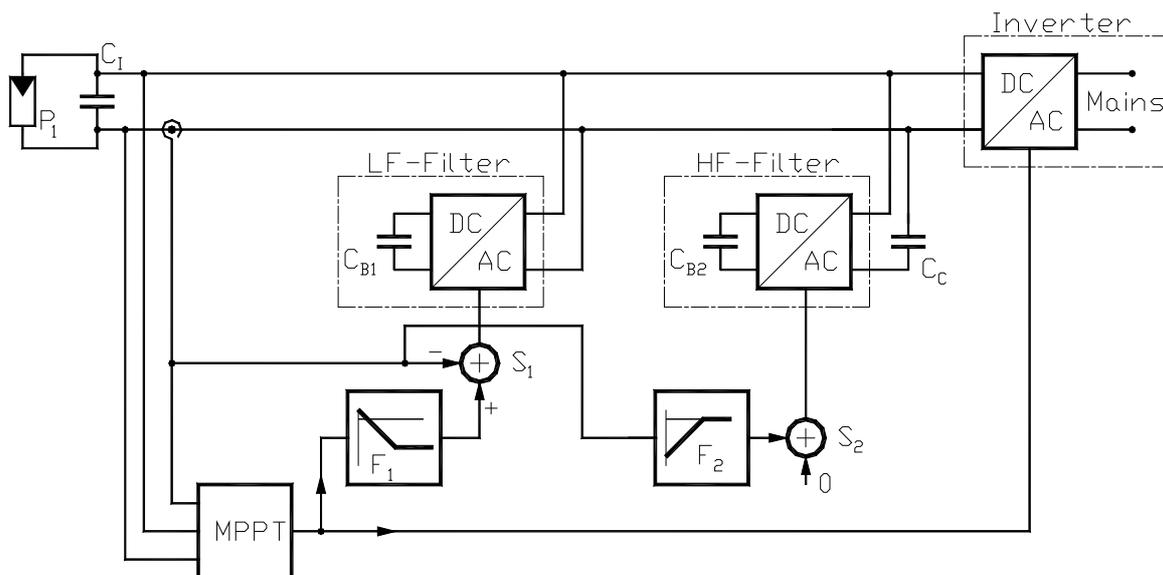


Fig. 4. Fig. 4. Compensator control principle for a single solar string

It should be noted, that for optimum plant efficiency a load sharing control system should be established. The simple principle of the parallel operation of controlled current sources forms a robust and fault-tolerant system. The proposed topology can be used as an alternative to multi-stage converters with a constant DC-link voltage and an active switching DC-to-AC inverter.

3. System Simulation

To clarify the advantages of the proposed topology, the simplified filter structure for both filters, the low-frequency input-ripple buffer and the medium-frequency output filter a detailed simulation was performed.

As one can be seen in Fig. 5. a state of the art 1.2kW solar string operating at full load has a rather huge cell voltage ripple (about 9% here), even with a rather large storage capacitor (1000 μ F in this case). A significant improvement of the voltage ripple can be achieved when an active filter stage was used (c.f. Fig. 6).

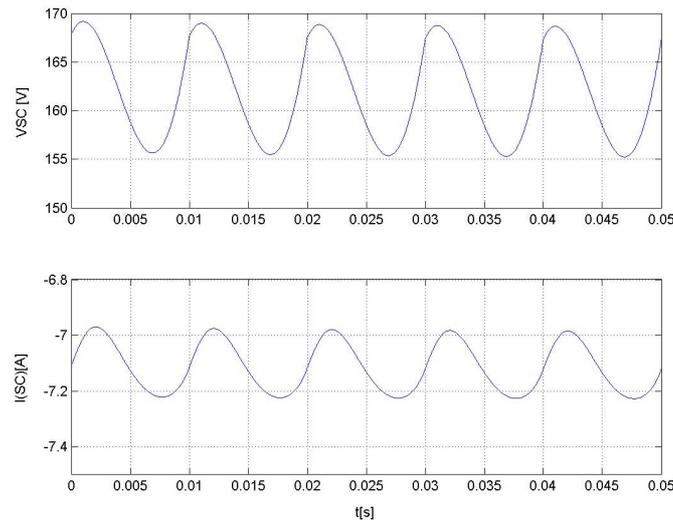


Fig. 5. Input current stress (lower trace) and voltage ripple (upper trace) of a conventional solution ($P_1=1.2\text{kW}$, $C_1 = 1000\mu\text{F}$)

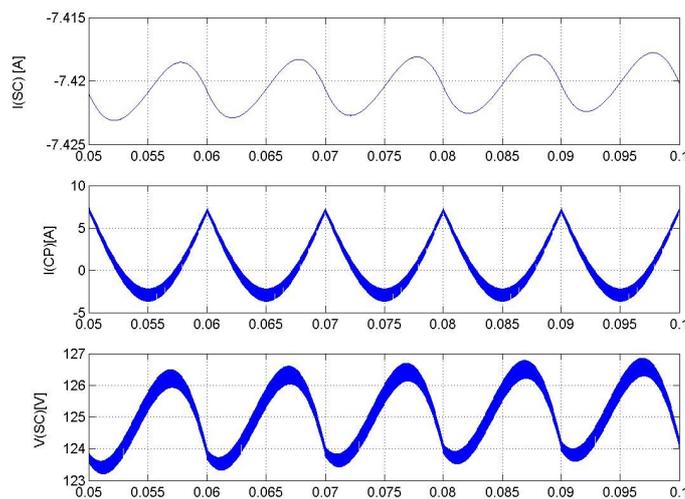


Fig. 6. Conventional compensator arrangement Input current stress, compensation filter current, array voltage ripple (from top to bottom) ($P_1=1.2\text{kW}$, 25kHz active bang-bang filter stage)

Figure 7 shows the proposed system. Here the current is shared between the two filter stages. One can see the significantly smoothed array current leading to an nearly optimal maximum power point without deviation due to mains current ripple.

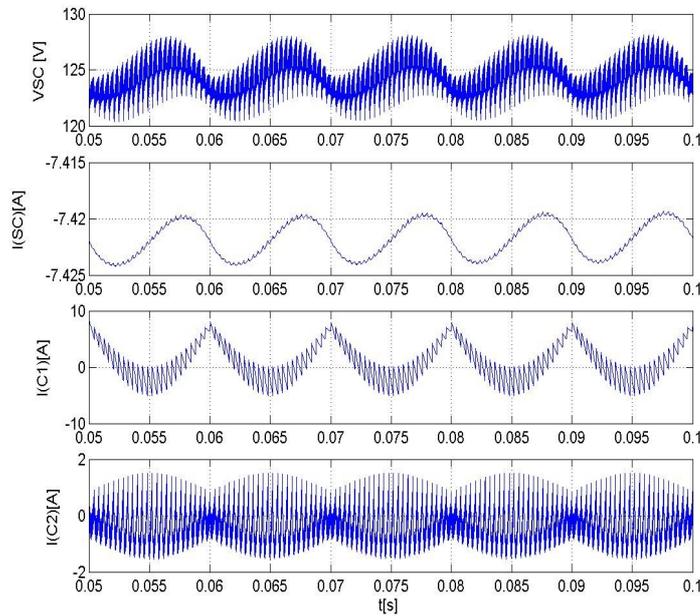


Fig. 7. System behavior of the two-loop compensator: array voltage ripple, input current stress, LF- and HF-compensation current, (from top to bottom) ($P_1=1.2\text{kW}$)

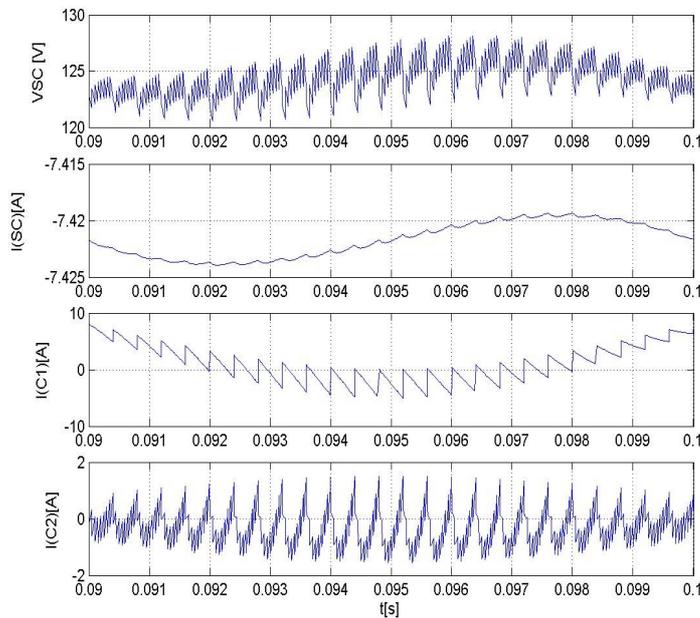


Fig. 8. Detailed system behavior of the two-loop compensator: array voltage ripple, input current stress, LF- and HF-compensation current, (from top to bottom) ($P_1=1.2\text{kW}$)

In Figure 8 the switching behavior of the stages is shown in detail. Due to the current disposing in two stages a significant improvement of the efficiency as well as component reliability in solar-, fuel cell- and battery fed inverter applications by an active reduction of the source current ripple can be achieved.

As a result the source is only loaded with a nearly perfect DC-current, which helps to hit the maximum power point without any dynamic distortions. Furthermore, the input capacitor can be decreased, because a common energy storage element is used operating at higher voltages with higher efficiency. Here under several circumstances also batteries can be used giving the possibility of building an redundant UPS-system,.

The power stage of the used filter consists of a simple half bridge arrangement feeding the ripple current. The converter is operated at several 1kHz and 10kHz respectively leading to a tolerable low output current ripple.

The effective usage of multi-phase input cells coupled with an active filter show us the capability to reach the goal of high efficiency, reduced current harmonics and improved EMC.

4. Conclusion

The proposed solution improves efficiency as well as component reliability in solar-, fuel cell- and battery-fed inverter applications by an active reduction of the source current ripple. As a result, the source is only loaded with a perfect DC-current, which helps to hit the maximum power point without any dynamic distortions. Furthermore, the input capacitor can be decreased, because a common energy storage element is used operating at higher voltages with higher efficiency. It should be noted, that for optimum plant efficiency a load sharing control system should be established. The simple principle of the parallel operation of controlled current sources forms a robust and fault-tolerant system. The proposed topology can be used as an alternative to multi-stage converters with a constant DC-link voltage and an active switching DC-to-AC inverter.

The power stage of the used filter consists of a simple half bridge arrangement feeding the ripple current. The converter is operated at several 10kHz leading to a tolerable low output current ripple. Cheap TO-247 or even TO-220 or cheap surface mount packages can be used leading to a compact and efficient system design.

The effective usage of multi-phase input cells coupled with an active filter shows us the capability to reach the goal of high efficiency, reduced current harmonics and improved EMC.

Furthermore, it should be noted that the parallel structures are forming a redundant system which can be used to increase the systems reliability by building a fault tolerant arrangement. All these advantages can simply be realized in software and do not affect the hardware.

The simple control principle of the power stages can easily be implemented using state-of-the-art microcontrollers without additional logic support for the pulse pattern generator; a simple PWM stage fulfills all the requirements. Also the maximum power point tracking for the solar generator can be easily implemented by monitoring the system signals ($i_1 \dots i_N$, and i_{zk}).

The topology presented in this paper is a simple and effective solution for small to medium power grid coupled applications. The concept is well suited for wind-, solar- and renewable energy as well as for aerospace applications.

5. Literature

- [1] Wai, R; Lin, C: "Active Low-Frequency Ripple Control for Clean-Energy Power Conditioning Mechanism", Proceedings of the IEEE Transactions on Industrial Electronics 1-2010, Vol.: PP , Issue: 99, pp.: 1-10
- [2] Veerachary, M.; Senjyu, T.; Uezato, K.: "Maximum power point tracking control of IDB converter supplied PV system", Proceedings of the IEE Electric Power Applications 2001, Vol.: 148 , Issue: 6, pp.: 494 - 502
- [3] K. H. Edelmoser, F. A. Himmelstoss: "A Simple, Efficient, and EMI-Optimized Solar Array Inverter, WSEAS Transactions on Circuits and Systems, Issue 9, Vol. 9, Sept. 2010, pp.597-606, ISSN: 1109-2734.