High-Efficiency Battery Storage Unit for Renewable Energy DC Micro-Grids

Helmut L. Votzi and Hans Ertl,
Power Electronics Section, Vienna University of Technology, Austria
helmut.votzi@tuwien.ac.at

Abstract

The paper describes a battery storage unit for small DC micro-grids based on a multi-cell topology. The system consists of a series arrangement of lead-acid type battery cells where each cell is equipped with an individual DC-DC buck converter located directly at the battery terminals. For minimizing the output ripple the cells are operated in interleaved PWM mode. With this the cell-to-cell wiring can be used as output ripple filter avoiding dedicated smoothing coils. The proposed circuit is based on low-voltage MOSFETs operated at low switching frequencies resulting in 99%+ converter efficiency rates. The control of the unit, furthermore, emulates a virtual output impedance of the battery storage system. This opens an easy possibility for energy management and load leveling of the DC micro-grid by adopting the power consumption of the individual loads according to the actual grid voltage which is used as a load status indicator of the grid.

1. Introduction

1.1. DC Micro-Grid – Basic Relations

Caused by the increasing energy shortage renewable energy systems, distributed generation and micro-grids will rapidly gain importance in the near future. It is predicted [1] that local distribution systems advantageously will be based on DC as a kind of renaissance of Edison's original DC grid concept. The key reason is that nearly all renewable energy sources (solar cell arrays, fuel cell systems, micro-turbines) and energy storage units (battery or super-capacitor sets) being required for load leveling and in especial the vast majority of electrical loads (computers, TV sets, lighting equipment, drives, power supplies, chargers, …) actually are based on DC (or an inner DC voltage link). In other words: If all generator, storage and load units are of DC origin and in any case are coupled to the micro-grid via power electronic converters, a DC-type micro-grid (as proved in practice since many years, e.g., for emergency lighting applications) will be optimal for common low-voltage power distribution because it avoids unnecessary rectifier/inverter losses and costs.

In general, the DC micro-grid which will be used for commercial facilities and industry applications [2, 3], for telecommunication equipment and server farms [4] or for residential/household power supply [5] does not operate in a pure standalone mode but usually shows a coupling to the public three-phase AC mains (e.g., a uni- or bi-directional converter connected to the secondary of the medium-voltage feeder transformer or directly to the low-voltage AC mains). The intention of the DC micro-grid, however, is that the energy exchange to the AC mains is minimized and limited by local generation, local storage units and load management.

An interesting pilot plant of a DC micro-grid based renewable energy system has been reported in [6]. The total system consists of (i) a solar cell generation unit, (ii) a wind turbine generation unit, (iii) an AC grid connected bidirectional inverter unit, (iv) a fly-wheel power leveling unit and, finally, (v) a battery storage unit which are all connected to a DC micro-grid with 345V nominal voltage (Fig.1). The basic power flow control of the system is performed such, that the power electronic converters of the units emulate a specific voltage/current characteristic which will be described in simplified manner in the following (fly-wheel and wind turbine unit neglected): According to Fig.1b, the solar generation unit shows a pure current source characteristic where the current (defined by the MPP control) is not dependent on the grid voltage U_{DC} up to a maximum limit. On contrary, the battery storage unit shows an (artificial) ohmic characteristic of low impedance value R_O up to a current limit. Finally, the AC grid inverter shows a much higher impedance around the nominal value of 345V but gets much stiffer for

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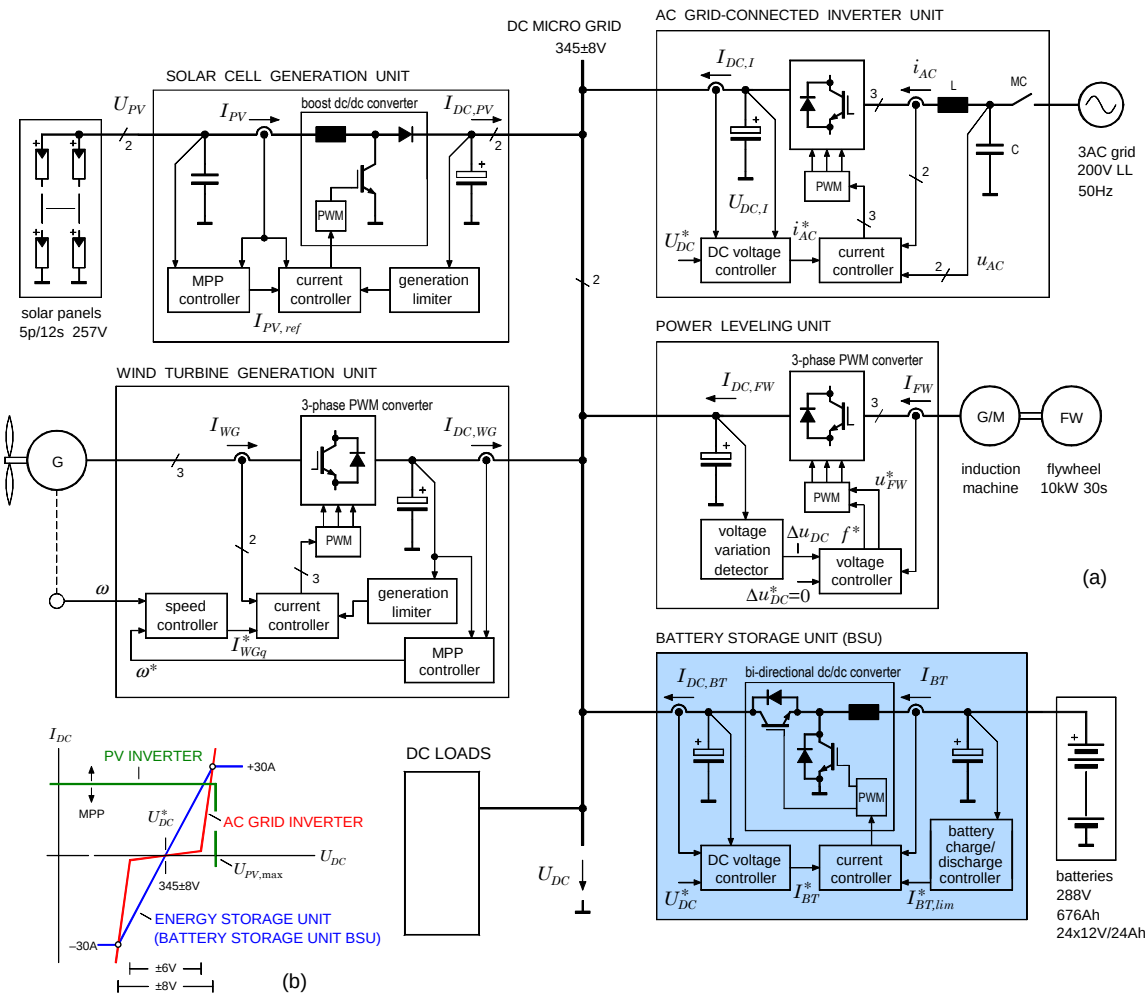


Fig.1: DC micro-grid based renewable energy supply system proposed in [6].

voltage deviations >±8V. Consequently, power fluctuations at first are covered first by the battery storage giving intelligent DC loads the possibility for reducing their power consumption via sensing the grid voltage. It shall be noted, that all DC loads are assumed to be of active type (i.e., equipped with power electronic) and accept varying supply voltages (which in fact is used to “communicate” the load status of the total system). As far as possible all DC loads shall provide a load characteristic where the drawn power is reduced (e.g., by switch-off “low-priority” circuit parts) in case of sagging grid voltage.

By the measures described before a very robust DC micro-grid can be achieved which may even be used for emergency power supply (e.g., emergency lighting), especially if distributed battery storage units (at least one unit within each fire compartment zone) are used. As compared to AC micro-grids where the control is much more complex because it has to consider active and reactive power flow and phase synchronization or phase loss [7], the DC solution features a simpler and more robust primary control. In addition, the storage devices of the renewable energy sources (solar and wind energy unit) for DC systems do not have to cover 100Hz power pulsations as this basically is the case for single-phase AC systems. As a consequence, huge electrolytic capacitors (being a very characteristic but temperature dependent and life-time limiting component of single-phase solar inverters) can be avoided to a large extent or even completely opening the possibility of integration of the converter into the (often rather hot) solar cell module.

1.2. Multi-Cell Converter Topologies – Semiconductor Relations

In Fig.1 the BSU is depicted as single-cell arrangement equipped by IGBTs due to the high DC grid voltage level of 345V. The basic drawback of this topology (besides not very high efficiency) is that

many DC sources (24 x 12V-battery packs) are connected in series at the input side and it is hardly possible to achieve battery charge balancing. These disadvantages can be avoided by multi-cell topologies where individual DC/DC converters are assigned to each battery pack. It might be objected, that such cascaded converter topologies show reduced efficiency due to the huge number of semiconductors being actually connected in series. However, it has to be considered that the required break-down voltage of the transistors is significantly reduced by the series arrangement. This leads to a substantial advantage in case MOSFETs are used. (MOSFETs act as a key switching device for renewable energy converters because their ohmic on-state characteristic gives improved partial-load efficiency.) Due to a basic principle of majority-carrier semiconductors, the on-resistance of standard MOSFET follows the relationship $R_{DS,ON} \infty (U_{DS,BR})^{2.5}$ with $U_{DS,BR}$ being the break-down voltage of the device. For equal chip-size, a MOSFET of half voltage rating only shows a $R_{DS,ON}$ -value of ≈1/6 (Fig.2a)! Thus if the total DC grid voltage now is split-up to be operated by N converters connected in series (which require MOSFETs with a voltage rating according 1/N) the on-state losses of the total converter array follow the relation $N \cdot (1/N^{2.5}) = 1/N^{1.5}$ and hence are lowered by application of the multi-cell principle (e.g., for N = 4, the on-state losses in theory will be reduced by a factor of 8!).

Standard MOSFETs follow the "power-2.5-law" closely (Fig.2a) with the exception of the very-low voltage region, where the resistance of the bonding dominates $R_{DS,ON}$. As is demonstrated clearly using a virtual short-circuit power of the transistor as a quality index (defined as $P_{SC} = (U_{DS,BR})^2/R_{DS,ON}$, Fig.2b), standard MOSFETS will be most effective in the voltage region 75...150V. Latest generation devices like OptiMOS® here show an even improved performance forming an ideal switching device for highly-efficient multi-cell renewable energy converters. Remark: Charge compensation switching devices like CoolMOS®/FD-Mesh® (in the region 500...800V) would also be characterized by an excellent on-state performance. However, these devices show a rather poor characteristic of the intrinsic free-wheeling diode which prohibits the application in full-bridge arrangements as required for the aimed applications.

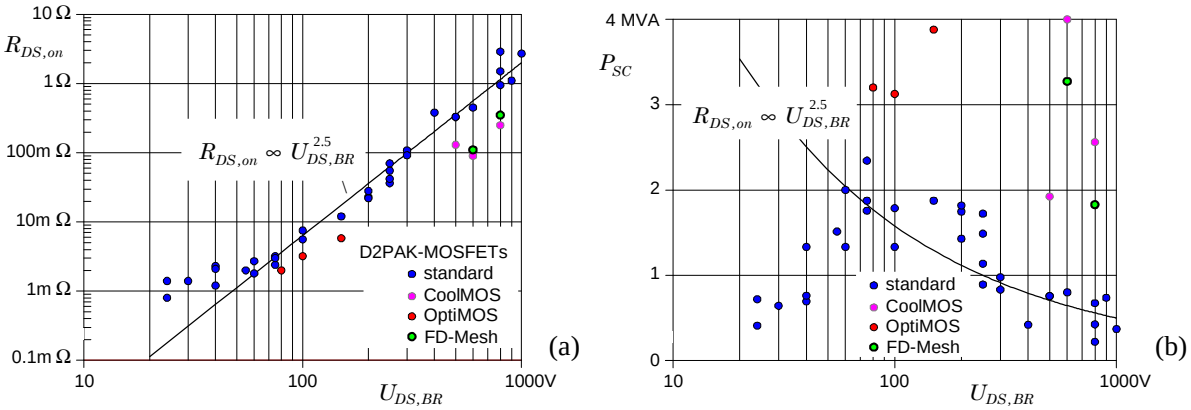


Fig.2: Comparison of commercially D2PAK-MOSFETs (standard, CoolMOS®, OptiMOS®, FD-Mesh®).

2. Multi-Cell Battery Storage Unit – Simulation Results

According to the previous considerations, 75…150V MOSFETs would be very well suited for high-efficiency converters. Taking into account however the battery balancing advantage, a multi-cell BSU is analyzed here where each individual battery is equipped with a converter stage. In this case 30…60V MOSFETs are utilized which still show good efficiency and which are available at very low costs due to their popular application in volume production electronic devices like mainboards, laptops etc.

As depicted in Fig.3 a BSU consisting of N =16 cells in a series arrangement is designed based on 12V lead-acid gel-type batteries. Each cell shows a buck-type DC/DC converter formed by MOSFETs in half-bridge configuration (Fig.4). The converter cells are operated in an interleaved PWM mode, resulting in an N-times effective switching frequency to reduce the ripple current. With this (despite the fact that a rather low actual switching frequency of only 1kHz is used by the cell to avoid high switching losses) the required smoothing inductor can be realized in a "distributed" manner. Instead a dedicated filter coil the inductance is provided by clip-on ferrites placed at the cell-to-cell wiring of the system. As

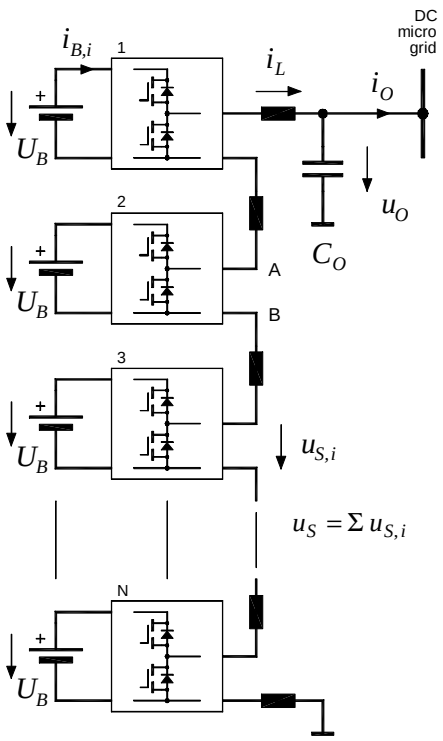


Fig.3: Basic topology of the proposed battery storage unit consisting of a multi-cell converter arrangement.

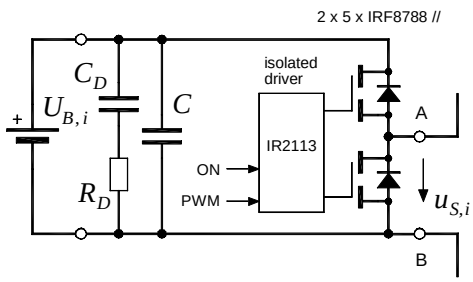


Fig.4: Structure of single converter/ battery cell.

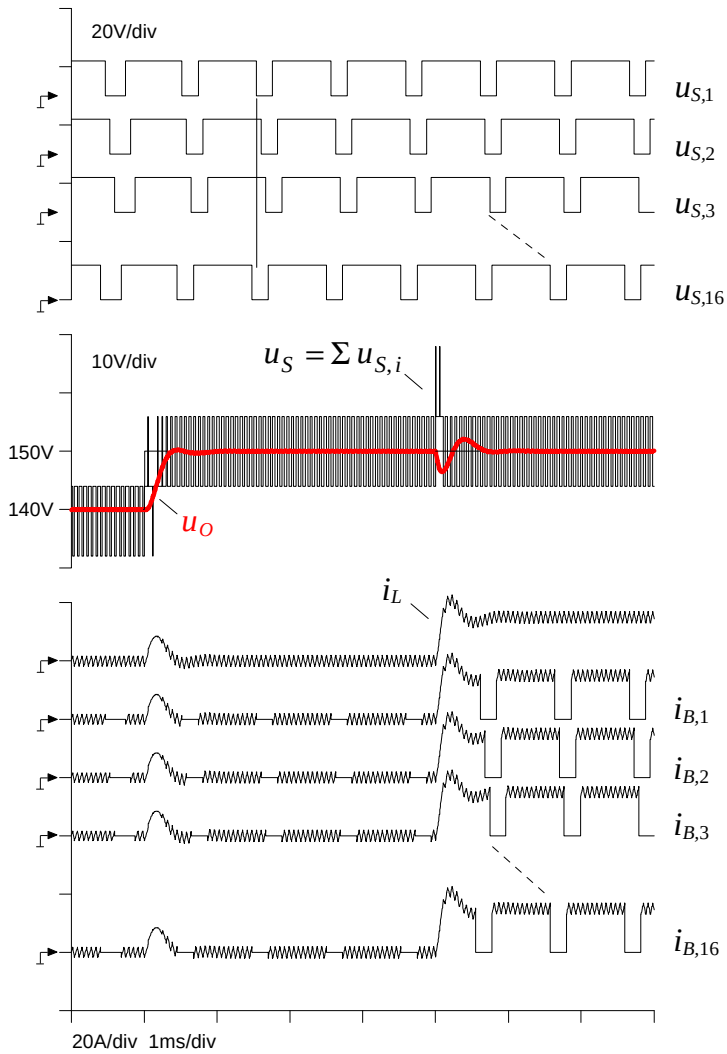


Fig.5: Voltage and current wave shapes of the proposed BSU. Reference voltage step ΔU_O=10V at t=1ms, load step ΔI_O ≈20A at t =5ms; Parameters: N=16, U_B ≈12V, f_S =1kHz, L_{SUM} = 50µH, C_O =200µF, duty cycle d ≈ 0.75 (simulation results).

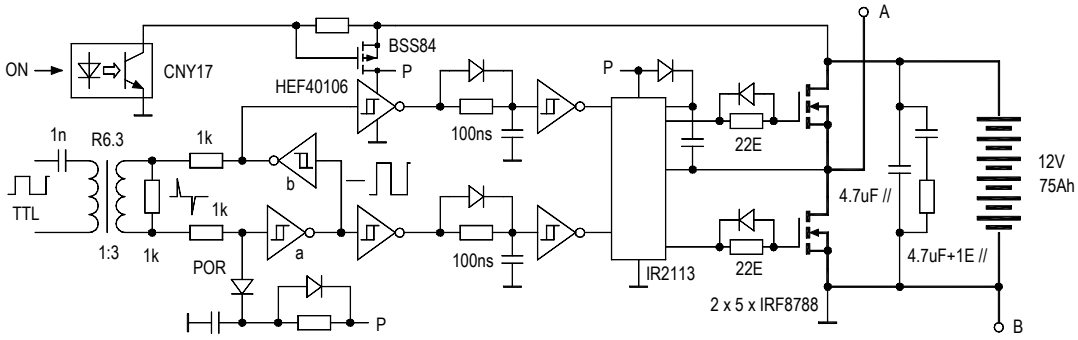
a consequence that the DC/DC converter is designed as a small PCB circuit located directly at the battery pack using solid terminal bars very high converter efficiency rates can be achieved within a wide load region.

Because the DC link of the converter is not equipped with large electrolytic capacitors the battery current is of pulsating shape (Fig.5) which might be seen as a drawback for the batteries. Several publications however report that the useful capacity of batteries even is increased using a pulsed current load instead of a constant current discharge. This is caused by the charge recovery process that takes place in the battery during the off-periods, called rest time [8]. In [9] it is dedicated mentioned that an intermitted discharging current using a frequency of ≈1kHz results in a several percent higher capacity. [9] is well supported by experimental results which illustrate that the provided energy of lead-acid batteries (as used in the proposed system) can be efficiently extended by pulse-shape load currents of typically 1kHz repetition rate. Inspired by these publications, the described BSU omits large DC link capacitors (electrolytic capacitors) in parallel to each battery. Instead, only small capacitors are implemented to limit the switching transients (C in Fig.4), additional snubber elements C_D, R_D are provided for damping the ringing caused by the inductance of the battery and the busbars). Hence, the battery currents will show a pronounced pulsed shape of basic (1kHz) switching frequency (cf. lower traces $i_{B,i}$ in the simulations of Fig.5).

3. Design of Converter Cell – System Control

The DC/DC converter of each cell here is designed for the application of 12V/75Ah (900Wh) batteries. A projected storage time of 5h therefore results in a typical output power level of 180W (9V/20A) per cell. To achieve efficiency rates of 99%+ all losses have to be minimized carefully considering (a) conduction losses (ultra-low $R_{DS,ON}$-MOSFETs), (b) switching losses (f_S only 1kHz, ripple minimization by interleaved PWM), (c) wiring losses (short distance current paths on PCB, utilization of cell-to-cell wiring as smoothing inductor). In addition, care has to be taken also on the losses of the driver stage. According to Fig.3 all PWM signals of the individual cells have to be isolated. Common isolation techniques like high-speed "logic" optocouplers, however, show rather high supply current requirements. A 6N137, e.g., would require ≈20mA supply current including output pull-up resistor; the associated loss (=0.25W) is not negligible. (It has to be considered that 99% efficiency on a 200W converter implies only 2W losses in total.) Furthermore, such "logic" optocouplers in general show 5V supply hence an additional voltage regulator is evident. In the proposed driver circuit, therefore, the PWM signal is magnetically isolated based on a small R6.3-pulse transformer. For reducing the core size only on-/off-pulses (≈1µs) are transmitted, which are restored to the original PWM signal by a flip-flop formed by a feedback loop of two inverters a, b (extended by a power-on reset POR). The residual gates of the logic IC (15V CMOS family) are used for generating the half bridge's interlock delay. The actual gate drive current is performed by an IR2113 device. The driver must be activated by supply voltage turn-on via a standard optocoupler controlling a small MOSFET-switch (turn off quiescent current ≈2µA). In operation mode a very low supply current of only 2.9mA has been measured including all of the MOSFETs gate drive power (no load output current, switching frequency 1kHz).

The TTL drive signal is provided by a central BSU controller where a multi-phase PWM generator is implemented using a FPGA. In order to minimize the switching delays, the drive signals are distributed to the cells using a parallel bus (hardware-coded addressing). The central BSU controller guides the system at the grid side (power management) and provides also the charge/discharge management of the individual battery packs calculating according reference values for the cell's voltage/current



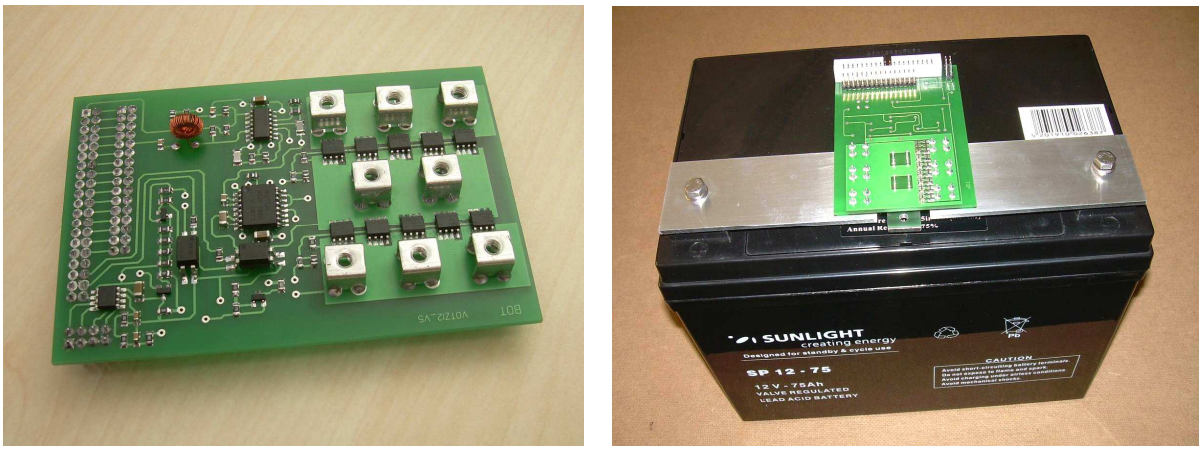


Fig.6: Implemented converter module; top: gate driver stage; left: DC/DC converter PCB showing 2x5xSO8 MOSFETs, driver and terminals; right: PCB module mounted (upside-down) directly on top of lead-acid battery.

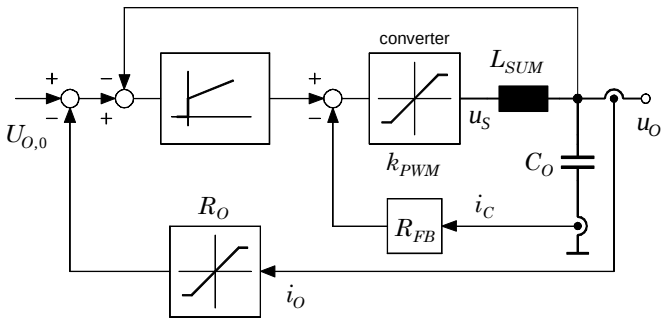


Fig.7: Basic BSU control scheme; PI-type output voltage control with underlying active damping of the LC filter ("pole-splitting"); virtual (emulated) output impedance R_O.

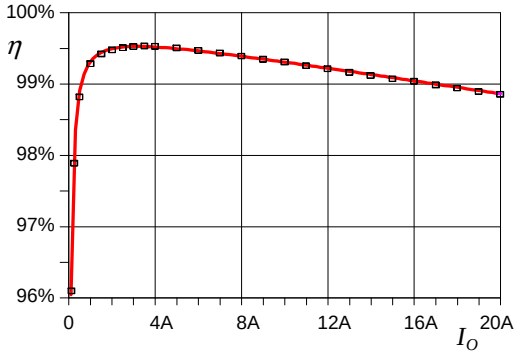


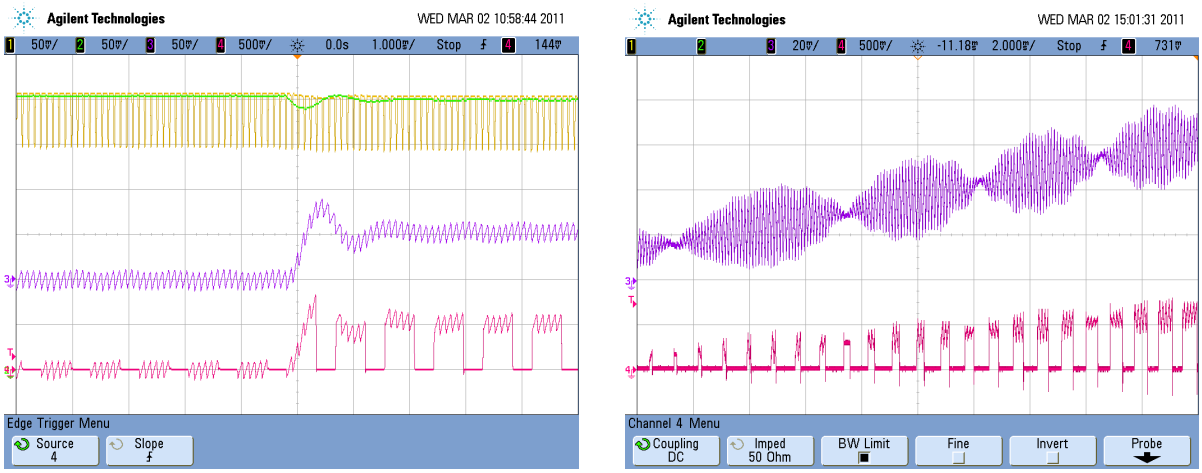
Fig.8: Measured efficiency of a converter cell (losses of smoothing coil not included).

controllers based on the measurement values of all BSU input (battery) and output quantities. For this the gate driver is equipped with small micro controller for measuring the battery voltage (not shown in the schematic of Fig.6). The communication between the central controller and the individual measuring controllers is performed using a serial 2-wire optically isolated data bus.

The basic output voltage control of the BSU is illustrated in Fig.7. Due to the quasi-natural sampling scheme implemented in the polyphase modulator, the PWM converter can be modeled by a simple proportional characteristic k_{PWM}. The LC output filter shows a poorly damped second order system (actually the system is damped only by the wiring losses and by the ESR of the output filter capacitor). To achieve a good control behavior using a simple PI-type controller, a virtual damping is introduced by adding a capacitor current feedback path to the control loop. The factor R_{FB} leads to a pole-splitting of the LC filter which eases the dimensioning of the PI controller (compensation of the slower filter time constant by the PI controller zero). By adding an output current feedback the BSU further is equipped with an output impedance R_O for the load management of the micro-grid as described in section 1.1. R_O here is of virtual type, i.e., lossless.

4. Measurement Results of Prototype System

The measurements taken from the laboratory prototype demonstrate very good efficiency rates η (Fig.8, parameters: battery voltage U_B=14V, duty cycle d=0.75, switching frequency f_S=1kHz); η > 99% is valid within a wide load range. Due to the minimized driver losses η=96% is achieved even in case of a 1% load. On the contrary in case of full load operation (20A) the losses are in a region (≈2W) that they can be dissipated easily by the PCB and the attached battery terminal bars. The diagram of Fig.8, however, does not include the cell-to-cell wiring (used as smoothing inductance), and certainly also the



t: u_S, u_O (10V/div) m: i_L b: i_B (10A/div) (1ms/div) t: i_L (4A/div) b: i_B (10A/div) (2ms/div)

Fig.9: Voltage/current wave shapes of 8-cell prototype; left: transient load response; right: duty-cycle ramp-up.

battery efficiency itself is not taken into account. The time behaviour of the converter voltage u_S and of the filtered BSU output voltage u_O (cf. Fig.3) as well as of the input (battery) current i_B and of the smoothing inductor current i_L is given in Fig.9. There the left picture illustrates a load step response similar to the simulation of Fig.5, whereas in the right part of Fig.9 a voltage ramp-up is depicted. Here the ripple amplitude of i_L shows the nodes being typical for multi-level converters.

5. Conclusions

In the paper the basic relationships of a multi-cell battery storage unit are verified. The system is characterized by a “stacked” arrangement of (here) 8…16 batteries where each battery is equipped with a dedicated DC/DC (buck) converter. Ultra-low $R_{DS,ON}$-MOSFETs therefore can be used leading to low on-state losses. Because the cells are operated in an interleaved PWM mode, a rather low switching frequency of typ. 1kHz is sufficient, despite the fact that the “parasitic” inductance of the cell-to-cell wiring (enhanced by clip-on ferrites) is used as smoothing inductance. Consequently, extremely low total converter losses appear leading to ≈99% efficiency rates valid within a wide load current region. For this, a driver stage designed showing minimal operating and quiescent power demand is a prerequisite which is achieved using 15V CMOS logic devices and pulse-transformer signal isolation.

The basic control of the system is performed by a (digital) PI-type controller with underlying filter capacitor current feedback implemented in an FPGA. Balancing of the batteries is aspired such that the voltage of each individual battery is measured (based on a small “local” microcontroller transmitting the measurement values via a serial 2-wire bus). Subsequently the central system controller slightly adopts the duty cycle ratio of the individual cells until equal d/dt-rates for the battery voltage is guaranteed. Simulation shows that with such a scheme the battery storage unit also can be operated in case of different Ah-ratings of the batteries which will appear in a real system for gradually battery ageing.

6. Literature

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