Analysis of a New Third Harmonic Injection Active Rectifier Topology Based on an NPC Three-Level Converter Cell

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Abstract

Active three-phase rectifier systems usually cover a wide field of applications where high total power factor (99%+) and low mains current THDi (typ. <5%) are required. Passive three-phase rectifiers on contrary are characterized as highly efficient and robust whereas their power factor is limited to 0.9…0.95 due to rather high harmonic input current components (THDi up to 48%). This paper analyzes a novel circuit topology for passive three-phase rectification. The proposed concept aims to an extension/option for standard diode rectifiers with DC side smoothing inductor based on third harmonic injection. The paper describes the fundamental operating principle and determines the current and voltage stress of the circuit components. Furthermore, design guidelines for a 10kW prototype rectifier including an appropriate control concept are included and proved by simulation.

1. Introduction

Standard passive three-phase rectifier circuits are widely used for industrial applications. Passive (diode) rectifiers are highly efficient, robust and simple and utilize a very cost effective mains input stage for feeding the DC link (formed in general by electrolytic capacitors) of e.g., switch-mode power supplies or drives. These rectifiers, consisting of a three-phase diode bridge and a smoothing inductor L_{DC} (mainly located on the DC side), however, are characterized by a total power factor limited to ~0.9 and rather high input current harmonics (THDi up to typically 48%). Further improvements of the input current quality would result in huge smoothing inductor size and in principal is limited to a THDi of > $\sqrt{(\pi^2/9-1)}$ = 31% and λ < 0.95 even for $L_{DC} \rightarrow \infty$) [1]. Consequently, in order to provide substantially enhanced ("sinusoidal") input currents a large quantity of circuit variants of active three phase rectifiers have been developed [2]. For many industrial applications (e.g., AC drives) however, it would be a very interesting concept if the basic application is equipped by a cheap passive rectifier which optionally can be enhanced by an additional upgrade device if sinusoidal mains currents are required.

The proposed unit is based on the third harmonic injection principle as described in [2] and illustrated in Fig.1. The total rectifier system is formed by three parts (Fig.1 (a)): (i) the standard three-phase diode bridge with DC side smoothing inductor and output capacitor, (ii) the active current shaping network, implemented here by two controlled current sources and (iii) three bidirectional switches S_1, S_2, S_3, which 60°-cyclically connect the current shaping network to the systems AC input. With this a current can be injected into the AC side also in that time intervals where a standard diode rectifier would show its characteristic 60°-gap. The two current sources now are controlled such, that current wave shapes as shown in Fig.1 (b) appear at the diode bridge (i_P (green) and i_N (blue)), resulting finally in three sinusoidal input currents at the AC side.

Various alternative topologies to implement an active three phase rectifier system via third harmonic injection have been proposed in literature (e.g., [3], or [4]). These approaches offer also a controlled DC output voltage, however, show the drawback that the full amount of output power has to be processed by the semiconductors. Recently, an approach has been published in [5] based on the principle as described in Fig.1 (featuring that the semi-conductor switches have to handle only a fraction of the total output power) where the two injection current sources are implemented by two two-level half-bridges. However, con-

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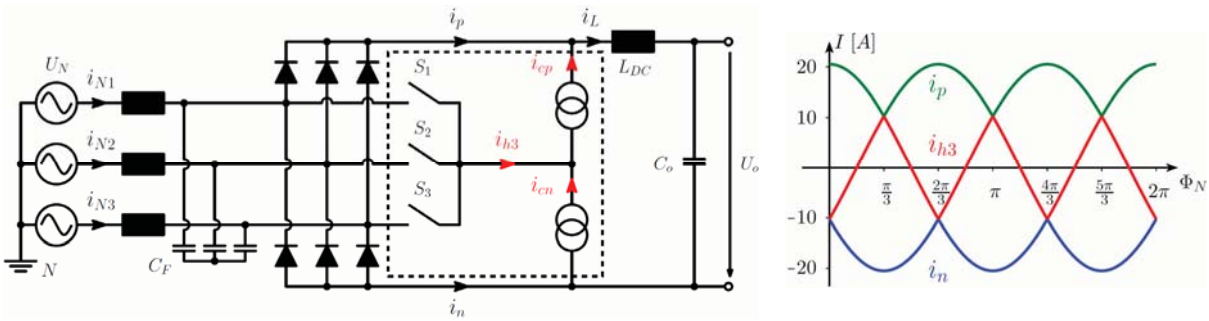
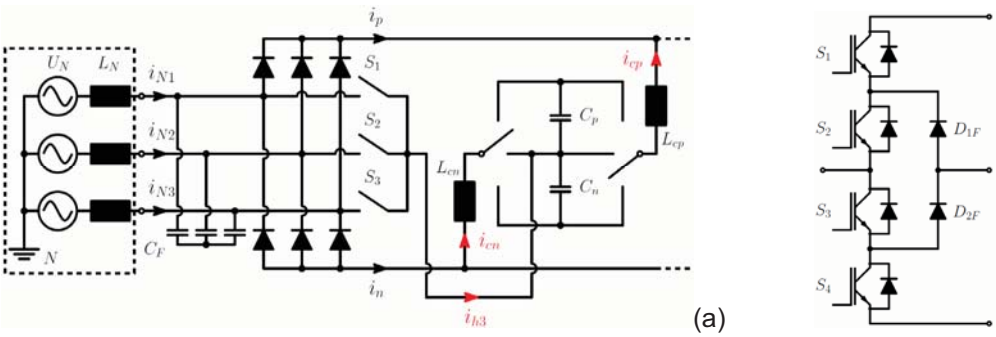


(a) (b)

Fig.1: Basic principle (a) and corresponding idealized current wave shapes $i_p(x)$, $i_{h3}(x)$, $i_n(x)$ (b) for a 10kW third harmonic injection active three-phase rectifier ($I_{p,pk}$ calculates to 20.5A).



(a) (b)

Fig.2: Third harmonic injection using three-level switching stage as current shaping network in order to prevent current distortions at the 60° interval transitions (a); realization of three-level branch based on neutral point clamped (NPC) topology (b).

sidering the voltage drop across the required switching-frequency smoothing inductors the proposed circuit cannot generate the required voltages at time instants where the midpoint voltage approaches the positive and negative DC-bus voltage waveforms. This leads to intrinsic current distortions appearing at the 60° sector transitions which finally worsen the THDi of the input currents. The proposed topology (Fig.2) therefore takes advantage of three-level structures and avoids the mentioned current distortion drawback of [5]. The three-level structure can be implemented as neutral point clamped (NPC) stage (Fig.2 (b)) which will be discussed here or, alternatively, in flying-capacitor or T-type structure.

2. System Description

A detailed schematic of the proposed topology is given in Fig.3. The circuit is formed by a standard passive rectifier stage (6 diodes D_1...D_6, a DC-side smoothing inductor L_{DC} with output capacitor C_o) and an active circuit extension (two three-level NPC branches with smoothing inductors L_{cn}, L_{cp}, three bidirectional switches S_1…S_3 and filter capacitors C_F at the AC side). The active circuit extension only actively shapes the rectifier input currents but the systems output voltage is still defined by the passive rectifier $U_o = \sqrt{6 \cdot 3/\pi} \cdot U_N$. Remark: On contrary to, e.g., a Vienna-Rectifier the analyzed system does not provide output voltage regulation which, however, is not a serious drawback for many industrial applications like drives or industrial power supplies. The two NPC branches inject “correction” currents i_{cn}, i_{cp} to the diode bridge such that i_n, i_p according to Fig.1 (a) result as diode bridge output currents. The center point M of the 3-level converter cell cyclically is switched to the AC input terminals via bidirectional “low-frequency” (i.e., $6 \cdot f_N$) switches S_1…S_3 which have to inject current into the appropriate mains phase during the zero-current period of the diode bridge. Low-frequency type IGBTs (e.g., two standard IGBTs with free-wheeling diode in anti-serial

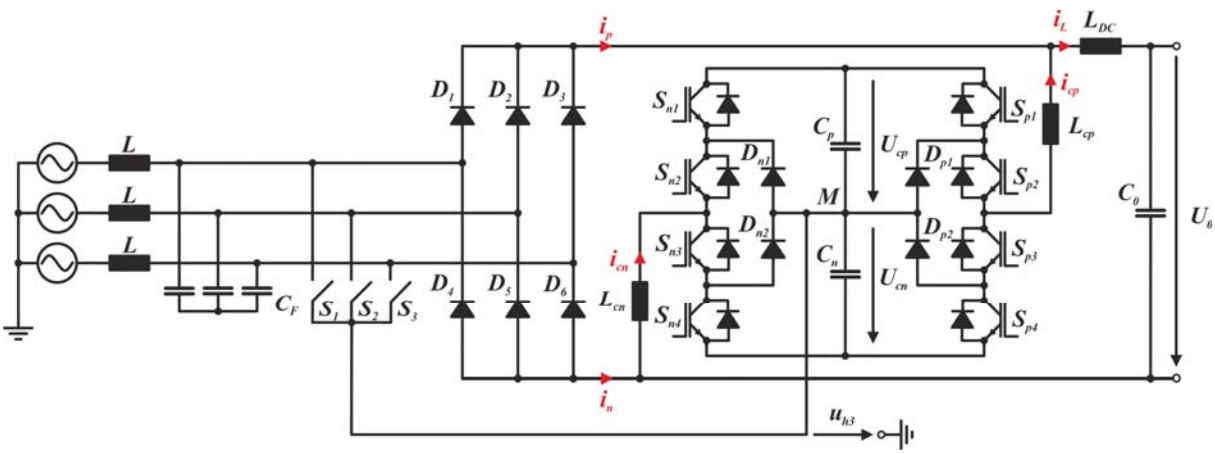


Fig.3: Proposed new circuit topology employing two 3-level NPC switching branches (shown AC side inductances L are not actual components but represent mains inner impedance).

configuration or, alternatively, two reverse-blocking IGBTs in anti-parallel arrangement) advantageously are used to implement $S_1 \ldots S_3$ achieving low switching and on-state losses as every bidirectional switch is turned on for a 60° interval only twice within a mains period. Each NPC branch consists of four switches (e.g., $S_{p1} \ldots S_{p4}$), two clamping diodes (e.g., D_{p1}, D_{p2}) and a common DC voltage link formed by C_p, C_n. By proper control of the NPC output currents finally sinusoidal mains currents in phase with the corresponding mains voltages can be achieved. This results in a permanently floating potential of the midpoint with respect to the grids neutral line (commonly earth GND). The midpoint voltage u_{h3} for the sector, e.g., $\phi_N = [0 \ldots \pi/3]$ is defined by

$$u_{h3}(\phi_N) = u_p(\phi_N) + u_n(\phi_N) = \hat{U} \cdot \cos\left[\phi_N - \tfrac{2\pi}{3}\right] \quad \text{with} \quad \hat{U} = \sqrt{2} \cdot U_N \ . \tag{1}$$

2.1 Duty Cycles

In the following the PWM of the switching cell is analyzed. For the three-level NPC branch connected to L_{cp} the required duty cycle d_{p1} calculates to

$$d_{p1}(\phi_N) = \frac{u_p(\phi_N) - u_{h3}(\phi_N)}{U_C} \tag{2}$$

with U_C being the DC link voltage level. Considering a specific 60° interval (e.g., $\phi_N = [0 \ldots \pi/3]$) the duty cycle can be computed to

$$d_{p1}(\phi_N) = \frac{\hat{U} \cdot \cos(\phi_N) - \hat{U} \cdot \cos(\phi_N - \frac{2\pi}{3})}{U_C} = \frac{-\sqrt{3}\hat{U} \cdot \cos(\phi_N - \frac{5\pi}{6})}{U_C} = \frac{-\hat{U}_{LL} \cdot \cos(\phi_N - \frac{5\pi}{6})}{U_C} \tag{3}$$

with U_{LL} representing the line-to-line voltage of the mains ($U_{LL} = \sqrt{3} \cdot U_N$). In order to guarantee operation a minimum DC link voltage level of typically $U_C = 600\text{V}$ has to be chosen assuming a standard 400V_{rms} mains leading to a modulation index M of

$$M = \frac{\hat{U}_{LL}}{U_C} = \frac{\sqrt{2} \cdot 400V}{600V} \approx 0.94 \ . \tag{4}$$

The individual DC link voltages U_{cp} and U_{cn} are assumed to remain constant within a switching interval. The corresponding duty cycles for one mains period are plotted in Fig.4 (a). $d_{p1}(\phi_N)$ and $d_{n2}(\phi_N)$ follow a 120°-periodic triangular-shaped behavior. $d_{p2}(\phi_N)$ and $d_{n1}(\phi_N)$ equal zero and are not used for this idealized case. Actually these duty cycles are valid if the voltage across the smoothing inductors is neglected. Considering the voltage drop at L_{cn}, L_{cp} the duty cycle of the relevant sector $[0 \ldots \pi/3]$ modifies to (omitting the detailed calculation)

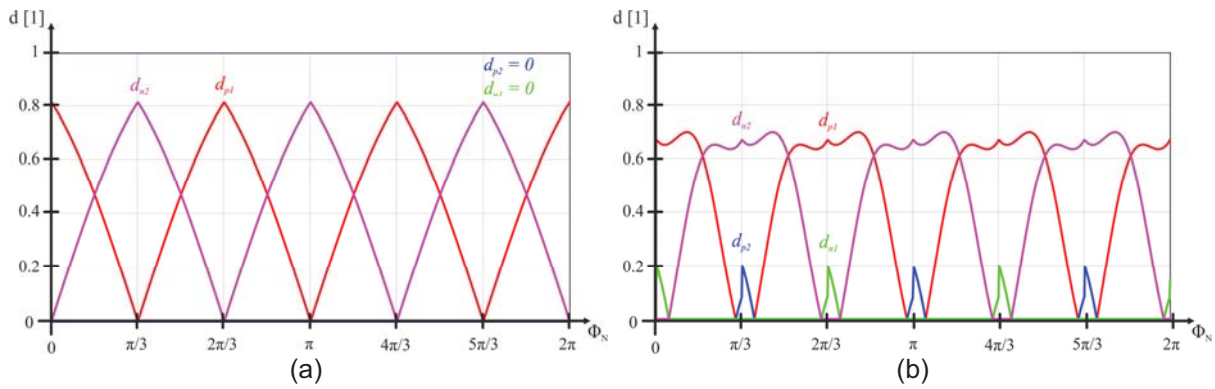


Fig.4: Duty cycle wave shapes for both NPC switching legs; (a) idealized case (neglected voltage drop across the smoothing inductors L_{cn}, L_{cp}); (b) duty cycle if actual voltage drop is considered.

$$d_{p1}(\phi_N) = -M \cdot \cos(\phi_N - \tfrac{5\pi}{6}) + \omega_N L_{cp} \cdot M \cdot \frac{P}{3\sqrt{3} \cdot \hat{U}^2} \cdot \sin(\phi_N) - \ldots$$

$$\ldots - 6 \cdot \frac{L_{cp}}{L_{DC}} \cdot M \cdot \left[\sin\left(\arccos\left(\tfrac{3}{\pi}\right)\right) - \tfrac{3}{\pi} \arccos\left(\tfrac{3}{\pi}\right) \right] \cdot \cos(6 \cdot \phi_N) \qquad (5)$$

where P denotes the output power. Hence, the inductor voltage drop significantly influences the switching of the cell. For intervals with $d_{p1} < 0$ the corresponding switch is turned-off during the whole switching period. The corresponding duty cycles of both NPC switching stages are shown in Fig.4 (b). d_{p1} and d_{n1} are the cycles for S_{p1} and S_{n1} whereas d_{p2} and d_{n2} are for switch S_{p4} and S_{n4}. Hence, $1 - d_{p1}$, $1 - d_{n1}$, $1 - d_{p2}$ and $1 - d_{n2}$ are the appropriate duty cycles for S_{p3}, S_{n3}, S_{p2} and S_{n2} (not plotted in Fig.4). It has to be noted that d_{p2} and d_{n1} now no longer appear to be zero. For increasing values of L_{cn}, L_{cp} both switches S_{p4} and S_{n1} more and more are involved; e.g., for $L_{cn} = L_{cp} = 6.3\text{mH}$ (as used in the analyzed system) d_{p2} reaches a peak duty cycle of 0.2.

2.2 Semiconductor Stress

<u>IGBT Voltage Stress</u>: Omitting switching transients the blocking voltage of all diodes and IGBTs of the NPC legs equals the DC link capacitor voltages U_{cp}, U_{cn}, being typically in the range 550…650VDC for a standard 400V mains. Including switching transients and safety margins hence 1000…1200V semiconductors are required. If, alternatively a T-type three-level branch is used, the “outer” semiconductor would be stressed to $U_{cp}+U_{cn}$, i.e., 1100… 1300V requiring 1700V semiconductors.

<u>Current Stress</u>: Current stress of switches and diodes has to be calculated for the design of the three-level NPC switching branch. Depending on the given current waveforms for i_{cp} in the section $\phi_N = [\pi/3 \ldots \pi]$

$$i_{cp}(\phi_N) = i_L(\phi_N) - i_p(\phi_N) = I_0 - \hat{I}_{L,ac} \cdot \sin(6\phi_N) - \hat{I} \cdot \cos(\phi_N - \tfrac{2\pi}{3}) \qquad (6)$$

(section interval shaded in Fig. 5), the zero-crossings Z of i_{cp} have to be calculated numerically. Consequently, the calculation of the rms and avg current ratings cannot be performed in an analytically closed manner, but have to be done numerically where also the corresponding duty cycles have to be taken into account. Furthermore, also the given waveform of $i_L(\phi_N)$ is an approximation, based on the fundamental ripple component. The converter output voltage U_o, the two DC-Link voltages $U_{cp} = U_{cn}$ and the switching frequency are supposed to remain constant for calculating the current stress of the applied semiconductors and passive components. The system parameters are given in Tab.1.

System Parameters		
Line to Line Mains Voltage	U_{LL}	400V
Mains Frequency	f_N	50Hz
DC-Choke	L_{DC}	2.25mH
Inductors	L_{cp}, L_{cn}	6.3mH
Switching Frequency	f_s	10kHz
Cell DC-Link Capacitor Voltages	U_{cp}, U_{cn}	600V
Output Power	P_o	10kW

Table 1: System parameters of the active three-phase rectifier topology.

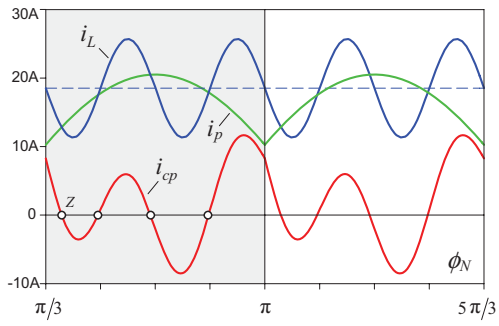


Fig.5: Current waveforms of i_p, i_L and of i_{cp} (interval [π/3…5π/3]).

As can be seen from Tab.2 each three-level bridge leg mainly operates as a two-level system, the three-level operation, however, is required for smooth current control at each 60° sector transition. It is evident, that the current ratings of the NPC leg components are not ”symmetrically” (i.e., equal for upper and lower part, as valid for, e.g., drive inverters) which might be seen as a drawback of the proposed concept. It is obvious from the given listing in Tab.2 that the NPC connected to the negative bus and the switching branch connected to the positive bus bar are stressed cross-symmetric. I.e., current stress of S_{n1} equals S_{p4}, whereas S_{n2} conforms S_{p3}, respectively. Depending on the calculated current and voltage stress, appropriate IGBTs and diodes for the system have been chosen, which would result in the fact that upper and lower semiconductor elements of each three-level bridge leg are of different rating/size leading to a specific power module. Nevertheless, standard three-level IGBT modules may be a cost-effective solution as they are used in high volumes in industry. The expected semiconductor efficiency of the total rectifier has been predicted to 98.9% (losses 104W) where passive components are not taken into account. The bidirectional switches are implemented by two series IGBTs with reverse diode. If reverse blocking IGBTs would be used, the semiconductor efficiency could be enhanced to 99%. It has to be noted that the losses of the standard passive three phase rectifier are approximately 41W and therefore highly inflict the total semiconductor efficiency.

NPC leg connected to		L_{cn}		L_{cp}	
		I_{avg}	I_{rms}	I_{avg}	I_{rms}
Switches					
	S_1	0.00A	0.00A	1.12A	2.74A
	S_2	0.72A	1.95A	3.37A	5.24A
	S_3	3.37A	5.24A	0.72A	1.95A
	S_4	1.12A	2.74A	0.00A	0.00A
Diodes					
	D_1	0.06A	0.62A	1.07A	2.58A
	D_2	0.06A	0.62A	1.07A	2.58A
	D_3	1.07A	2.58A	0.06A	0.62A
	D_4	1.07A	2.58A	0.06A	0.62A
Freewheeling Diodes					
	D_{1F}	0.72A	1.95A	2.25A	4.46A
	D_{2F}	2.25A	4.46A	0.72A	1.95A
Inductor currents					
		1.64A	6.18A	1.64A	6.18A
DC link capacitor currents					
	C_p, C_n		5.6A		5.6A

Table 2: Calculated current stress of the main system components.

2.3 Current Ripple

This section briefly discusses the design of both inductors L_{cp} and L_{cn} connected to the positive and negative bus bar of the passive three-phase rectifier system. The maximum peak-to-peak current ripple can be found for a duty cycle of 50% located close to $\pi/2$ and can be calculated to

$$\Delta i_{cp/cn,\max} = \frac{\frac{\sqrt{3}}{2}\hat{U}\cdot\left(1-\frac{M}{2}\right)}{f_s \cdot L_{cp/cn}} \tag{7}$$

Using, e.g., $\Delta i_{cp} = u_{L,cp}/L_{cp}\cdot\Delta t$ with $\Delta t = d_{p,1}\cdot T_s$ and $u_{L,cp}$ in the sector $[\pi/3\ldots 2\pi/3]$

$$u_{L,cp}(\phi_N) = U_c - u_p(\phi_N) + u_{h3}(\phi_N) = U_c - \hat{U}\cdot\cos(\phi_N - \tfrac{2\pi}{3}) + \hat{U}\cdot\cos(\phi_N)\,. \tag{8}$$

A mains voltage of $U_{LL} = 400\text{V}$ and a DC link voltage of $U_C = 600\text{V}$ results according to (4) in a modulation rate of $M = 0.94$. Assuming a peak-to-peak current ripple of 20% of the peak value of i_{cp} and a switching frequency of $f_S = 10\text{kHz}$ the required inductor value can be calculated to $L_{cp/cn} = 6.3\text{mH}$.

2.4 System Control

The control of the rectifier system is based on a cascade-like structure (Fig.6). It should be noted that as already mentioned no output voltage control is performed with this rectifier. As illustrated in Fig.6 in a first step the rectifier's average output power P_o is determined using measurement values of i_L and u_{rec} (output voltage of diode bridge). Based on P_o now a conductance value g_e can be calculated which is used for generating reference values for the diode rectifier output currents, i.e., $i_p^* = g_e\cdot u_{pos}$ and $i_n^* = g_e\cdot u_{neg}$, respectively. The duty cycles of the NPC legs finally are defined by two PI-type current controllers $G_p(s)$, $G_n(s)$ based on the sensed output currents i_p, i_n of the diode bridge using further a voltage feed-forward to improve the control characteristic. As the NPC switching stage only influences i_{cp}, i_{cn} the current i_L has to be taken into account as a disturbance quantity for the current loop. Next to current control also the DC link voltages U_{cp} and U_{cn} have to be controlled. This can be performed using a superimposed voltage controller with slow dynamic (not shown in Fig.6). The control of the DC link voltages is, however, not further discussed here.

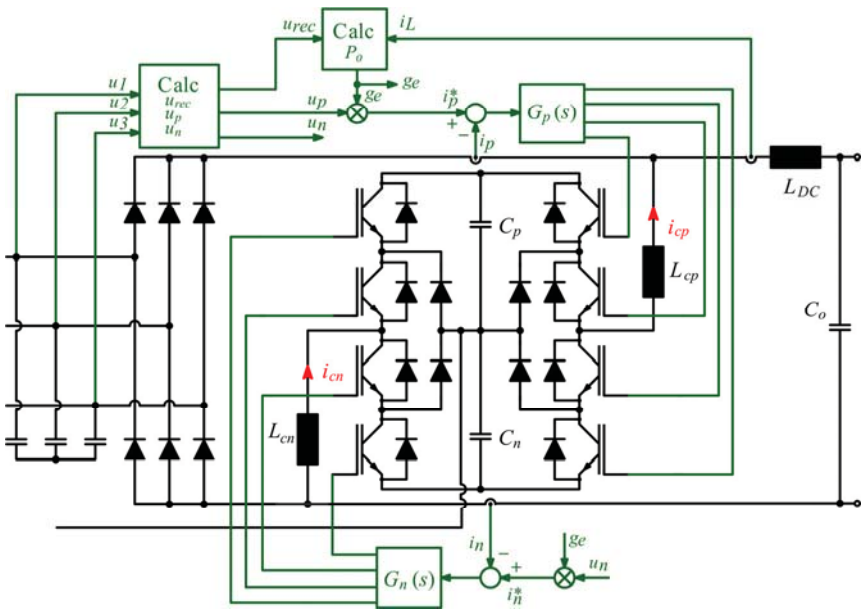


Fig.6: System control of third harmonic injection employing two three-level NPC switching branches.

3. Simulation Results

Operation of the novel rectifier system has been verified by simulation of a 10kW system according to the parameters given in Tab.1 using the PLECS simulation software. AC-side filtering capacitors of $C_F = 6.8\mu\text{F}$ in star-configuration have been used and an output capacitor of $C_o = 1000\mu\text{F}$ is used to achieve a low output voltage ripple of $\Delta U_{o,pp} \approx 8\text{V}$. The simulated voltage and current characteristics are given in Fig.7. Figure 7 (a) illustrates the diode bridge output currents i_p, i_n and the injection current i_{h3} which are "combined" to the aimed input currents i_{N1}, i_{N2}, i_{N3} at the AC side of the diode bridge (cf., Fig.7 (a)) resulting after filtering by C_F in sinusoidal mains currents in phase to the mains voltages u_{N1}, u_{N2}, u_{N3}. The input filter C_F also has to smooth current peaks originating from the commutation of the switches $S_1 \ldots S_3$ every 60° interval transition. Figure 7 (b) demonstrates the good transient behavior of the system, shown for a 10kW to 7kW output power load step.

4. Conclusion

A novel approach for improving the mains current quality of standard three-phase diode bridge rectifiers with DC side smoothing inductor as widely used in industry, especially in drive systems has been proposed. The system is based on the third harmonic injection principle using a current injection stage and three bidirectional low-frequency gated semi-conductor switches to the AC input. The current injection stage is implemented using two three-level neutral point clamped IGBT bridge legs in order to minimize the current distortions at the 60° sector transitions. Simulation results verify the good performance of the proposed system for stationary operation (THDi < 5%) as well as for load transients. The proposed topology advantageously also can be used realizing an optional extension module for upgrading a standard diode bridge rectifier. The advantage in comparison to "full" active three-phase rectifiers is that the proposed system requires less installed semiconductors (injection stage has to handle significant lower currents), however does not provide output voltage regulation.

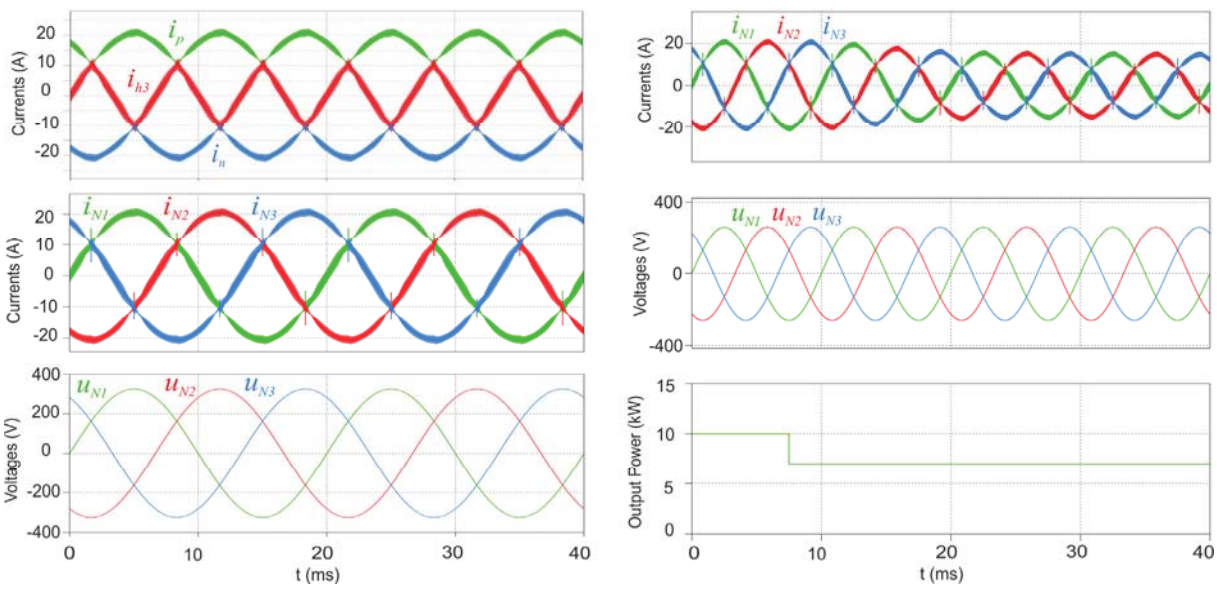


Fig.7: (a) Simulated stationary operation of the proposed rectifier; diode bridge output current and injection current (top), resulting mains currents (middle) in phase to mains voltage (bottom). (b) Simulated transient load step from 10kW to 7kW DC output power.

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