IWN 2014

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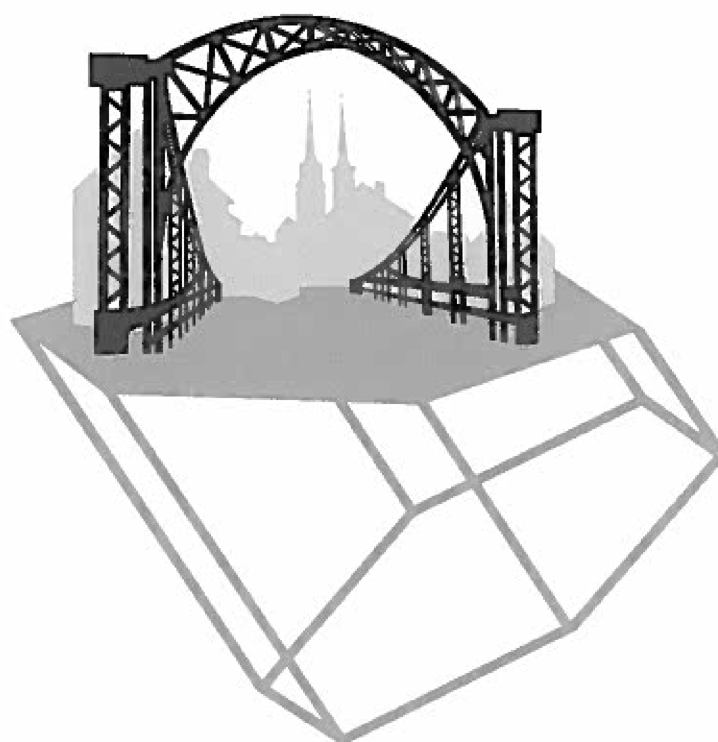
AUGUST 24-29, 2014



18:15–18:30 | MoEO12

Peter Lagger
Understanding the Fundamental Limitations for the Improvement of Forward Gate Bias Induced Vth Drift Stability of GaN based MIS-HEMTs.

P. Lagger (1,2), M. Reiner (1), G. Denifl (1), M. Stadtmueller (1), D. Pogany (2) and C. Ostermaier (1)

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2. TU Wien, Institute of Solid-State Electronics, Wien, Austria

WORKSHOP O: Optical Devices

SESSION Opto 1 – LED I
Chair: Shuji Nakamura // Multi-purpose Hall

Time *Presentation Code*

14:00–14:30 | MoOI1 (invited)

Bastian Galler
Droop effects limiting efficiency in high brightness LEDs.

OSRAM OS, Regensburg, Germany

14:30–15:00 | MoOI2 (invited)

Francesco Bertazzi
Auger processes in InGaN/GaN LEDs: full-band modeling experiments.

F. Bertazzi (1,2), M. Goano (1,2), X. Zhou (1), M. Calciati (1), G. Ghione (1), M. Matsubara (3), E. Bellotti (3)

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2. ECE Department, Boston University, Boston, U.S.A.

15:00–15:15 | MoOO3

Dmitry Zakheim
Two-level design of high power blue LED chips based on AlGaInN heterostructure with suppressed efficiency droop.

Dmitry A. Zakheim (1,2), Grigoriy V. Itkinson (2), Mikhail V. Kukushkin (2), Lev K. Markov (1,2), Oleg V. Osipov (2), Alexey S. Pavluchenko (1), Irina P. Smirnova (1,2), Dmitry A. Bauman (3)

1. Ioffe Institute, St.-Petersburg, Russia
2. NTL Innovation LLC, St.-Petersburg, Russia
3. Svetlana Optoelectronics JSC, St.-Petersburg, Russia

15:15–15:30 | MoOO4

Michael Wallace
Simultaneous optical and induced current mapping of InGaN LEDs with different quantum barrier growth temperature.

Understanding the Fundamental Limitations for the Improvement of Forward Gate Bias Induced V_{th} Drift Stability of GaN based MIS-HEMTs

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Motivation The high number of defect states at the dielectric/III-N interface (shortly interface) in GaN based MIS-HEMTs causes tremendous V_{th} drifts (ΔV_{th}) and is the most severe challenge for the development of normally-off MIS-HEMT devices. Recent studies revealed a broad distribution of stress/recovery time constants for different dielectric materials [1, 2, 3]. In this work, we show that the magnitude and dynamics of ΔV_{th} is mostly determined by the electrostatic properties of the gate stack and the measurement conditions itself. Subsequently, we conclude that the density of interface states is much larger than what can be measured electrically. Therefore, the interface quality has only a minor influence on ΔV_{th}. We reveal that the measured ΔN_{it} values, i.e. the number of trapped electrons at the interface per unit area due to $V_G > 0$ stress, vary over more than two orders of magnitude by solely varying the layer thicknesses on wafers sharing the same interface quality. The major role of electrostatics is further proved by the scaling of ΔN_{it} with the dielectric constant k.

Experiments The measurement is based on the monitoring of the transient recovery of ΔV_{th} after stress pulses with a magnitude of $V_G = V_{G,stress}$ and a duration of t_s [2, 3]. Wafers with varying dielectric and III-N barrier thickness, t_D and t_B respectively, are compared, cf. Tab. 1. For all wafers the same deposition process for the SiN_x dielectric is used and hence the interface quality is equivalent. The test devices have a gate length and width of 1.3 μm and 480 μm, respectively. Fig. 1 reveals a strong increase of ΔV_{th} and ΔNit for increasing t_B under the same stress conditions. The connection between ΔV_{th} and ΔN_{it} is given by (1). In Fig. 2, ΔV_{th} and ΔN_{it} are compared for wafers with varying t_D, showing an opposite trend compared to the t_B variation. Fig. 3 shows a nearly constant ΔV_{th} for different dielectric materials, i.e. varying dielectric constant k, for the same stress conditions, while ΔN_{it} increases with k.

Discussion The large-signal equivalent circuit model of the gate stack [3, 4] is used to explain the experimental results, cf. Fig. 4a. Fig. 4b shows the bandstructure of the gate stack for $V_G > 0$, where the barrier potential Φ_B is decreased by V_B. Values for V_B/V_G according to (2) are given in Tab. 1. Fig. 5 shows the ΔV_{th} data of Fig. 1-2, where the V_G-axis is scaled by V_B/V_G. This clearly demonstrates the role of the barrier (V_B) for the charging of the interface. Fig. 5b shows that ΔN_{it} for wafers 1-3 is very similar, while the ΔN_{it} of wafer 5 is significantly lower and wafer 4 shows a transition from low to high ΔN_{it}. The deviation of wafer 4-5 could be due to the down-scaling of the dielectric electrical field strength E_D with increasing t_D, which might influence the trapping behavior at the interface. Interestingly, the increase in ΔN_{it} with k in Fig. 3b is compensated by the decreasing $\Delta N_{it}/\Delta V_{th}$ (cf. Tab. 1) and ΔV_{th} is nearly constant Fig. 3a. This is explained by the increase of V_B/V_G with k, cf. (2).

Conclusion Our results indicate that ΔV_{th} is mainly influenced by the change of the barrier potential V_B, because the interface density is still too high to have a significant impact. In [1], a ΔN_{it} improvement by a factor of 2 for different deposition processes is observed, while we demonstrate that simple t_D variations change ΔN_{it} by more than two decades. The V_{th} drift increases with V_G and t_s, which further suggests that the upper limit for ΔV_{th} is set by the stress and measurement conditions itself [2, 3]. A fundamental limit of the electrical measurement is given by $(k \cdot E_{crit})/q < \Delta N_{it,max}$, where E_{crit} is the critical electric field strength for the dielectric breakdown [3]. Moreover, the model in Fig. 4a implies that $\Delta V_{th} \leq V_{G,stress}$, because the distribution of V_G is distributed to the dielectric with ongoing stress [3]. The observations described in this paper are crucial for the interpretation of ΔV_{th} and ΔN_{it} data.

[1] W. Choi et al., IEEE EDL, Vol. 35, No. 1, 2014
[2] P. Lagger et al., Proc. of the IRPS 2014
[3] P. Lagger et al., IEEE Tr. on Electron Dev., online, 2014
[4] J. R. Jameson et al., IEEE TED, Vol. 53, No. 8, 2006

Wafer	t_D [nm]	t_B [nm]	V_B/V_G	$\Delta N_{it}/\Delta V_{th}$ [cm^{-2} V^{-1}]
1	25	21	0.40	$1.55 \cdot 10^{12}$
2	10	10	0.44	$3.87 \cdot 10^{12}$
3	25	10	0.24	$1.55 \cdot 10^{12}$
4	40	10	0.16	$9.67 \cdot 10^{11}$
5	75	10	0.09	$5.16 \cdot 10^{11}$

Tab. 1. Overview of wafers with a SiN_x dielectric (k = 7) used for the experiments with varying dielectric thickness t_D and barrier thickness t_B. In addition, the change of the barrier potential V_B normed to the applied gate bias V_G and $\Delta N_{it}/\Delta V_{th}$ are given. $\Delta N_{it}/\Delta V_{th}$ is used for the translation of the measured ΔV_{th} values to equivalent ΔN_{it}. It is a measure for the sensitivity of the gate stack to changes of the interface charge density $q \cdot \Delta N_{it}$. The values are calculated using (1) and (2). All samples have an AlGaN barrier with an Al-content of 20%. All wafers have the same buffer structure. Further, the wafers 2-5 have the same barrier structure. All wafers share the same process for SiN_x deposition.

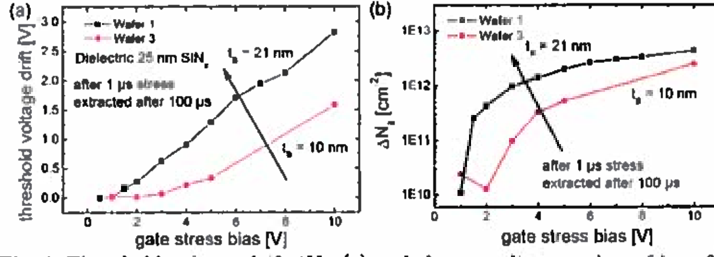

Fig. 1. Threshold voltage drift ΔV_{th} (a) and the according number of interface trapped charges ΔN_{it} (b) are compared for different barrier thickness t_B of 10 nm (wafer 3) and 21 nm (wafer 1) for varying gate stress bias $V_{G,stress}$ and constant stress time t_s = 1 µs.

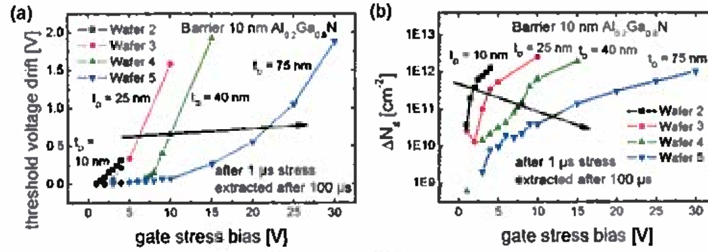

Fig. 2. Impact of the dielectric thickness t_D on ΔV_{th} (a) and ΔN_{it} (b) for wafers 2-5 for varying gate stress bias $V_{G,stress}$ and constant stress time t_s = 1 µs.

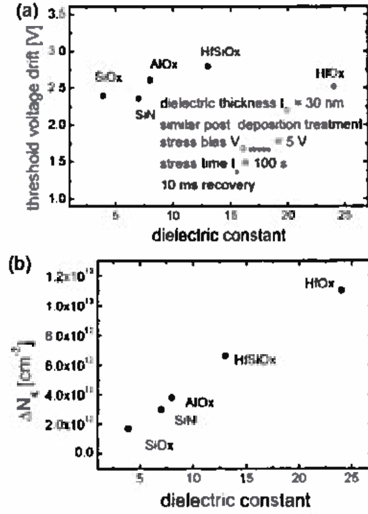

Fig. 3. Influence of the dielectric constant k on ΔV_{th} (a) and ΔN_{it} (b) under the same stress conditions for comparable wafers. The thickness of the dielectric is 30 nm.

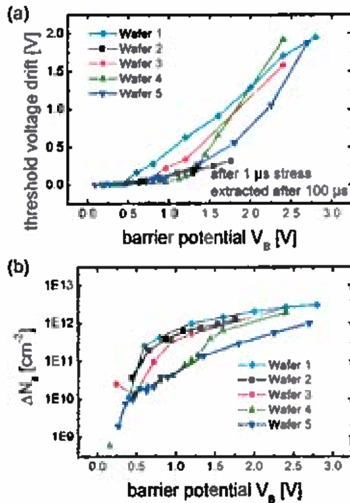

Fig. 5. ΔV_{th} (a) and ΔN_{it} (b) data from Fig. 1 and Fig. 2 plotted as a function of the barrier potential V_B, cf (2).

$$(1)\ \Delta V_{th} = q \cdot \Delta N_{it}/C_D$$

$$(2)\ V_B/V_G = C_D/(C_D+C_B)$$

Formulas: ΔV_{th} is the threshold voltage drift, q is the elementary charge, ΔN_{it} is density of electrons trapped during electrical stress with a gate bias $V_G > 0$, C_D and C_B are the dielectric and barrier capacitances, V_B is the change of the barrier potential for $V_G > 0$.

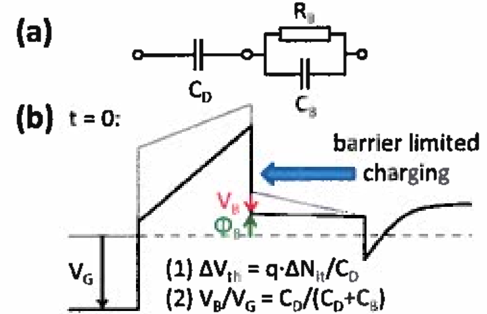

Fig. 4. (a) Equivalent circuit model of the gate stack, where C_D and C_B are the dielectric and barrier capacitances and R_B is the barrier resistance. R_B models the transport of electrons from the 2DEG channel to the interface [2, 4]. R_B decreases with increasing V_B, due to e.g. thermionic emission. (b) Distribution of the applied gate bias $V_G > 0$ to the dielectric and the barrier according to this model. The barrier potential Φ_B, i.e. the conduction band minimum of the barrier at the interface with respect to the Fermi-level, is changed by V_B due to the applied gate bias V_G. Although the model gives a first-order qualitative understanding, further effects may play a role, like e.g. pinning of the barrier potential due to a dominant defect level or due to spill-over (accumulation of a second channel at the interface). In addition, also the field in the dielectric may play a role for the stress/recovery dynamics.