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Different layer designs for normally-off GaN HEMTs with ultrathin AlN barrier, GaN cap and in situ SiN passivation

M. Capriotti[1,*], A. Alexewicz[1], C. Fleury[1], J. Derluyn[2], D. Visalli[2], D. Pogany[1] and G. Strasser[1]
[1] *Institute of Solid State Electronics, Vienna University of Technology, 7a Floragasse, 1040 Vienna, Austria*
[2] *EpiGaN, Kempischesteenweg 293, 3500 Hasselt, Belgium*
* E-mail: mattia.capriotti@tuwien.ac.at

ABSTRACT

In this work we present two novel designs for GaN HEMTs with ultrathin AlN barrier, unintentionally doped (UID) GaN cap and in situ deposited SiN passivation and we show that by accurate tuning of the barrier and GaN cap thicknesses it is possible to produce devices with low access resistance, high transconductance and normally-off capability.

I. INTRODUCTION

GaN-based high electron mobility transistors (HEMTs) with ultrathin AlN barrier layer are attractive because they allow normally-off operation combined with high performance [1]. For normally-off operation the high density of polarization charges of AlN needs to be compensated, by reducing the barrier thickness down to 1.5-2 nm and by the inclusion of a cap layer. Among the possible cap layer materials (e.g. InGaN, n+ GaN, p+ GaN), unintentionally doped (UID) GaN has shown to be effective for threshold voltage tuning [2]. Low access resistance can be preserved by deposition of a passivation which provides favorable surface conditions to preserve the electrons in the 2DEG [3]. At the same time it has been shown that the selective removal of the in situ SiN passivation below the gate contact leads to a complete depletion of the 2DEG below the gate. In this work we present two novel designs for GaN HEMTs with ultrathin AlN barrier, UID GaN cap and in situ deposited SiN passivation and we show that by accurate tuning of the barrier and GaN cap thicknesses it is possible to produce devices with low access resistance, high transconductance and normally-off capability.

2. DEVICE FABBRICATION

We processed the devices on MOCVD-grown heterostructures on silicon substrate. Two heterostructures are involved in this work: type 1 and type 2. Type 1 is composed by an AlN/AlGaN buffer, 150 nm GaN channel, 2 nm AlN barrier and 2 nm GaN capping layer. Type 2 heterostructure is composed by comparable buffer and channel layers to type 1 but different thicknesses of the AlN barrier and the GaN capping layer, which are 1.5 nm and 6 nm respectively. Both types 1 and 2 are passivated *in situ* with 50 nm of SiN within the reactor at the end of the growth. All processed devices are schottky barrier (SB) HEMTs with Ni/Au gate contacts and Ti/Al/Ni/Au ohmic contacts.

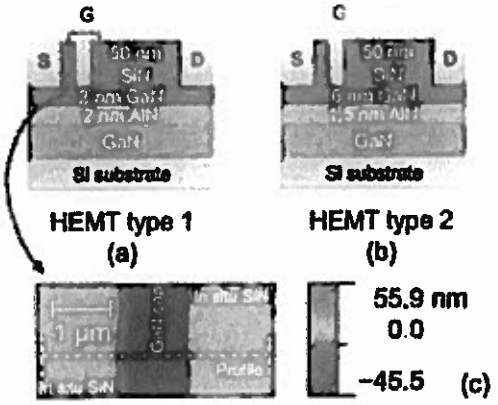

Figure 1: (a) Schematic drawing of a HEMT type 1. (b) Schematic drawing of a HEMT type 2. (c) AFM micrograph of a gate trench after full removal of the in situ SiN passivation layer.

The schematic representations of the schottky barrier (SB) devices processed on heterostructure type 1 and type 2, are shown in figure 1a and 1b. The *in situ* passivation layer has to be removed prior to deposition of ohmic and gate contacts in both types of devices. We selectively removed the *in situ* passivation layer with a two step dry etching recipe based on SF_6. The first 30 nm of the in situ SiN are removed by reactive ion etching (RIE).

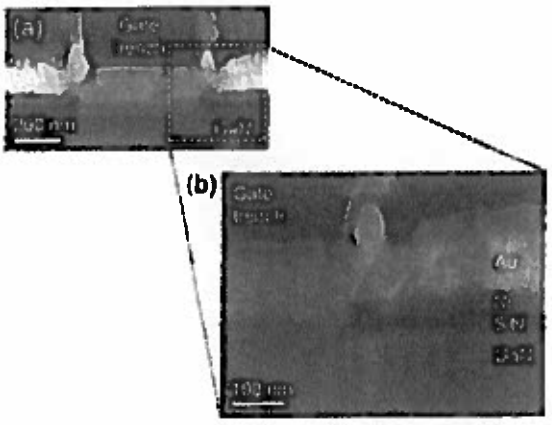

Figure 2: (a) Micrograph of the gate region of a SB-HEMT processed on type 1 heterostructure acquired by scanning electron microscopy (SEM). (b) Detail from figure 2a acquired at higher magnification. From the image it is clearly visible that the *in situ* SiN was completely removed from the gate region.

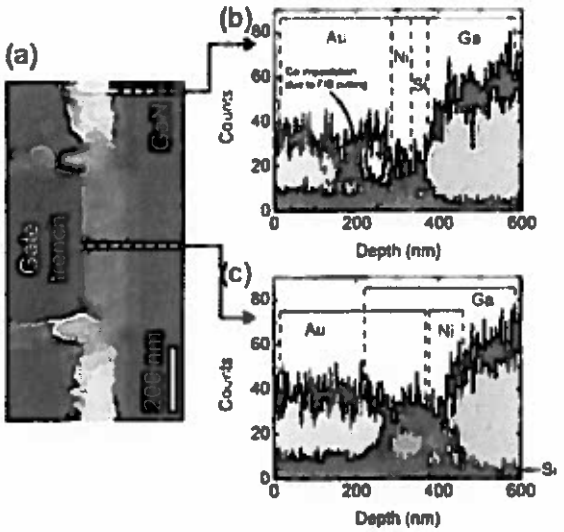

Figure 3: (a) SEM Micrograph of the gate region of a type I HEMT. The two white dashed lines underline the line scanned with the electron beam for EDX spectroscopy. (b) EDX spectrum acquired in the access region of a type I HEMT. The Silicon signal is clearly visible between the Ni peak and the main Ga peak. (c) EDX spectrum acquired in the gate trench of a type I HEMT. Si is not detected in this area.

The residual 20 nm of the passivation are etched by inductively coupled plasma (ICP) in order to minimize the surface damage. The gate trench is analyzed directly after SiN removal with atomic force microscopy (AFM) (see Fig 1c). From the AFM micrograph a gate trench depth of approximately 50 nm is extracted. The AFM results confirm that *in situ* SiN is completely removed. In order to further demonstrate the complete removal of the *in situ* nitride layer, the gate area of a type I HEMT (see fig 2) is milled by a focused Ga ion beam (FIB) and the cross-section of the gate area is analyzed by Energy Dispersive X-ray spectroscopy (EDX). By comparison of the EDX spectra from the access region and the gate trench of the device under analysis it is clear how the Si peak attributed to *in situ* SiN passivation is clearly visible in the first one and it not detected in the second one (see fig 3).

3. RESULTS AND DISCUSSION

The produced devices are characterized in DC and pulse conditions. During the pulsed measurements only the gate is pulsed with pulse width of 100 ns and pulse period of 100 µs. In figure 4a and 4b we show typical DC and pulse characteristics of a HEMTs type I. The device shows a maximum output current of 0.6 A/mm with a maximum transconductance of 140 mS/mm and a slightly negative threshold voltage (V_{th}) of -0.5 V. For the devices processed on the heterostructure type I, the thickness of the GaN capping layer is too thin in order to effectively counter-balance the high polarization of the AlN barrier and provide a positive V_{th}.

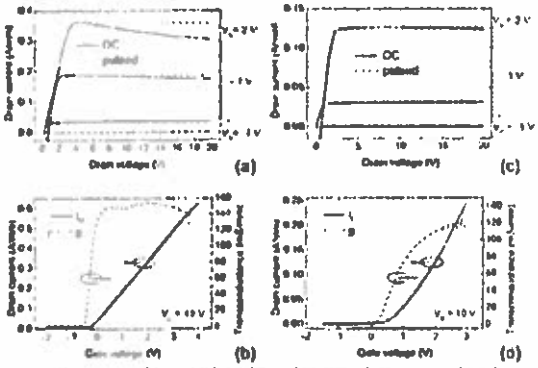

Figure 4: (a-b) DC and pulse characterizations of a HEMT type 1. (c-d) DC and pulse characterizations of and HEMT type 2. In both type 1 and type 2 devices the source to drain distance is 15 µm.

Devices processed on a heterostructure type 2, with a thicker GaN cap and thinner barrier shows a maximum output current of 0.25 A/mm, with a transconductance peak of 120 mS/mm and a positive V_{th} of 0.5 V (see Fig 4c and 4d). The decrease in the maximum transconductance is due to the increased thickness of the GaN capping layer. As we expected increasing the thickness GaN capping layer and reducing the barrier thickness AlN barrier leads to an increase in the V_{th}, which allows normally off operation.

4. CONCLUSIONS

We produced SB-HEMTs based on two novel heterostructure designs with high polarization AlN barrier. Combining inclusion of an UID GaN capping layer [2], selective removal of an *in situ* deposited SiN passivation [1,2] we were able to reach normally off operation maintaining low access resistance and high transconductance.

ACKNOWLEDGMENT

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18:00-20:12	**OPTOELECTRONIC DEVICES**	
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18:00	**Polaritonic Devices (invited)**	**Pavlos Savvidis**
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19:24	Impact of contact patterning on light extraction in AlGaN/InGaN/GaN light-emitting diodes	I. Khmyrova
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