ESD Characterization of Germanium diodes

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Abstract – Germanium (Ge) as a high mobility channel material is an option for future PMOSFET for sub 14 nm node. This work presents the ESD robustness of planar Ge diodes on *Silicon-on-Insulator* (*SOI*) and *bulk* Si substrate. They show a reduced I_{t2} with a remarkably improved clamping behavior compared to Si diodes, which is attributed to the intrinsic material properties of Germanium.

I. Introduction

A silicon based FinFET device architecture is used in today's most advanced CMOS technology node [1]. FinFET devices show an improved leakage and short channel control compared to planar *bulk* or *PDSOI* devices. To keep the technology scaling pace, alternative channel materials, like e.g. compressive strained SiGe or Ge for PMOS and III-V materials or tensile strained Ge for NMOS are considered. Besides changes in channel material other device architectures like Gate-All-Around devices (GAA) are considered, in combination with new channel materials [1].

Each change in device architecture or channel material can potentially impact the intrinsic ESD performance of a technology. The ESD robustness of silicon FinFET devices have been studied in *SOI* [3] and *bulk* [4] CMOS technologies. The impact on the ESD robustness by introducing a SiGe quantum well in the channel of a planar device and SiGe clad around Si FinFET ggPMOS have been studied in [5] and [6], respectively. The quantum well increases the I_{t2} for silicided ggPMOS devices due to intrinsic current inhibition, which acts as ballasting of the device. Gated diodes show a small decrease in performance due to the smaller band gap of the SiGe, compared to silicon. The first planar Ge ggPMOS TLP data was shown in [5] on a prototype technology. A promising improvement of the Ge ggPMOS I_{t2} has been observed compared to a silicided silicon reference.

In this work, an in-depth study of the ESD performance of planar diodes in Ge technologies is carried out. The impact of the material change from Si to Ge on ESD behavior is reported. Section II briefly describes the technologies used. In Section III the diode characterization will be presented together with the analysis of the data. In Section IV, a model is proposed for the response of Ge under ESD conditions. The main conclusions of this work are drawn in Section V.

II. Technologies

Two technologies are considered in this work. Both technologies contain an unstrained (fully relaxed) epitaxially grown Germanium layer. Junctions are formed using the classical implant and anneal scheme. All tested devices have been manufactured with fully CMOS compatible processes.

Technology 1 is a *Silicon-on-Insulator* (*SOI*) technology for integrated optical interconnects [6]. In this technology a 300 nm thick undoped Ge film is locally epitaxially grown on top of the silicon, see Figure 1. P+/ nwell and n+/ pwell diodes with equivalent doping profiles are made in SOI and Ge on SOI. Diodes with the same geometry exist for Si and Ge.

For Si devices a Nickel silicide (NiSi) is formed that lowers the contact resistance. No Nickel Germanide (NiGe) is present for Ge devices in *technology 1*. To form a NiSi and NiGe contact alloy in one process module is not possible, because the preclean chemistry that is used for NiSi process, recesses Ge severely. A separate module would add process complexity and costs.

Figure 1 SEM of *technology 1*: *SOI* technology with local epitaxially grown Ge islands.

Technology 2 is a 65 nm *bulk* Ge CMOS technology with 300 nm thick undoped Ge channel, see Figure 2. The Ge layer is formed by first etching the silicon after the STI processing, followed by an epitaxial Ge regrowth in the etched regions. This technology only enables Ge devices. Therefore a germanidation module to lower the contact resistance of the devices, can be used in *technology 2*. With this process module, a NiGe alloy layer is formed on the wafer, equivalent to the silicidation process in Si technologies. In this technology, Gated and STI diodes are available.

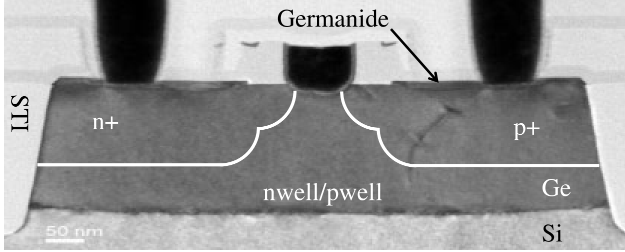

Figure 2 TEM of Ge gated diode on *technology 2* (*bulk*) with epitaxially grown Ge and NiGe formed.

III. Measurements

For TLP characterizations, the HANWA W5000 TLP tester is used with 200 ps rise time and pulse length of 100 ns or 500 ns. For on-wafer HBM characterizations HANWA W5000M system is used. The failure level is judged on a minimum of 10 % leakage increase at 1 V reverse bias.

This chapter is split in five sections. In section A, a direct comparison of TLP characterizations of Si and Ge planar gated diodes is performed for *technology 1* (*SOI*). In section B, the effect of layout variations is reported for Si and Ge in *technology 1*. Afterwards, the impact of different process changes on Ge diode behavior is discussed in section C. Before summarizing all TLP observations in section E, STI diodes, provided by *technology 2* (*bulk*), are studied in detail in section D.

A. Si vs. Ge diodes in *technology 1* (*SOI*)

Figure 3 and Figure 4 show the overlay of the forward and reverse biased TLP IV curves for a fixed diode dimension (L and W), using different materials. The observed failure current in forward TLP of Ge diodes are around 30% lower compared to the Si diode counterparts. Three key observations are made. First, Ge diodes have a 1000 x higher leakage current. This is due to the smaller band gap of Ge (0.66 eV) compared to Si (1.12 eV) [8]. The reverse bias TLP IV curves, Figure 4, show only a breakdown voltage (V_{BR}) shift. The observed shift can be explained by the band gap offset between Ge and Si plus an additional difference in background doping [9],

$$V_{BR} \cong 60 \cdot \left(\frac{E_g}{1.1}\right)^{\frac{3}{2}} \cdot \left(\frac{N_B}{10^{16}}\right)^{-\frac{3}{4}}, \qquad (1)$$

where E_g is band gap and N_B is background doping in cm^{-3}. The regular breakdown behavior rules out crystalline defects as root cause of the increased leakage level of Ge.

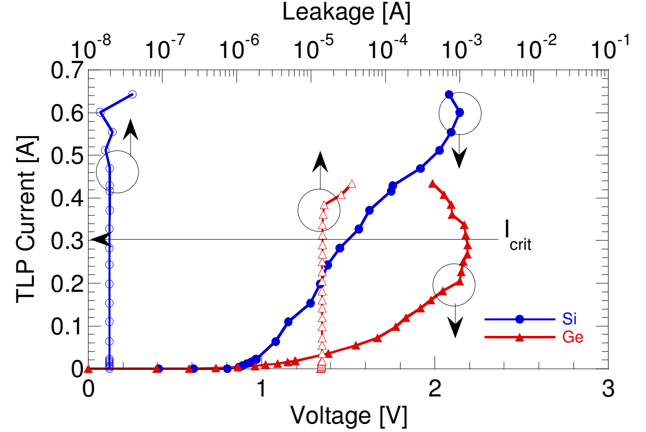

Figure 3 Forward biased TLP (100 ns) measurement of Si diode with NiSi vs. Ge diode without NiGe (W=50 µm, L=200 nm).

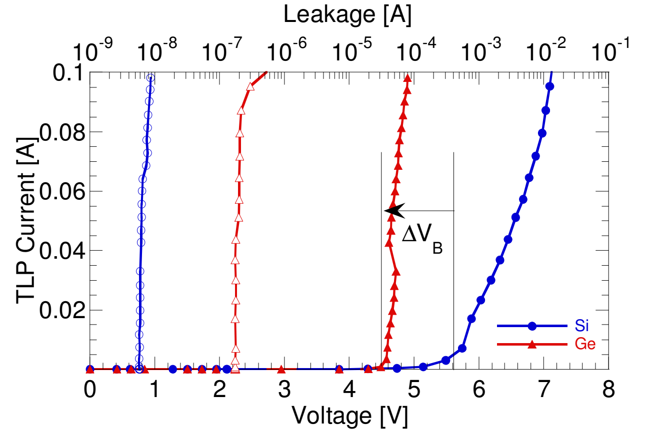

Figure 4 Reverse biased TLP (100 ns) measurement of Si diode with NiSi vs. Ge diode without NiGe (W=50 µm, L=200 nm).

A second observation is the resistance at low TLP current (<0.1 A) is higher in Ge compared to Si. This can be explained by the presence of NiSi in the Si diode. This reduces the contact resistance to the N+/P+ doping while the absence of NiGe in Ge diode leads to high series resistance. The third observation is that the differential resistance in the Ge diode gets lower with increasing TLP current contrary to Si. At a critical current level, I_{crit} in Figure 3, the device has a zero differential resistance.

Since this high current differential resistance lowering of Ge is unique, it is required to check if the Ge device survives the high current differential resistance lowering induced by TLP stress, excluding gradual degradation effects. This is done by repeated TLP sequences on the same Ge diode sample. The first two runs has been stopped before fail current was reached. These result are overlaid in Figure 5. All three runs are on top of each other with no leakage increase. This confirms that the high current differential resistance lowering for Ge diodes is not causing damage to the device.

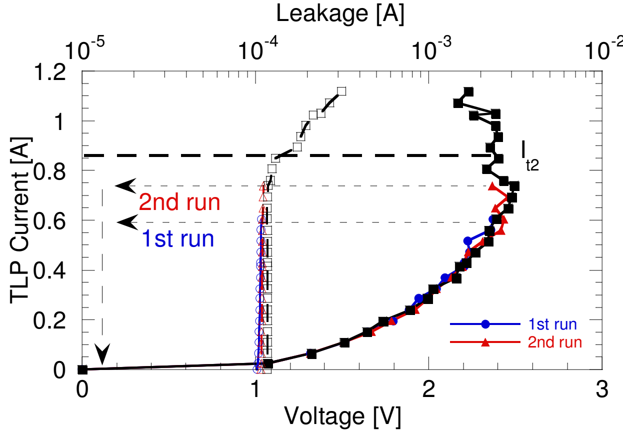

Figure 5 Repeated TLP sequence of same Ge diode sample without NiGe (W=100 µm, L=200 nm).

B. Diode layout variation in *technology 1* (*SOI*)

Figure 6 to Figure 9 show the TLP IV curves for Si and Ge forward biased diodes realized in the *SOI* based technology with different geometries. For all characterized diodes in *technology 1* the anode and cathode contact area consists of 5 contact rows.

Figure 6 and Figure 7 show TLP IV curves as a function of anode to cathode spacing (L), with a fixed junction width (W) for Si and Ge, respectively. The anode to cathode spacing (L) is varied from 100 nm to 1 µm. For Si, the on resistance increases with L and above 500 nm a selfheating induced resistance increase is visible in Figure 6. For Ge, the high current differential resistance lowering is present for all L variations. I_{crit} is independent of L and the differential resistance gets zero at current density J_{crit} of 6 mA/µm. (see Figure 7).

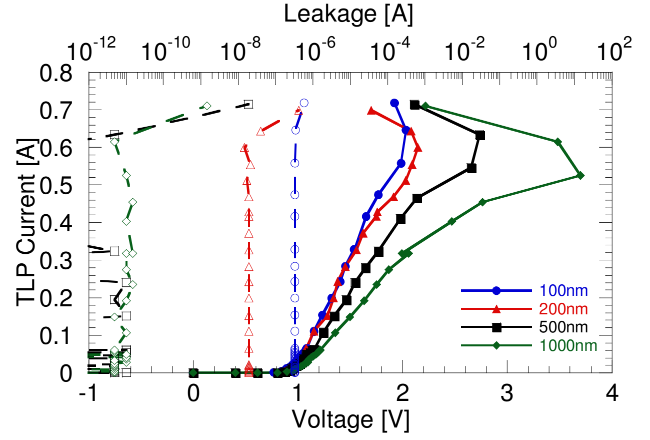

Figure 6 TLP (100 ns) measurement of L variation of Si diodes with NiSi (W = 50 µm).

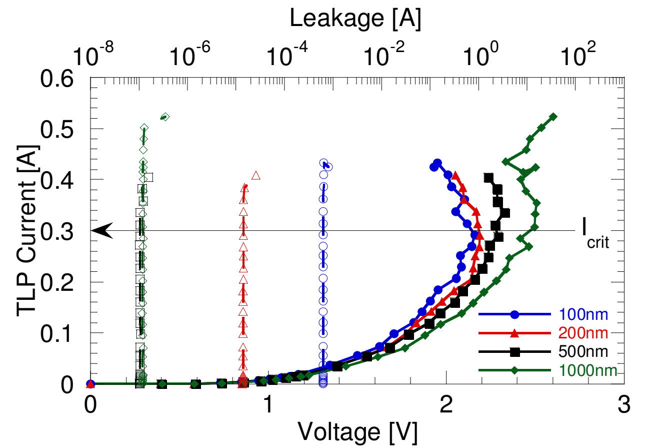

Figure 7 TLP (100 ns) measurement of L variation of Ge diodes without NiGe (W=50 µm).

For Si and Ge diodes, the failure voltage, $V_{t2,}$ increases with L. L increases the layout defined series resistance component of the device,

$$U = U_{pn} + I\left(R_s \frac{L}{W} + R_c\right), \quad (2)$$

where U is the voltage drop over the diode, U_{pn} is the voltage over the junction, R_s is the sheet resistance of and R_c is the contact resistance.

For Ge diodes, up to L=500 nm a negative differential resistance was observed above I_{crit}, while I_{t2} stays constant. For L>500 nm, the differential resistance stays zero above I_{crit} and I_{t2} increases. For this geometry the Ge related resistance lowering cannot compensate the series resistance and no negative differential resistance was observed. This might explains why this diode can survive higher current levels.

Figure 8 and Figure 9 show the variation of junction width (W) for Si and Ge. The range of junction width (W) variation is 25 µm to 100 µm. For Si, shown in Figure 8, the on resistance reduces with W and at W=25 µm the selfheating induced differential resistance increase is visible. For Ge diodes, see Figure 9, the high current differential resistance lowering is present for all W variations. The low current on-resistance (<0.1 A) reduces with W.

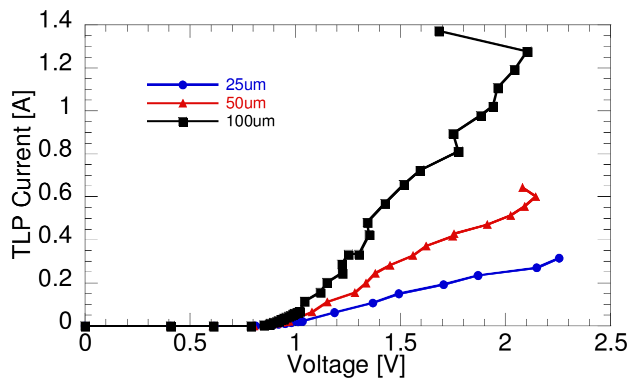

Figure 8 TLP (100 ns) measurement of W scaling of Si diodes with NiSi (L=200 nm).

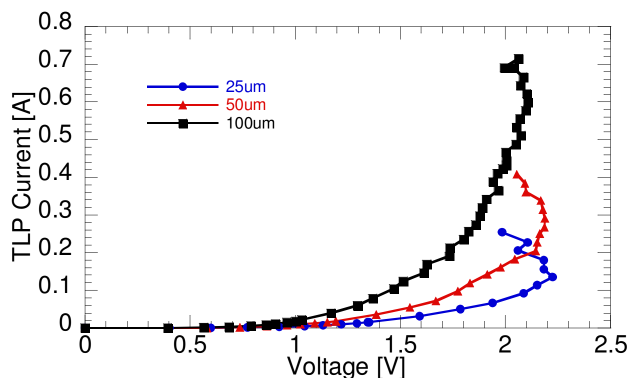

Figure 9 TLP (100 ns) measurement of W scaling of Ge diodes without NiGe (L=200 nm).

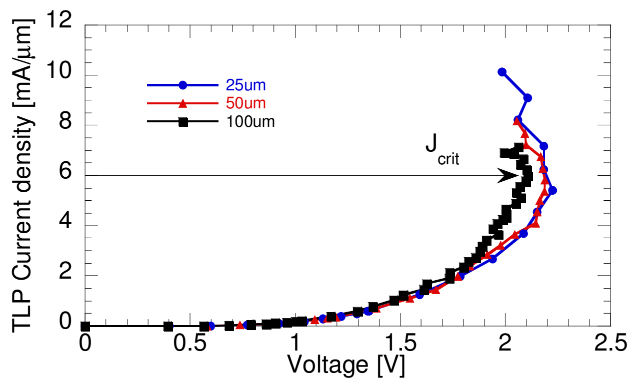

Figure 10 Normalized TLP IV (100 ns) of Ge diodes for different W without NiGe (L=200 nm).

The overlay of the normalized TLP IV curves of the W variation, Figure 10, illustrates that J_{crit} is independent of W at 6 mA/µm. I_{t2}/µm get smaller with increasing W. This could indicate a non uniform failure mechanism.

C Impact of process changes on Ge diode IV

Three process changes are studied addressing: *SOI* substrate doping type, junction implant energy and contact resistance lowering by germanidation.

In Figure 11, TLP IV curves of Ge diodes with n- or p-doped *SOI* films are overlaid. No change in TLP IV curve is observed by changing the doping of the silicon substrate (*SOI*) from n- to p-type. Hence the mechanism that leads to lowering of the high current differential resistance occurs only in the Germanium layer.

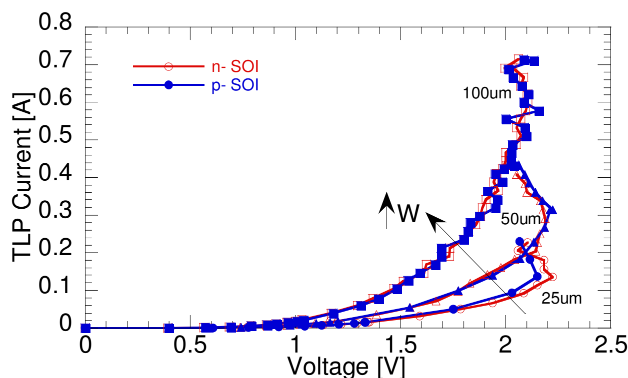

Figure 11 TLP (100 ns) measurement of W scaling of Ge diodes with n- and p- *SOI* substrate without NiGe (L=200 nm).

Figure 12 illustrates the modulation of Ge TLP behavior for reduced junction depth of anode by lowering of the junction implant energy. This results in a smaller effective junction area and a higher sheet resistance R_s, see (2).

A less pronounced high current differential resistance lowering was observed for shallower junction implants. However I_{crit} is not changed. Lower I_{t2} for the shallower implant was observed. The shallower implant reduces the volume where the current flows. This increases intrinsic current density and leads to earlier failure.

Adding Germanide to the diode, while keeping the anode junction doping profile the same (comparing the two available Ge technologies), lowers the Ge diode contact resistance R_c. This process change lowers the low current resistance at 1mA/µm Figure 13 and V_{t2}.

Lower R_c, see (2), leads to higher voltage drop over the intrinsic diode junction at same current level for the germanided diode. This dissipates more power

into the intrinsic diode and leads to 2x lower J_{crit} and I_{t2} for the germanided device.

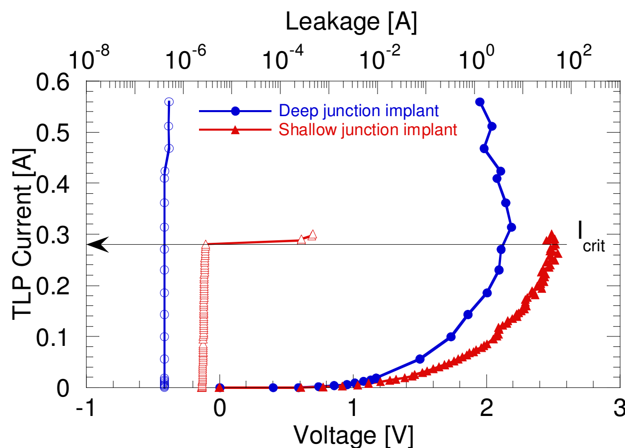

Figure 12 TLP (100 ns) measurements of Ge diode without NiGe with different junction implant conditions (W=50 µm, L=200 nm).

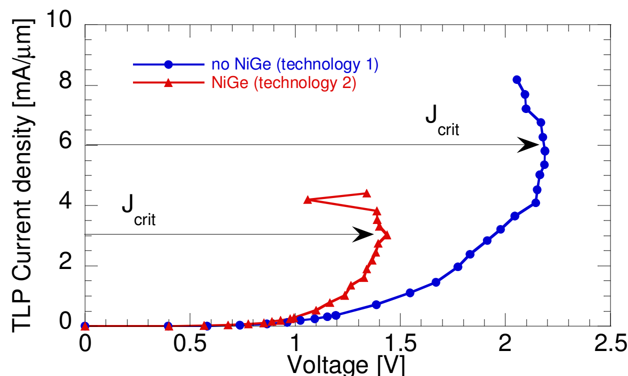

Figure 13 Normalized TLP (100 ns) measurement of Ge diodes w/ NiGe (*technology 2*) and w/o NiGe (*technology 1*) (L=200 nm), with comparable anode junction.

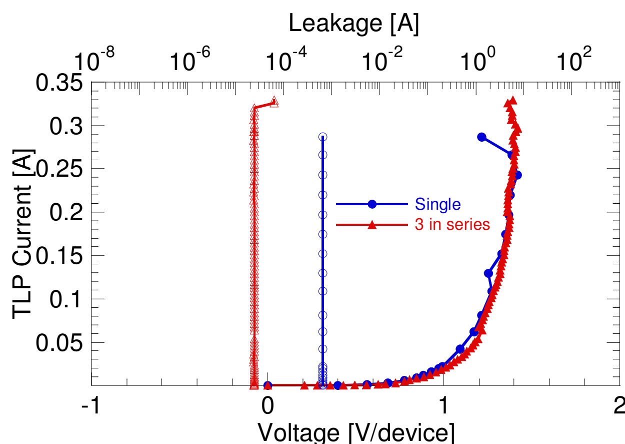

Figure 14 TLP (100 ns) measurement of Ge diodes with NiGe (W=80 µm, L=200 nm) in single and three in series configuration, Voltage is normalized per device.

The TLP IV curves of a single gated Ge diode and three Gated Ge diodes in series in *technology 2* are compared in Figure 14. The voltage is normalized per device. The IV curves matches. It shows that the differential resistance lowering attributed to Ge is present.

D Ge STI diodes in *technology 2* (*bulk*)

Technology 2 also provides STI diode structures with nwell and pwell regions. Schematics are shown in Figure 15. Besides a PN junction, these diodes also contain two material interfaces between Ge and Si (Bulk substrate). These interfaces contain crystalline defects caused by strain relaxation due to lattice mismatch between Si and Ge. This fact makes the diodes not suitable for ESD protection. The anode to cathode spacing (L) is defined by the STI dimension. Due to the longer current path and the material interface these diodes should have a higher series resistance compared to the Gated counterparts.

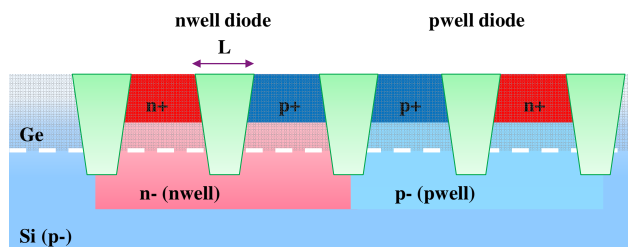

Figure 15 Schematic cross section of STI like diodes in *technology 2* (*bulk*), dashed line indicating Si to Ge interface with crystalline defects .

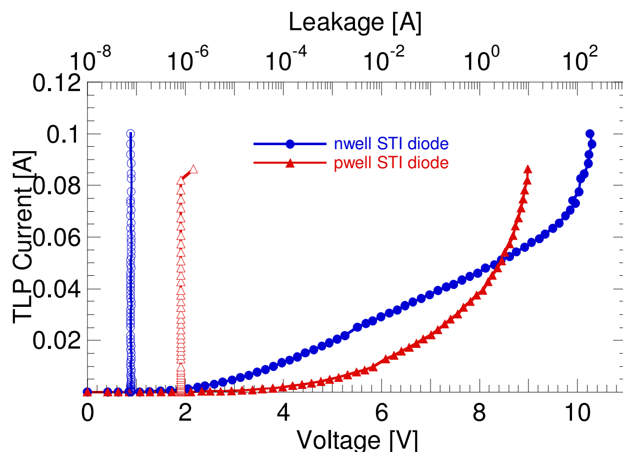

Figure 16 TLP (100 ns) measurement of nwell and pwell Ge STI diodes with NiGe (W=80 µm, L=320 nm).

The TLP IV curves of a nwell and a pwell STI diodes are overlaid in Figure 16. Both characteristics show high current differential resistance lowering as observed for gated diodes. This confirms that the behavior is Ge related. But the differential resistance

lowering starts at a higher voltage. This is due to the higher series resistance of nwell diode, because the pwell doping adds to the p- background substrate doping level while nwell counter dopes it. This is in conjunction with the previous findings that the differential resistance lowering can be modulated by the series resistance.

E Summary of TLP findings

All Ge structures show a significant differential resistance lowering at high current. At I_{crit} the differential resistance is zero. The differential resistance can get negative above I_{crit}, when the series resistance is small due to low R_c (NiGe) or short L (<500 nm). The fact that the behavior is independent of *SOI* doping type, confirms that the differential resistance lowering occurs only in the Ge layer. Change in series resistance modulates the differential resistance lowering. This was confirmed by changes in junction implant energy, by reduced contact resistance by adding NiGe, and by L and W variations. In addition, also a structural change going from Gated to STI diodes, confirms the existence of high current differential resistance lowering in the Ge layer.

IV. Discussion

While for Si, a clear signature of self-heating induced differential resistance increase in the 100 ns TLP with increasing L, shown in Figure 6, is observed, no similar trend is present in the Ge diodes, see Figure 7. To better understand this difference, 500 ns TLP characterization of Si and Ge diodes in *technology 1* has been done, see Figure 17 and Figure 18. In contrast to silicon technologies, longer pulses lead to a lower voltage across the Ge diode. This observation leads to the conclusion, that self-heating behavior of Ge diodes is different compared to Si diodes.

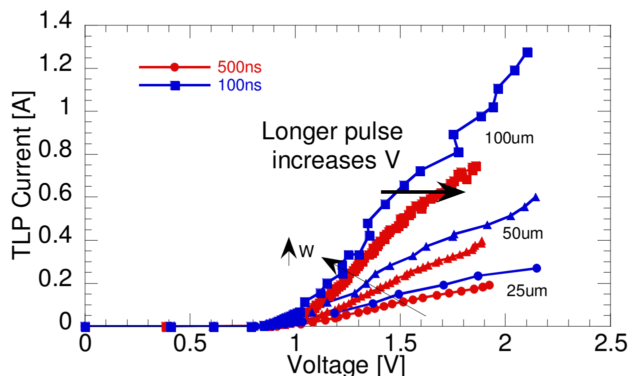

Figure 17 TLP measurement of W scaling of Si diodes with NiSi (L=200 nm) using 100 ns and. 500 ns TLP pulse length.

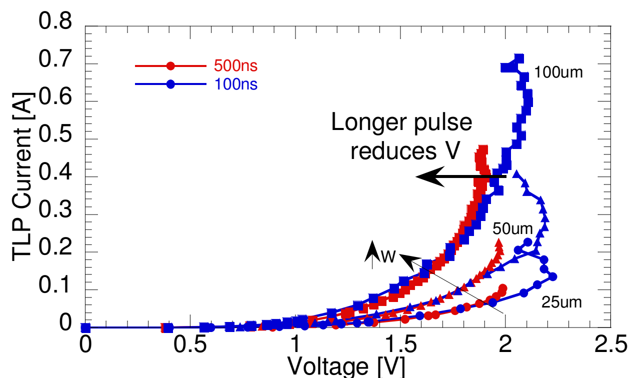

Figure 18 TLP measurement of W scaling of Ge diodes without NiGe (L=200 nm) using 100 ns and 500 ns TLP pulse length.

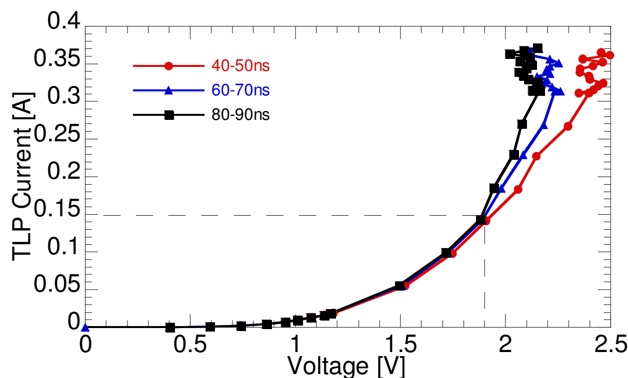

Figure 19 TLP (100 ns) measurement of Ge diodes without NiGe (W=50 µm, L=200 nm) with different averaging window.

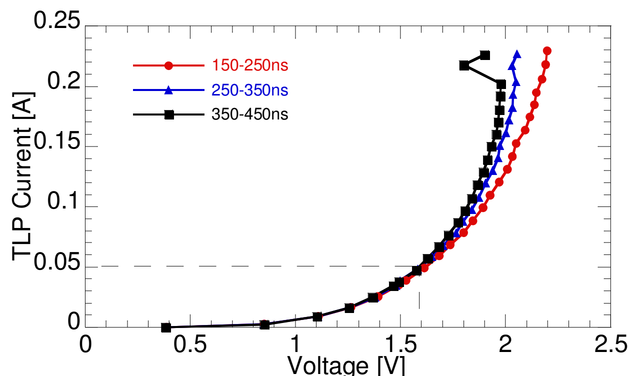

Figure 20 TLP (500 ns) measurement of Ge diodes without NiGe (W=50 µm, L=200 nm) with different averaging window.

Figure 19 and Figure 20 show TLP IV curves of 100 ns and 500 ns TLP pulse length, with different averaging windows for a Ge diode. There are three findings. First, the differential resistance lowering gets less pronounced with earlier averaging window Second, the voltage across the device is decreasing with averaging window moved to end of pulse. Third, differential resistance lowering occurs above a certain current level, when the curves split (above 0.15 A for 100 ns, Figure 19, and 0.05 A for 500 ns, Figure 20).

This means that the differential resistance reduction depends on the energy that is dissipated into the diodes.

To model the observed differential resistance lowering, we propose a temperature induced positive feedback mechanisms in strong forward ESD conduction for the Ge diode. When current increases, the internal temperature increases in the device due to Joule heating. The intrinsic carrier concentration n_i is a function of band gap E_g and temperature T *[9],*

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{2kT}\right), \qquad (3)$$

where N_C is effective density of states in the conduction band and N_V is effective density of states in the valence band. Already at 300 K, germanium has a 1000 x higher n_i than Si. E_g is a function of temperature, given by [10],

$$E_g(T) = E_g(0) - \frac{\alpha \cdot T^2}{T + \beta} \ . \qquad (4)$$

For Ge, E_g shows a stronger temperature dependence. As the band gap E_g of Ge is lower than for Si and the intrinsic temperature (temperature at which thermally generated carrier concentration approaches the majority carrier concentration) is also lower, more intrinsic carriers are thermally generated in Ge compared to Si. This self-heating induced carrier generation increases n and current, see (5). This leads to differential resistance lowering.

$$I \cong \mu \cdot n \cdot E \, , \qquad (5)$$

where μ is carrier mobility and n is carrier density. Above a critical current density J_{crit}, which corresponds to a critical temperature, the differential resistance drops to zero. As shown in the 100 ns vs. 500 ns TLP overlap data, Figure 18, this thermal process is relatively slow and hence the device can sustain relatively long time in this regime.

This model is confirmed by simple TCAD simulations of a Ge and Si diodes. Figure 21 shows the simulation of the voltage drop over a forward bias diode while varying the temperature, when stressed with a fixed current of 16mA/µm. Simulation shows that the voltage drop over a Germanium diode lowers with temperatures above 300 K until melting, illustrating the differential resistance lowering described above. For Si, voltage increases up to 700 K and drops at higher temperature.

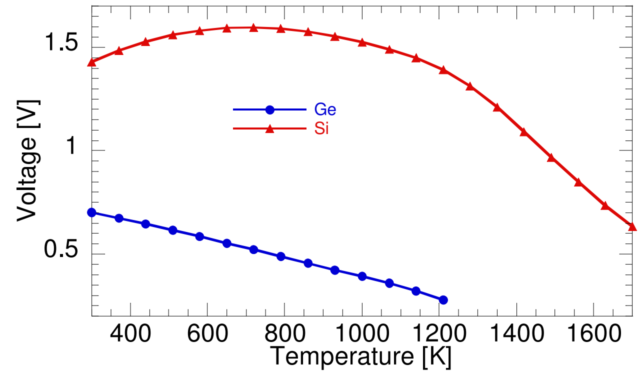

Figure 21 TCAD simulations of the voltage drop over a forward bias diode while varying the temperature, when stressed with a fixed current of 16 mA/µm.

Besides the high current differential resistance lowering observed in Ge, it was also observed that normalized I_{t2} is not independent of W for Ge. The I_{t2} normalized to W of Si and Ge diodes of *technology 1* are shown in Figure 22. The failure current density lowers with increasing width for Ge, while for Si it slightly increases. This indicates a non-uniform thermal failure mechanism in Ge, for example by filaments formed only at the boundary of the Ge diodes. However the exact fail mechanism and why Ge diodes can sustain zero differential resistance before failing was not identified and is subject of further research.

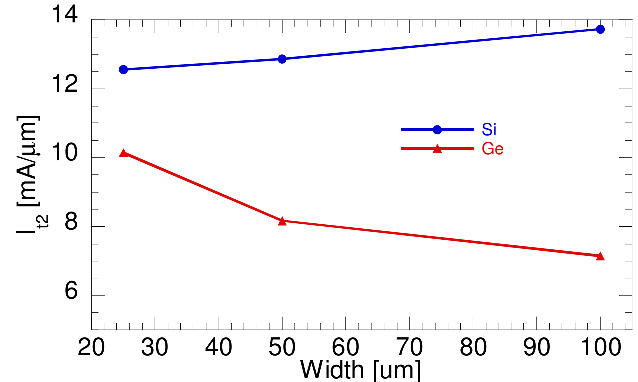

Figure 22 I_{t2} of TLP (100 ns) of Ge diodes without NiGe and Si with NiSi for different W (L=200 nm).

A Model validation by HBM IV

The proposed model links the differential resistance lowering observed in TLP characterizations of Ge diodes to thermally induced carrier generation. When the temperature exceeds the intrinsic temperature the thermally induced carrier generation starts and the differential resistance lowers. During a TLP pulse, temperature increases throughout the pulse. This was verified by a mixed mode simulation of a single in

TLP pulse on a Germanium-on-Insulator diode similar to *technology 1* (Figure 23) shown in Figure 24. Decimm simulator [12] was used.

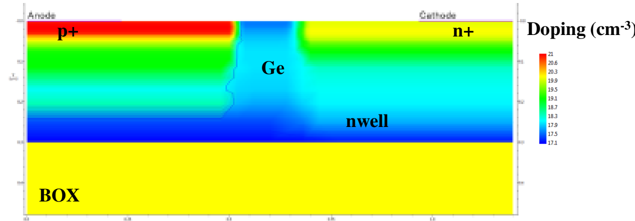

Figure 23 TCAD setup for Ge on Insulator diode (*technology 1*) with doping.

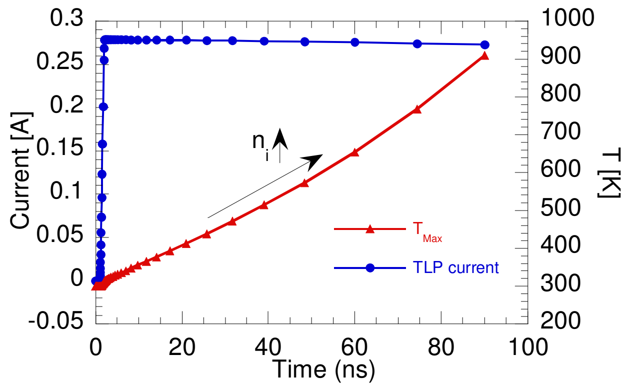

Figure 24 TCAD simulations of the T evolution during a single 300 mA TLP pulse (W=10 µm, L=200 nm).

By moving the averaging window towards the beginning of the pulse, less intrinsic carriers are generated and the differential resistance lowering is less pronounced. This is confirmed by Figure 19 and Figure 20 where the differential resistance lowering gets modulated by averaging window shift.

While a HBM pulse, the temperature increases until a peak temperature and declines after 200 ns. This temperature evolution was confirmed with Decimm [12], see Figure 25.

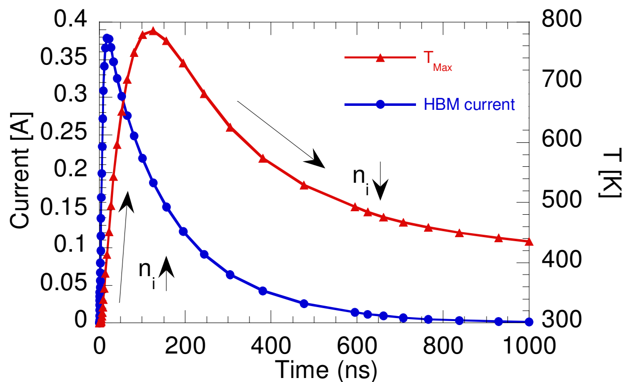

Figure 25 TCAD simulations of the T evolution for a 600 V precharge HBM pulse (W=10 µm, L=200 nm).

For HBM, thermally carrier generation starts when temperature (T) exceeds the intrinsic temperature and carriers continue to be generated until the temperature drops below the intrinsic temperature. The maximum temperature and the resulting maximum n_i correlates to the HBM peak current, which is linked to the precharge voltage. When intrinsic carrier generation occurs, the minimum differential resistance is a function of precharge voltage in the quasi static HBM IV. The minimum differential resistance lowers with increasing precharge voltage. Figure 26 and Figure 27 shows HBM IV curves [11] with different precharge voltages for a Ge and Si diode of *technology 1* (*SOI*).

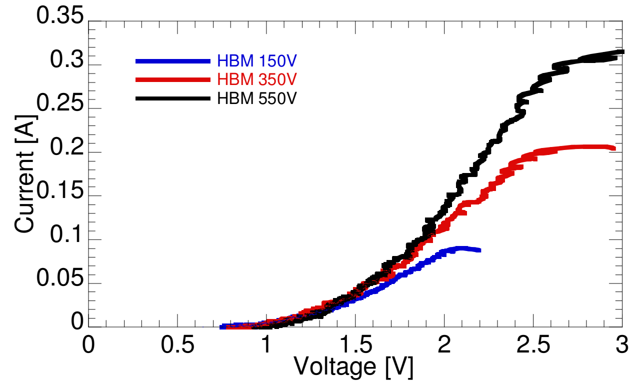

Figure 26 HBM measurements with different precharge voltages of Ge diodes without NiGe (W=50 µm, L=200 nm).

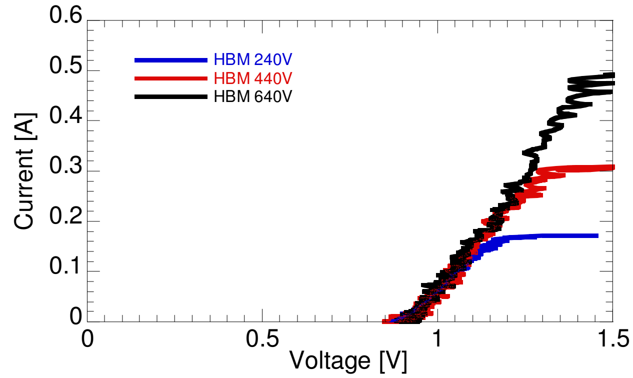

Figure 27 HBM measurements with different precharge voltages of Si diodes with NiSi (W=50 µm, L=200 nm).

For Ge diode, the maximum slope (minimum differential resistance) of the HBM IV curves increases with higher precharge voltage. For Si, the curves are on top of each other with no slope change. This confirms that only in Ge intrinsic carriers are generated and the proposed model is valid.

V. Conclusions

A thermally induced carrier generation that leads to zero-differential resistance at high TLP current is observed for Germanium diodes. This behavior is not known for Si diodes and enables superior clamping capability for Ge diodes.

All studied structures with a Ge layer show the high current differential resistance lowering. Above I_{crit} the differential resistance is zero.

It is possible to achieve negative differential resistance when the series resistance is low enough. This behavior was observed for devices with short L or NiGe. The onset of the differential resistance lowering can be suppressed by increasing the series resistance. This finding was confirmed with junction implant energy reduction or increase of L. In addition also a structural change going from Gated to STI diodes confirms the existence of high current differential resistance lowering is related to Ge.

A model to explain the differential resistance lowering in Ge by a temperature induced positive feedback mechanisms is proposed. This model is validated by HBM IV measurements.

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