# Design and Experimental Verification of a Third Harmonic Injection Rectifier Circuit Using a Flying Converter Cell 

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#### Abstract

The proposed active three-phase rectifier circuit utilizing a Flying Converter Cell (FCC) based on the concept of third harmonic injection allows the extension of a passive three-phase diode bridge rectifier to a low-harmonic input stage ( $\mathbf{T H D}_{\mathbf{i}}<5 \%$ ) for applications where dc-link voltage control is not required. In this work the design and experimental verification of a 10 kW laboratory prototype using the proposed concept is addressed. Based on the analysis of the rectifier system a control concept is developed which is implemented in a digital signal processor. It is shown that the proposed rectifier system shows several degrees of freedom which can be used for system optimization. Several implementation details are discussed and experimental results taken from the constructed 10 kW laboratory prototype demonstrate the good performance of the proposed rectifier system and verify the proper operation of the developed control concepts.


## I. Introduction

In recent years power quality and low harmonic distortion of the power supply grid are getting more and more important. Especially due to the smart grid vision, where many small power loads and generators are planned to be operating on the mains, power converter systems connected to the mains are facing advanced requirements in order not to distort the grid. Passive three-phase rectifier circuits, such as the standard B6 diode bridge with dc-side located smoothing inductor, are very robust, highly efficient and have therefore been widely used in industry. They can, however, not fulfill the more stringent requirements on input current quality ( $\mathrm{THD}_{\mathrm{i}}<5 \%$ ) anymore. Active rectifier systems such as the bidirectional six-switch rectifier circuit [1] are commonly used to improve the input current quality. An overview of active three-phase rectifier systems can be found in [2], [3]. The active current shaping of these topologies, however, results in a reduced efficiency compared to the B6 diode bridge rectifier. Existing passive diode rectifier systems can furthermore not be extended to these active rectifier circuits.
The idea of third harmonic injection improves the input current quality by injecting a current either into all three phases [4], [5] or into a single phase [6] of the diode bridge. It was first applied by the Minnesota Rectifier [4] which uses boost stages at the output of the diode bridge for current shaping and recently the Swiss rectifier [5] has been developed which uses buck stages for current shaping. The topologies show a $\mathrm{THD}_{\mathrm{i}}<5 \%$ and
offer a controlled dc-link voltage. A comprehensive overview on such three-phase rectifier topologies using the concept of third harmonic injection can be found in [7]. These topologies, however, also suffer from a reduced efficiency as the full power still has to be processed by the semiconductors used for current shaping and dc-link voltage control.
In many applications, e.g. ac drives, etc., a controlled dc-link voltage is not required and topologies based on the concept of third harmonic injection using either passive [8], [9] or active [10], [11] current shaping networks have been developed which do not offer a controlled dc-link voltage. These topologies typically require a constant power load at the output of the rectifier and cannot be used with a considerably large dc-link capacitors as often required in industrial applications.

In this work the design, implementation and control of a three-phase third harmonic injection rectifier circuit using a "Flying" converter cell (FCC) as proposed in [12] is discussed in detail (cf., Fig. 1). The FCC topology allows the extension of an existing passive B6 diode bridge rectifier with smoothing inductor and large dc-link capacitor to a low-harmonic rectifier system by application of an additional power electronic circuit called "Flying" converter cell.

## II. Flying Converter Cell

The basic structure of the three-phase rectifier circuit using an FCC is shown in Fig. 1. The passive B6 diode bridge rectifier circuit with dc-side located smoothing inductor $L_{\mathrm{DC}}$ and considerably large output capacitor $C_{\mathrm{o}}$ is extended by the FCC and three bidirectional switches for current injection of the third harmonic current $i_{\mathrm{h} 3}$ into a single phase. The basic idea is to inject current into the phase which would not conduct current in passive diode mode. In addition, currents $i_{\text {cp }}$ and $i_{\mathrm{cn}}$ are injected into the positive and negative output of the diode bridge in order to achieve sinusoidal mains currents. The FCC basically consists of three converter stages: two halfbridges ( $S_{\mathrm{cp} \pm}, S_{\mathrm{cn} \pm}$ ) and a three-level bridge leg ( $D_{\mathrm{h} 3 \pm}, S_{\mathrm{h} 3}$ ). A unidirectional implementation of the three-level bridge-leg is used in this work, however, as discussed in [12] dependent on the operating mode of the FCC a bidirectional implementation of the three-level bridge leg may be required. As shown in


Fig. 1: Basic schematic of the proposed rectifier system employing a Flying Converter Cell.

Fig. 1 three inductors, $L_{\mathrm{cp}}, L_{\mathrm{cn}}$ and $L_{\mathrm{h} 3}$, are required for proper operation of the FCC. According to Kirchhoff's law the three currents have to fulfill

$$
\begin{equation*}
i_{\mathrm{cp}}=i_{\mathrm{cn}}+i_{\mathrm{h} 3} \tag{1}
\end{equation*}
$$

and therefore a coupled three-phase arrangement can be used advantageously for implementation of the chokes.

As discussed in [12] several operating modes of the FCC exist. The three converter systems are equal regarding control of the three currents and in this work the operating mode II, the two half-bridges are used to control the injected currents and the three-level bridge leg is used to control the average value (averaged over the switching frequency) of the midpoint voltage $v_{\mathrm{MN}, \mathrm{avg}}$, is used. The required FCC dc-link voltages $V_{\mathrm{cp}}$ and $V_{\mathrm{cn}}$ are related to the mains voltage and a modulation index

$$
\begin{equation*}
M=\frac{\hat{V}_{\mathrm{N}}}{V_{\mathrm{c}}} \tag{2}
\end{equation*}
$$

is defined. The FCC dc-link voltage results in $V_{\mathrm{c}}=400 \mathrm{~V}$ for a mains voltage of $V_{\mathrm{LL}}=400 \mathrm{~V}$ and a modulation index of $M=0.813$ and therefore semiconductors with a blocking voltage capability of 600 V can advantageously be applied for the half-bridges ( $S_{\mathrm{cp} \pm}, S_{\mathrm{cn} \pm}$ ) and the switches of the three-level bridge-leg $S_{\mathrm{h} 3}$.

One remarkable advantage of the proposed topology is that the FCC only has to process a small amount of output power

$$
\begin{equation*}
P_{\mathrm{h} 3}=P_{\mathrm{cp}}+P_{\mathrm{cn}}=5.8 \% P_{\mathrm{o}} \tag{3}
\end{equation*}
$$

Whereas the three-level bridge-leg processes only active power the two half-bridges used for injection of the currents $i_{\mathrm{cp}}$ and $i_{\text {cn }}$ have to deal with reactive power of $Q_{\mathrm{c}}=16.7 \% P_{\mathrm{o}}$. As will be further discussed in section IV the total losses of the FCC are quite small which results in an excellent efficiency. The proposed rectifier also shows no high-frequency CM voltage at the rectifier output $V_{\mathrm{o}}$, only the FCC shows a midpoint-voltage $v_{\text {MN }}$ which is only present inside of the FCC.

In Fig. 2 simulated current and voltage waveforms of the topology are shown for the parameters $P_{\mathrm{o}}=10 \mathrm{~kW}, V_{\mathrm{LL}}=$


Fig. 2: Simulated current and voltage shapes of the proposed rectifier system for an output power of $P_{\mathrm{o}}=10 \mathrm{~kW}$ and $V_{\mathrm{LL}}=400 \mathrm{~V}, f_{\mathrm{N}}=50 \mathrm{~Hz}$.

400 V and $f_{\mathrm{N}}=50 \mathrm{~Hz}$. The mains currents are in phase with the mains voltages and show sinusoidal shape with a $\mathrm{THD}_{\mathrm{i}}$ of $2.7 \%$. The currents $i_{\mathrm{cp}}$ and $i_{\mathrm{cn}}$ injected into the positive/negative bus bar show $3^{r d}$ and $6^{\text {th }}$ harmonic components of the fundamental frequency. The current $i_{\mathrm{h} 3}$ is composed of sections of the three mains currents and shows approximately triangular shape. In addition the high-frequency component of the midpoint voltage $v_{\mathrm{MN}^{\prime}}$ is shown in Fig. 2 together with its averaged value $v_{\mathrm{MN}^{\prime} \text {,avg }}$. More detailed information on the basic operation principle can be found in [12].


Fig. 3: Measured signals used for the digital control of the rectifier circuit.

## III. Control

Several controllers are required for proper operation of the new rectifier circuit. It is obvious that fast-acting current controllers are required to shape the mains currents, however, it is not clear in which way the reference currents must be generated. The reference current generation of topologies using the concept of third harmonic injection without output voltage control has insufficiently been discussed in literature up to now and a promising method is given below. Next to the current controller also controllers for the FCC dc-link voltages are required. In Fig. 3 the measurement signals used for the digital control of the rectifier circuit are shown. Next to the mains voltages $v_{\mathrm{N} i}$ also the currents $i_{\text {pos }}, i_{\text {neg }}$ and $i_{\mathrm{L}}$ are measured as well as the rectifier output voltage $v_{\text {rec }}$ and midpoint voltage $v_{\mathrm{MN}^{\prime}}$.

## A. Current Control

The basic structure of the proposed current controller is shown in Fig. 4. In the following the concept of average mode current control is used. The basic idea is to control the output currents $i_{\text {pos }}$ and $i_{\text {neg }}$ of the diode bridge by injecting adequate currents $i_{\mathrm{cp}}$ and $i_{\text {cn }}$ into the busbars as

$$
\begin{equation*}
i_{\text {pos }}=i_{\mathrm{L}}-i_{\mathrm{cp}} \quad i_{\mathrm{neg}}=i_{\mathrm{cn}}-i_{\mathrm{L}} \tag{4}
\end{equation*}
$$

applies. The two half bridges are therefore used for current control whereat the three-level bridge-leg is used for balancing of the FCC dc-link voltages and to control the average value of the midpoint voltage $v_{\mathrm{MN}, \text { avg }}$ to zero. Two independent current controllers are used for $i_{\text {pos }}$ and $i_{\text {neg }}$ and the current $i_{\mathrm{h} 3}$ results due to (1).

In Fig. 5 the simplified model of the FCC is shown. For $\varphi_{N} \in\left[0 \ldots \frac{\pi}{6}\right]\left(i_{\mathrm{N} 1}\left(\varphi_{\mathrm{N}}\right)>0 ; i_{\mathrm{N} 2}\left(\varphi_{\mathrm{N}}\right), i_{\mathrm{N} 3}\left(\varphi_{\mathrm{N}}\right)<0\right)$

$$
\begin{array}{r}
\delta_{\mathrm{cp}} v_{\mathrm{cp}}+v_{\mathrm{MN}, \mathrm{avg}}-v_{\mathrm{pos}}=L \frac{d i_{\mathrm{cp}}}{d t} \\
\left(1-\delta_{\mathrm{h} 3}\right)\left(-v_{\mathrm{cn}}\right)+v_{\mathrm{MN}, \mathrm{avg}}-v_{\mathrm{mid}}=-L \frac{d i_{\mathrm{h} 3}}{d t}  \tag{5}\\
\left(1-\delta_{\mathrm{cn}}\right)\left(-v_{\mathrm{cn}}\right)+v_{\mathrm{MN}, \mathrm{avg}}-v_{\mathrm{neg}}=-L \frac{d i_{\mathrm{cn}}}{d t}
\end{array}
$$

can be calculated where equal inductors $\left(L=L_{\mathrm{cp}}=L_{\mathrm{cn}}=\right.$ $L_{\mathrm{h} 3}$ ) for the three converter stages are assumed. In the sector $\varphi_{N} \in\left[0 \ldots \frac{\pi}{6}\right] v_{\mathrm{pos}}=v_{\mathrm{N} 1}, v_{\mathrm{mid}}=v_{\mathrm{N} 2}$ and $v_{\mathrm{neg}}=v_{\mathrm{N} 3}$


Fig. 4: Basic structure of the proposed current controller including pulse-width modulation.


Fig. 5: Simplified circuit of the FCC used to derive the converter model for current control.
applies. The two dc-link voltages are controlled by the FCC dc-link voltage controller with reduced dynamic and equal (constant) voltages $V_{\mathrm{cp}}=V_{\mathrm{cn}}=V_{\mathrm{c}}$ are assumed for the current controller. Also the average value of the midpoint voltage $v_{\mathrm{MN}, \text { avg }}$ can be treated as constant as it shows much smaller dynamic. Based on this simplification Laplace Transformation can be applied which results in

$$
\begin{align*}
\delta_{\mathrm{cp}} V_{\mathrm{c}}+V_{\mathrm{MN}, \mathrm{avg}}-v_{\mathrm{pos}} & =s L i_{\mathrm{cp}} \\
\left(1-\delta_{\mathrm{h} 3}\right)\left(-V_{\mathrm{c}}\right)+V_{\mathrm{MN}, \mathrm{avg}}-v_{\mathrm{mid}} & =-s L i_{\mathrm{h} 3}  \tag{6}\\
\left(1-\delta_{\mathrm{cn}}\right)\left(-V_{\mathrm{c}}\right)+V_{\mathrm{MN}, \mathrm{avg}}-v_{\mathrm{neg}} & =-s L i_{\mathrm{cn}}
\end{align*}
$$

In the following only the equation for current $i_{\text {cp }}$ is exemplary analyzed, similar considerations can, however, be done for the other currents. Using (4) for $i_{\mathrm{cp}}$ results in

$$
\begin{equation*}
s L i_{\mathrm{pos}}=s L i_{\mathrm{L}}-\delta_{\mathrm{cp}} V_{\mathrm{c}}-V_{\mathrm{MN}, \mathrm{avg}}+v_{\mathrm{pos}} \tag{7}
\end{equation*}
$$

By inspecting (6) and Fig. 5 it is obvious that the upper half bridge of the FCC must generate an average voltage which is equal to the voltage difference $v_{\text {pos }}-V_{\mathrm{MN}, \text { avg }}$ which means that this voltage difference can advantageously be used as feedforward signal. According to (4) the current $i_{\mathrm{L}}$ is a disturbance input of the current control loop and disturbance rejection can be applied using the measured current value $i_{\mathrm{L}}$. Using the resulting feed-forward signal

$$
\begin{equation*}
\delta_{\mathrm{cp}}=\tilde{\delta}_{\mathrm{cp}}+\frac{v_{\mathrm{pos}}-V_{\mathrm{MN}, \mathrm{avg}}}{V_{\mathrm{c}}}+s \frac{L i_{\mathrm{L}}}{V_{\mathrm{c}}} \tag{8}
\end{equation*}
$$

together with (7) results in the very simple model

$$
\begin{equation*}
G_{\mathrm{I}}(s)=\frac{i_{\mathrm{pos}}(s)}{\tilde{\delta}_{\mathrm{cp}}(s)}=-\frac{V_{\mathrm{c}}}{s L} . \tag{9}
\end{equation*}
$$

The corresponding feed-forward terms are shown in Fig. 4 where the required differentiator block for $i_{\mathrm{L}}$ is extended by a low-pass filter with higher cut-off frequency for noise suppression. The current controller $K_{\mathrm{I}}(s)$ can be a P-type or a PI-type controller.

## B. Midpoint Voltage

According to Fig. 1 the FCC is connected to the passive diode bridge using either three individual inductors or a coupled three-phase choke. Due to the switching actions of the FCC the midpoint voltage shows high-frequency voltage fluctuations (cf., Fig. 2) and its average value is only defined by the precontrol signals. An additional controller must be implemented to control the average value of the midpoint voltage to a dedicated value. The midpoint voltage $v_{\mathrm{MN}}{ }^{\prime}$ can be measured between the midpoint $M$ of the FCC and the artificial star point $N^{\prime}$ built by the ac-side connected filter capacitors (see also Fig. 1 and Fig. 3). The average value is determined by simply filtering the measured midpoint voltage which is not a challenge as the high-frequency components are at the switching frequency and harmonics of the switching frequency.

As the two half-bridges already shape the FCC currents the three-level bridge-leg can be used for control of the midpoint voltage (and for balancing of the FCC dc-link voltages). The reference value $v_{\mathrm{MN}}^{*}$ is thereto compared to the filtered voltage $v_{\mathrm{MN}^{\prime}, \text { avg }}$ and the deviation is the input of the midpoint voltage controller showing small dynamic. Similar to the current controller also here the voltage $v_{\mathrm{h} 3}$ can be used as feed-forward term. The resulting controller is shown in Fig. 7(b).

## C. Generation of Reference Currents

In conventional active rectifier circuits [3], the reference currents are often generated by a superimposed voltage controller which indirectly determines the power demand by measuring the voltage of the dc-link capacitor. The output voltage of the proposed rectifier system is, however, not controlled, but is dependent on the mains and load situation and is even not measured. The power transferred from the mains to the output of the rectifier is not dependent on the current shape and can therefore be determined by measurement in both operating modes, operating in diode mode as well as for active current shaping using the FCC. The power demand can be determined using the mains voltages/currents

$$
\begin{equation*}
p(t)=v_{\mathrm{N} 1}(t) i_{\mathrm{N} 1}(t)+v_{\mathrm{N} 2}(t) i_{\mathrm{N} 2}(t)+v_{\mathrm{N} 3}(t) i_{\mathrm{N} 3}(t) \tag{10}
\end{equation*}
$$

with subsequent low-pass filtering of the actual active power. This would, however, require three additional current sensors for mains current measurement. A more convenient way is to use $v_{\text {rec }}$ and $i_{\mathrm{L}}$

$$
\begin{equation*}
p(t)=v_{\mathrm{rec}}(t) i_{\mathrm{L}}(t) \tag{11}
\end{equation*}
$$

The voltage $v_{\text {rec }}$ can either be calculated using the mains voltage measurement or measured using a dedicated voltage
measurement circuit. Considering also the case where all diodes are in blocking mode measuring of the voltage $v_{\text {rec }}$ is preferred. The equivalent conductance $g_{\mathrm{e}}^{*}$ can now be calculated by

$$
\begin{equation*}
g_{\mathrm{e}}^{*}=\frac{P_{\mathrm{in}}}{V_{\mathrm{N} 1, \mathrm{rms}}^{2}+V_{\mathrm{N} 2, \mathrm{rms}}^{2}+V_{\mathrm{N} 3, \mathrm{rms}}^{2}} \tag{12}
\end{equation*}
$$

and finally multiplied with the (calculated) voltages $u_{\text {pos }}$ and $u_{\text {neg }}$ to derive the reference currents $i_{\text {pos }}^{*}$ and $i_{\text {neg }}^{*}$.

## D. Modulation

In this work pulse width modulation is used to generate the gate signals of the semiconductors. The triangular shaped carrier signals of the FCC's three converter stages can advantageously be synchronized and a possibility to optimize system behavior with respect to current ripple and midpoint voltage $v_{\text {MN }}$ exists. Fig. 6(a) shows the PWM, the switching sequence and the resulting midpoint voltage $v_{\mathrm{MN}}$ at $\varphi_{\mathrm{N}}=15^{\circ}$ if all three triangular shaped carrier signals are in phase and Fig. 6(b) depicts the situation where the carrier signal of $S_{\mathrm{h} 3}$ is phase shifted by $180^{\circ}$. In order to analyze the behavior similar to [12] a switching state $\left(s_{\mathrm{cp}}, s_{\mathrm{h} 3}, s_{\mathrm{cn}}\right)$ can be defined where e.g. $s_{\mathrm{cp}}=1$ denotes the turn-on state of the switch $S_{\mathrm{cp}+}$ (switch $S_{\mathrm{cp}-}$ is turned off) and $s_{\mathrm{cp}}=0$ denotes the turn-on state of the switch $S_{\mathrm{cp}-}$ (switch $S_{\mathrm{cp}+}$ is turned off).
As shown in Fig. 6(a) for $\varphi_{\mathrm{N}}=15^{\circ}$ the midpoint voltage shows voltage levels of $\pm V_{\mathrm{C}} / 3,0$ and $\pm 2 V_{\mathrm{C}} / 3$ if symmetrical FCC dc-link voltages are assumed. As can be observed in Fig. 6(b) the midpoint voltage shows only voltage levels of $\pm V_{\mathrm{C}} / 3$ and 0 if the carrier signal for the three-level bridge-leg is shifted by $180^{\circ}$. This allows to optimize the high-frequency midpoint voltage $v_{\mathrm{MN}}$. On the other hand the current ripple of the injected currents increases considerably if the carrier signals are phase shifted by $180^{\circ}$ (not shown in Fig. 6). The maximum current ripples derived in [12] are only valid for carrier signals showing a phase shift of $180^{\circ}$ (cf., Fig. 6(b)). If synchronized carrier signals without phase shift shall be used the maximum current ripple calculates to

$$
\begin{align*}
\Delta i_{\mathrm{c} \frac{\mathrm{p}}{\mathrm{n}}, \mathrm{pkpk}} & =\frac{V_{\mathrm{c}} M^{2}}{4 f_{\mathrm{s}} L} \\
\Delta i_{\mathrm{h} 3, \mathrm{pkpk}} & =\frac{V_{\mathrm{c}} \frac{M}{2}\left(1-\frac{M}{2}\right)}{f_{\mathrm{s}} L} \tag{13}
\end{align*}
$$

which are quite smaller than the current ripples given in [12]. The choice of phase shift between the carrier signals therefore allows to optimize the system behavior for minimal current ripple or for minimal midpoint voltage $v_{\mathrm{MN}}$. As the current ripple is directly related to losses the operating mode with synchronized carrier signals in phase is used in this work.

## E. FCC DC-Link Voltages

As already noted, the voltages of the FCC dc-link must be controlled. The total voltage is handled by a voltage controller and balancing of the two dc-link capacitors requires a dedicated controller. Control of the dc-link voltages must be done without disturbing the input currents. The structure of the voltage


Fig. 6: Modulation of the three converter stages of the FCC using synchronized triangular shaped carrier signals at $\varphi_{\mathrm{N}}=15^{\circ}$. (a) All three converter stages use carrier signals in phase and (b) the three-level bridge-leg uses a carrier signal with a phase shift of 180 deg .
controller is shown in Fig. 7(a). The output of the FCC dclink voltage controller $\Delta p$ is added to the measured power $P_{\text {meas }}$ which yields the requested power $P^{*}$. The equivalent conductance $g_{\mathrm{e}}^{*}$ is finally calculated according to (12). Please note that the FCC dc-link voltage controller may include some nonlinear control behavior and that the power demand $\Delta p$ required for control is typically only a small fraction of $P^{*}$.

A detailed analysis of the FCC showed that different midpoint voltages $v_{\mathrm{MN}}$ result in different currents in the two dc-link capacitors. This effect can be used for balancing of the FCC dclink capacitor. The average value of the midpoint voltage must thereto be shaped as shown in Fig. 8. Dependent on the offset $v_{\text {off }}$ of the rectangular waveform $v_{\text {rect }}$ the capacitors are charged or discharged. The amplitude of the rectangular waveform is fixed to a small amount of $V_{c}$ and the balancing controller only alters the offset. These details are not shown in Fig. 7(b) and the whole controller is simply represented by $K_{\mathrm{B}}(s)$. The output of the balancing controller $v_{\mathrm{MN}}^{*}$ is the reference value for the


Fig. 7: (a) Structure of FCC dc-link voltage controller and reference current generation and (b) balancing of FCC dc-link voltages and control of average value of midpoint voltage $v_{\mathrm{MN}^{\prime}}$.


Fig. 8: Proposed midpoint voltage variations used for balancing of the two FCC dc-link voltages.
midpoint controller.

## IV. System Design

A 10 kW laboratory prototype according to the specifications given in TABLE I has been constructed. The built prototype is used to verify the basic operating principle of the FCC and is neither optimized for size nor for efficiency. It should furthermore act as a scaled demonstrator for higher power ratings (e.g. 200 kW ) and therefore a rather small switching frequency of $f_{\mathrm{s}}=10 \mathrm{kHz}$ is chosen intentionally. Please note that MOSFETs could be applied advantageously due to the small voltage rating of the FCC switches which would allow to increase the switching frequency considerably and which would result in a considerably higher power density. In addition the switching frequency of 10 kHz is a challenge for control as the currents $i_{\mathrm{cp}}$ and $i_{\mathrm{cn}}$ show high harmonics ( $3^{\text {rd }}$ and $6^{\text {th }}$ harmonic) and the head room to the switching frequency is rather small. As shown below the constructed hardware demonstrates that a high current quality can be achieved using

TABLE I: Design Specifications of the Built Three-Phase Rectifier using a FCC.

| Mains voltage: | $V_{\mathrm{LL}}=400 \mathrm{~V} \mathrm{rms}$ |
| :--- | :--- |
| Mains frequency: | $f_{\mathrm{N}}=50 \mathrm{~Hz}$ |
| Switching frequency: | $f_{\mathrm{s}}=10 \mathrm{kHz}$. |
| FCC dc-link voltage: | $V_{\mathrm{cp}}=V_{\mathrm{cn}}=400 \mathrm{~V}$ |
| Output power: | $P_{\mathrm{o}}=10 \mathrm{~kW}$ |



Fig. 9: Constructed 10 kW laboratory prototype of the FCC and used threephase choke. Dimensions FCC: $300 \mathrm{~mm} \times 200 \mathrm{~mm} \times 97 \mathrm{~mm}$ and three-phase choke $120 \mathrm{~mm} \times 50 \mathrm{~mm} \times 100 \mathrm{~mm}$.
the proposed topology even with the small switching frequency.
The constructed prototype is shown in Fig. 9 together with the applied three-phase choke (the passive diode rectifier with dc-side located smoothing inductor is not shown in Fig. 9). The FCC consists of two boards, the power board containing all main power components such as semiconductors, FCC dclink capacitors, input filter, etc., and the control board which basically includes the digital controller and analog measurement circuitry. The proposed control algorithm is implemented in a fixed point DSP (TI 320F2808) and a Lattice CPLD (Mach XO 2280) is used to implement the four step commutation sequence for the bidirectional switches.

The current stress formulas for semiconductors and passive components derived in [12] have been used to design the FCC and system losses are calculated. The applied components of the FCC are listed in TABLE II and the results of the loss calculation for an output power of $P_{\mathrm{o}}=10 \mathrm{~kW}$ are given in Fig. 10 where a calculated efficiency of $98.0 \%$ is stated. The system elements with highest losses are, as expected, the diode bridge and the dc-side connected smoothing inductor of the passive rectifier circuit as $95 \%$ of the output power is delivered by the diode bridge. The biggest loss part of the FCC is the coupled three-phase choke. The semiconductor losses of the FCC on the other hand are quite small and the losses of the three-level bridge leg are mainly caused by switching losses which could be reduced by application of SiC diodes. As discussed earlier also the losses of the bidirectional switches can be reduced by application of RB-IGBTs.

TABLE II: Power Devices Selected for Implementation of the FCC Prototype.

| $S_{\mathrm{ia}, \mathrm{b}}$ | $1200 \mathrm{~V} / 40 \mathrm{~A} \mathrm{IGBT}$, IKW40T120, Infineon |
| :--- | :--- |
| $S_{\mathrm{c} \mathrm{p}} \pm$ | $600 \mathrm{~V} / 20 \mathrm{~A}$ IGBT, IKW20N60H3, Infineon |
| $D_{\mathrm{h} 3 \pm}$ | $1200 \mathrm{~V} / 15 \mathrm{~A}$, STTH1512W, ST-Microelectronics |
| $C_{\mathrm{c}}^{\mathrm{p}}$ | $470 \mu \mathrm{~F} / 400 \mathrm{~V}$, EPCOS B43501-type |
| $L_{\mathrm{p}}=L_{\mathrm{cn}}=L_{\mathrm{h} 3}$ | 3.2 mH, Iron core 3UI60a, N = 123 turns |
| $C_{\mathrm{F}}, C_{\mathrm{S}}$ | $6.8 \mu \mathrm{~F} / 275 \mathrm{~V}$ AC, MKP X2, Arcotronics |
| $C_{\mathrm{o}}$ | $2.2 \mathrm{mF} / 400 \mathrm{~V}$, Felsic CO 39 A728848 |
| $L_{\mathrm{DC}}$ | 2.25 mH, Iron core $2 \times$ xI60a |
| $D_{1}-D_{6}$ | $35 \mathrm{~A} / 1600 \mathrm{~V}, 36 \mathrm{MT} 160$, Vishay |



Fig. 10: Calculated power loss breakdown of the proposed rectifier system for an output power of 10 kW .

## A. Bidirectional switches $S_{1 \mathrm{a}} \ldots S_{3 \mathrm{~b}}$

The bidirectional switches ( $S_{1 \mathrm{a}} \ldots S_{3 \mathrm{~b}}$ ) used for current injection of the current $i_{\mathrm{h} 3}$ into the mains are implemented using back-to-back connected 1200 V rated IGBTs (cf., Fig. 1). Alternatively to the two back-to-back connected IGBTs also parallel arranged Reverse Blocking IGBTs (RB-IGBTs) could be used which would allow a reduction of losses. In Fig. 11 the required switching scheme of the switches $S_{1 \mathrm{a}} \ldots S_{3 \mathrm{~b}}$ is shown. According to Fig. 11 each IGBT is switched only twice a period and semiconductors with a large chip area and therefore small conduction losses can be applied as switching losses can be neglected due to the very few switching actions. A four step commutation sequence as known from Matrix converters [13] can be implemented advantageously to commutate the current $i_{\mathrm{h} 3}$ from one phase to another phase. As can be seen in Fig. 11 the commutation has to be done when the amplitude of $i_{\mathrm{h} 3}$ reaches its maximum/minimum and the current direction in these points is clearly defined. The current dependent four step commutation sequence is therefore applied. In case of no-load or light-load situation the detection of the actual current direction might be incorrect and two additional diodes ( $D_{\mathrm{P}+}$ and $D_{\mathrm{P}_{-}}$) to the positive/negative output of the diode bridge as indicated in Fig. 1 are proposed to prevent the bidirectional switches from damage.

A sector detection must be implemented to initiate the four step commutation sequence. The correct detection of the sectors is very important as slight deviations result in considerably large current distortions. Sector detection could be done by application of a PLL in the digital controller, however, the


Fig. 11: Switching scheme of bidirectional switches $S_{1 \mathrm{a}} \ldots S_{3 \mathrm{~b}}$ used for current injection of $i_{\mathrm{h} 3}$ into a single phase.
limited switching frequency of 10 kHz results in an update of every $50 \mu$ s if double edge sampling is used for PWM which would lead too large current distortions. Analogue comparators in combination with bandpass filters are hence used for sector detection and the commutation sequence is implemented using a Lattice CPLD (Mach XO 2280).

## B. Input Filter

Filter capacitors at the ac-side of the rectifier are required due to the current ripple of the injected currents. These filter capacitors build an LC-tank together with the mains impedance which is excited at the end of every multi-device commutation process of rectifier diodes and bidirectional switches and must be damped. An RC snubber circuit ( $R_{\mathrm{S}}, C_{\mathrm{S}}$ ) as shown in Fig. 1 is used to damp this oscillation. The FCC may optionally be used to implement active damping of the input filter but this is subject of further research.

## V. Experimental Results

Measurement results of the constructed 10 kW laboratory prototype are given in Fig. 12 and Fig. 13. Fig. 12(a) shows the transition from passive diode mode operation with poor input current quality $\left(\mathrm{THD}_{\mathrm{I}}=46.4 \%\right)$ to active current shaping using the proposed FCC for $P_{\mathrm{o}}=10 \mathrm{~kW}$. A smooth transition can be observed and the active current shaping results in sinusoidal mains currents with good input current quality.

The three mains currents $i_{\mathrm{N} i}$ and phase voltage $v_{\mathrm{N} 1}$ are shown in Fig. 12(b) for $P_{\mathrm{o}}=10 \mathrm{~kW}$. The currents show a THD $\mathrm{I}_{\mathrm{I}}$ of $2.3 \%$ and a power factor of $\lambda=0.99$ can be read. Please note that the mains voltage already shows a $\mathrm{THD}_{\mathrm{v}}$ of $1.7 \%$. Adverse spikes of $i_{\mathrm{N} 2}$ which can be observed in Fig. 12(b) originate from a non-optimal sector determination of phase $i_{\mathrm{N} 3}$ caused by an inaccurate behavior of one channel of the analog measurement circuitry. It is expected that with an enhanced analog stage this spikes can be avoided leading also to a slight $\mathrm{THD}_{\mathrm{I}}$ improvement.

Fig. 13(a) shows the measured currents $i_{\text {pos }}, i_{\mathrm{L}}$ and $i_{\mathrm{cp}}$ for an output power of $P_{\mathrm{o}}=10 \mathrm{~kW}$. The current $i_{\mathrm{L}}$ is defined by the voltage difference between the output of the diode bridge

(a)

(b)

Fig. 12: Measurement results taken from the laboratory prototype an output power of 10 kW ; (a) Transition from passive diode mode operation ( $\mathrm{THD}_{\mathrm{I}}=$ $46.4 \%, \lambda=0.905$ ) to active current shaping using the proposed FCC, (b) Steady state operation at $P_{\mathrm{o}}=10 \mathrm{~kW}\left(\mathrm{THD}_{\mathrm{I}}=2.3 \%, \lambda=0.998\right)$.
and the output voltage $V_{\mathrm{o}}$ and shows an average value of $I_{\mathrm{L}, \text { avg }}=18.5 \mathrm{~A}$ and a peak to peak ripple of $\hat{I}_{\mathrm{L}, \mathrm{AC}}=15 \mathrm{~A}$ with characteristic $6^{\text {th }}$ harmonic. In addition to the expected 300 Hz ripple also a 150 Hz variation occurs. This is a result of asymmetrical voltages of the feeding mains and the injection currents $i_{\text {cp }}$ and $i_{\text {cn }}$ have to compensate this effect as shown in Fig. 13(a). Fig. 13(b) shows the situation for $P_{\mathrm{o}}=2.6 \mathrm{~kW}$ where in passive operating mode a discontinuous current $i_{\mathrm{L}}$ would occur. Negative values of $i_{\mathrm{L}}$ can be read which is injected by the currents $i_{\mathrm{cp}}$ and $i_{\mathrm{cn}}$ - the ripple current results in a circulating current in $L_{\mathrm{DC}}, C_{\mathrm{o}}$ and the two half-bridges which reduces the efficiency at light-load or no-load condition.

The measured efficiency rates $\eta_{\text {meas }}$ of the total converter are shown in Fig. 14(a) as a function of output power $P_{\mathrm{o}}$ in comparison with the calculated efficiency $\eta_{\text {calc }}$. An excellent measured efficiency of $97.8 \%$ can be read at $P_{\mathrm{o}}=10 \mathrm{~kW}$. The efficiency of the passive diode rectifier for the same load conditions has been obtained with $98.7 \%$. Fig. 14(b) depicts the measured input current quality $\mathrm{THD}_{\mathrm{I}}$ and power factor $\lambda$ as a function of output power $P_{\mathrm{o}}$. The built rectifier system achieves a $\mathrm{THD}_{\mathrm{i}}$ below $5 \%$ down to $P_{\mathrm{o}} \approx 3 \mathrm{~kW}$. Also a power factor above 0.95 is measured for an output power above


Fig. 13: Measured currents $i_{\text {pos }}, i_{\mathrm{L}}$ and $i_{\mathrm{cp}}$ for an output power of (a) $P_{\mathrm{o}}=$ 10 kW and (b) $P_{\mathrm{o}}=2.6 \mathrm{~kW}$.
$P_{\mathrm{o}} \approx 2.2 \mathrm{~kW}$. The constructed FCC shows a good performance even for half load condition $\left(P_{\mathrm{o}}=5 \mathrm{~kW}\right)$ where a $\mathrm{THD}_{\mathrm{I}}$ of $2.7 \%$ and a power factor of $\lambda=0.992$ can be measured at a good efficiency of $\eta_{\text {meas }}=97.5 \%$. It has to be noted that the presented prototype converter neither has been optimized for power density nor for efficiency. A further improvement of the efficiency would be achievable based on an optimized design.

## VI. Conclusion

The basic operating principle of the three-phase rectifier circuit using a FCC is verified by the constructed laboratory prototype with a power rating of 10 kW . Although the system is not optimized for efficiency and a rather small switching frequency of 10 kHz is used an efficiency of $97.8 \%$ is achieved. The input currents show a $\mathrm{THD}_{\text {I }}$ of only $2.3 \%$ and even at $30 \%$ of output power a $\mathrm{THD}_{\text {I }}$ of $\approx 5 \%$ is measured. The system shows several degrees of freedom which allow to optimize it in different directions. The topology allows the extension of an existing passive rectifier circuits with dc-side located smoothing inductor to a low-harmonic input stage but in contrast to standard active three-phase rectifier systems the rectifier output $V_{0}$ shows no high-frequency CM voltage. Several controllers are required for the proper operation of the rectifier topology which are implemented in a single DSP.


Fig. 14: (a) Measured $\eta_{\text {meas }}$ and calculated efficiency $\eta_{\text {calc }}$ of the laboratory prototype for a mains voltage of $V_{\mathrm{LL}}=400 \mathrm{~V}$. (b) Measured power factor $\lambda$ and input current quality $\left(\mathrm{THD}_{\mathrm{I}}\right)$ as a function of output power.

## References

[1] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics Converters, Applications and Design, NY, Wiley/Academic, 2nd ed., 1995.
[2] B. Singh et al., "A Review of Three-Phase Improved Power Quality ACDC Converters," IEEE Trans. Ind. Electron., vol. 51, no. 3, pp. 641-660, 2004.
[3] J.W. Kolar and T. Friedli, "The Essence of Three-Phase PFC Rectifier Systems - Part I," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 176198, 2013.
[4] N. Mohan, "A Novel Approach to Minimize Line-Current Harmonics in Interfacing Power Electronics Equipment with 3-Phase Utility Systems," IEEE Trans. Power Del., vol. 8, no. 3, pp. 1395-1401, 1993.
[5] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Design and Implementation of a Three-Phase Buck-Type Third Harmonic Current Injection PFC Rectifier SR," IEEE Trans. Power Electron., vol. 28, no. 4, pp. 1608-1621, 2013.
[6] J. C. Salmon, "Reliable 3-Phase PWM Boost Rectifiers Employing a Stacked Dual Boost Converter Subtopology," IEEE Trans. Ind. Appl., vol. 32, no. 3, pp. 542-551, 1996.
[7] H.Y. Kanaan and Al-Haddad, "Three-Phase Current-Injection Rectifiers: Competetive Topologies for Power Factor Correction," IEEE Ind. Electron. Mag., vol. 6, no. 3, pp. 24-40, 2012.
[8] P. Pejovic, "A Novel Low-Harmonic Three-Phase Rectifier," IEEE Trans. Circuits Syst. I, vol. 49, no. 7, pp. 955 -965, 2002.
[9] P. Pejovic, P. Bozovic, and D. Shmilovitz, "Low-Harmonic, ThreePhase Rectifier That Applies Current Injection and a Passive Resistance Emulator," IEEE Power Electron. Lett., vol. 3, no. 3, pp. 96-100, 2005.
[10] H. Yoo and S. Sul, "A New Circuit Design and Control to Reduce Input Harmonic Current for a Three-Phase AC Machine Drive System Having a very Small DC-Link Capacitor," in 25th IEEE Appl. Power Electron. Conf. and Exp. (APEC 2010), 2010, pp. 611 -618.
[11] Du et. al., "DC Link Active Power Filter for Three-Phase Diode Rectifier," IEEE Trans. Ind. Electron., vol. 59, no. 3, pp. 1430 -1442, 2012.
[12] M. Hartmann and R. Fehringer, "Active Three-Phase Rectifier System Using a "Flying " Converter Cell," in IEEE Int. Energy Conf. and Exh. (ENERGYCON 2012), 2012, pp. 82-89.
[13] J. W. Kolar, T. Friedli, F. Krismer, and S. D. Round, "The Essence of Three-Phase AC/AC Converter Systems," in Proc. of the 13th Power Electron. and Motion Control Conf. (EPE-PEMC '08), 2008, pp. 27-42.

