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FOR ABSTRACTS

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DEALING WITH UNCERTAINTIES IN ELECTRONIC SYSTEMS SIMULATION

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"Making Things Smarter" is one of the most contemplated requirements for the development of new electronic products. In a hardware perspective, the design of embedded systems (microchips) faces new challenges in increasing functional density and decreasing silicon structural sizes. With the consequence that variations of circuit parameters, input signals, manufacturing processes, etc. from its ideal may receive an increased parasitic impact on the full system behavior. Main research topic within this work is simulation and analysis of electronic designs where system parameters are superimposed by random uncertainties.

Types and classification of occurring uncertainties

Uncertainty is used to summarize effects that cause a circuit to deviate from its ideal behavior. In [1] a classification by a three-dimensional concept regarding their location (*e.g. input values*), cause (*e.g. probabilistic noise*) and nature (*e.g. dynamic process variations*) is presented. However, to improve system characteristics as robustness, performance, confidence, etc. state of the art modeling and simulation methods deal with ubiquitous uncertainties from the very early beginning of the design process.

Modeling of uncertainties and considering them during simulation

A conceptional meta-model to consider uncertainties in computer models is to characterize variations by probability distribution functions [2]. For simulation, classically multi-run methods (Monte Carlo, worst/corner case techniques) are applied, where implicit values within the tolerance interval are selected for each single simulation run. These methods suffer from high computational effort and less expressiveness in the description of attenuation, correlation and dynamic effects.

Semi-Symbolic modeling and simulation methodology

Within our approach using Affine Arithmetic, each uncertainty is modeled by a single abstract symbol $\epsilon_i = [-1, 1]$. These symbols representing a dedicated uncertainty cause are respected during the full simulation and still integrated in computed output forms. Hence, the classical numerical simulation turns to a semi-symbolic methodology. A full Affine Arithmetic form $\hat{x}$ representing a quantity including (several) uncertainties is defined as $x_0 + \sum_{i \in \mathcal{N}_{\hat{x}}} x_i \epsilon_i$, where x_0 is the exact value and x_i scales the deviation intervals symmetrically located around x_0 [3]. Based on this simulation concept the following advantages/enhancements in contrast to multi-run approaches can be identified:

- Output ranges of the model are computed within a single simulation step.
- Correlation of uncertainty causes can be described by multible integration of equal symbols in various Affine Arithmetic forms.
- Description of attenuation and gaining effects (x_i can be either positive or negative).
- Enhanced verification and analysis approaches may be applied (*e.g. assertion based verification, sensitivity and stability analysis, symbol tracking, location of uncertainty hot-spots, etc.*) [4].

As a demonstration example, we modeled a CMOS inverter stage under uncertain structural silicon dimensions of transistor channels (width $W{=}10{\cdot}10^{-6}{+}2{\cdot}10^{-6}\epsilon_1{+}1{\cdot}10^{-6}\epsilon_2$ and length $L{=}0.6{\cdot}10^{-6}{+}0.05{\cdot}10^{-6}\epsilon_1{+}0.06{\cdot}10^{-6}\epsilon_3$). Model equations are adapted from the commonly used BSIM3 model including effects for drain current modes, oxide capacitances, carrier mobility etc. Fig. 1. highlights the resulting bounds of the propagation switching delay (1.97 ns to 3.78 ns). The four displayed traces indicate the variance of the propagation delay under the correlated uncertainty cause ϵ_1 at corner case of ϵ_2 and ϵ_3. The circle in Fig. 1. marks the exact solution ($\epsilon_{1,2,3} = 0$) facing a delay of 2.6 ns. Sensitivity analysis results that the impact of ϵ_1 is dominating. Reducing the associated variance can be a basis for further optimization of the design.

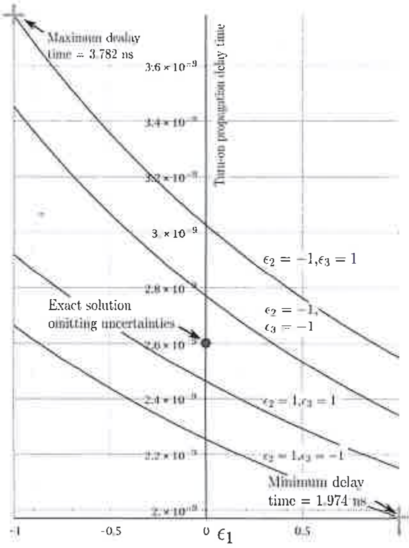

Fig. 1. Propagation delay under uncertain structural transistor dimensions

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