Topology Survey of DC-Side-Enhanced Passive Rectifier Circuits for Low-Harmonic Input Currents and Improved Power Factor

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Abstract

Passive diode bridge (B6) rectifiers are widely used in industry for three-phase AC-to-DC conversion due to simplicity of circuit and design, high efficiency as well as robustness and low cost. For applications which require high input current quality (low THD_i and high power factor) active three-phase rectifiers have to be used which in general are dedicated systems fully replacing the passive rectifier stage. For specific applications (e.g., AC drives) now a concept is attractive which opens the opportunity that an existing B6 rectifier optionally can be upgraded to high quality mains currents if required. This paper provides a concise topology survey and proposes several new circuits regarding such DC-side located add-on options for standard B6 rectifiers. All proposed topologies (introduced and also new circuits) are based on the third harmonic injection principle. The most attractive concepts are analyzed in detail concerning *injection inductor design*, *DC- link capacitor design* and *voltage/current stress* of the required switching semiconductor devices. Measurements of a laboratory prototype finally illustrate good stationary and dynamic performance of the implemented system.

1. Introduction

Passive three-phase B6 diode rectifiers are highly efficient, robust and simple and utilize a very cost attractive mains input stage for feeding the DC voltage link (formed in general by electrolytic capacitors) of, e.g., AC drives or switch-mode power supplies. These rectifiers, consisting of a three-phase diode bridge and a smoothing inductor (mainly located at the DC-side), however, are characterized by a power factor limited to $0.9 \ldots 0.95$ and rather high harmonic input current components (THD_i up to 48%). Using one of the proposed and analyzed circuit concepts based on the third harmonic injection principle [1] (**Fig. 1**), simple diode rectifiers optionally can be enhanced if low-harmonic input currents and unity power factor are required. The concept, moreover, allows improved efficiency of the overall converter system. In contrast to a six switch active rectifier (where the full power has to be processed by the semiconductor switches) the major part of the power here is processed by the passive diode bridge. The optional unit only has to handle approximately $6\% \cdot P_o$ of active and $16\% \cdot P_o$ (given in [2]) of reactive power. Different to known active three-phase rectifiers the proposed add-on concept, however, does not provide any control of the output voltage V_o which is fixed by the mains voltage amplitude (as this is the case for standard B6 rectifiers) and does not show any high frequency common-mode component on its output voltage V_o.

Alternatives for achieving low harmonic input currents and high power factor are AC-side active

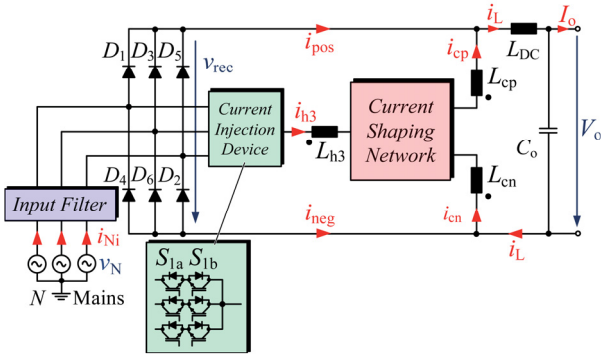

Fig. 1: Basic concept of third harmonic injection for a three-phase rectifier system. The current shaping network generates currents i_{cp} and i_{cn} injected to the DC-side busbars (i_{pos} and i_{neg} resemble 120°-cyclic sinusoidal waveshapes) which finally guarantee sinusoidal line currents i_{Ni}, in which the 60° gaps (being characteristic for passive three-phase diode rectifiers) now are "filled-up" by i_{h3} via the current injection device ($S_{ia,b}$).

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power filters as discussed, e.g., in [3-5]. These concepts in general are characterized by a lower complexity compared to DC side filter structures. E.g. a simple six-switch PWM converter arranged in parallel to a diode bridge rectifier can be used to compensate the rectifiers input harmonics resulting in sinusoidal mains currents of the total system. As both (AC- or DC-side) filtering concepts are suitable for harmonic current suppression of B6 rectifiers, differences are addressed and discussed in [6]. It is stated that besides increased complexity, DC-side active filters show advantages as (i) reduced switch stress, (ii) increased compensation capacity and (iii) improved compensation performance.
Within this work, therefore, several topology variants of DC-side active filters - based on the concept of **Fig. 1** and applicable as "add-on option" for existing diode rectifiers - are proposed and analyzed.

2. Topology Overview

The DC-side active power filter consists of two parts, (i) the *current injection device* and (ii) the *current shaping network* (c.f. **Fig. 1**). The current injection device can be designed in passive (e.g. [7] or [8]) or active configuration. All further proposed topologies in this work assume an active injection device using three bidirectional semiconductor switches (e.g. standard MOSFETs/IGBTs in back-to-back configuration or a parallel arrangement of reverse-blocking IGBTs).

For implementation of the current shaping cell, 7 different circuit combinations are proposed in this paper. Topology A (**Fig. 2a**) is the most basic solution as the optional DC-side power filter is designed as simple "center-tapped" full-bridge stage. The DC-link is formed by two capacitors C_{cp}, C_{cn} in series with midpoint M connected directly to the injection device. This topology yields lowest complexity of all proposed circuits and is suitable for both high and low switching frequency applications. The switches, however, are stressed with the total DC-link voltage $v_{\mathrm{cp}} + v_{\mathrm{cn}}$. For a standard $400\mathrm{V}$ low-voltage mains ($V_{\mathrm{pk}} = 325\mathrm{V}$) and expecting a typical modulation index of 0.8125 ($= 3/2 \cdot V_{\mathrm{pk}}/V_{\mathrm{c}}$) a DC-link voltage of $1200\mathrm{V}$ ($= v_{\mathrm{cp}} + v_{\mathrm{cn}} = 2V_{\mathrm{c}}$) is required for proper operation and hence at least $1700\mathrm{V}$ IGBTs would be necessary in practice. This topology furthermore shows the highest current ripple of all proposed solutions as the total DC-link voltage ($1200\mathrm{V}$) fully is applied to both current injection chokes L_{cp}, L_{cn}.

In order to reduce these drawbacks, a serial connection of two half-bridges appears to be preferable (Topology B, **Fig. 2b**). Both half-bridge legs (connected individually to C_{cp} and C_{cn}) now are stressed by only $600\mathrm{V}$ ($= v_{\mathrm{cp}} = v_{\mathrm{cn}} = V_{\mathrm{c}}$). Hence, $1200\mathrm{V}$ IGBTs or SiC MOSFETs can be used. The two bridge legs can generate bipolar output currents i_{cp}, i_{cn}. The output voltages, however, are uni-polar with respect to the midpoint M (the output voltage of the cell fed by C_{cp}, e.g. is limited to the range $0 \ldots V_{\mathrm{cp}}$). The respective half-bridge connected to L_{cp} has to compensate sinusoidal wave shapes as well as $300\mathrm{Hz}$ current components due to the DC-side smoothing inductance ($L_{\mathrm{DC}} \neq \infty$) current i_{L}. Considering the non-ideal case ($L_{\mathrm{cp}} \neq 0$) the voltage drop across L_{cp} would result in a negative duty cycle, which however is limited to the range $[0...1]$ (0 means upper switch $S_{\mathrm{cp+}}$ opened and lower switch ($S_{\mathrm{cp-}}$) closed and vice versa). Consequently, the voltage drop across L_{cp} and L_{cn} cannot be adjusted by the half-bridges anymore due to duty cycle limitations which lead to unfavourable distortions in i_{pos}, i_{neg} and subsequently results in augmented input/mains current distortions.

This issue can be solved/improved by either increasing the switching frequency f_{s} (which causes depreciated impact of the $300\mathrm{Hz}$ voltage drop due to reduced injection inductance value ($L_{\mathrm{cp}} \rightarrow 0$ for $f_{\mathrm{s}} \rightarrow \infty$)) or, alternatively, by adding an additional constant voltage source in series to each half-bridge power semiconductor connected to the cell midpoint M. The required voltage drop is defined by mains voltages, injection currents, and DC-side smoothing inductance and calculates to

$$v_0 = \hat{V}_N \frac{L_c}{L_{DC}} \left(\frac{3}{2} - \frac{3\sqrt{3}}{\pi} \right) - \frac{\sqrt{3}}{2} \omega L_c \hat{I}_N \tag{1}$$

The proposed additional voltage source could be e.g. implemented as dual active or single active bridge connected to its dedicated half-bridge capacitors (C_{cp} and C_{cn}). With this voltage source, the current shaping cell could operate for a wide frequency range and can still achieve input current distortion of $< 5\%$. Two additional converter stages, however, would mean a high increase in complexity considering voltage control and a vast number of power semiconductor devices (20 switches instead of 4). Therefore, such a concept should not be further analyzed in this paper.

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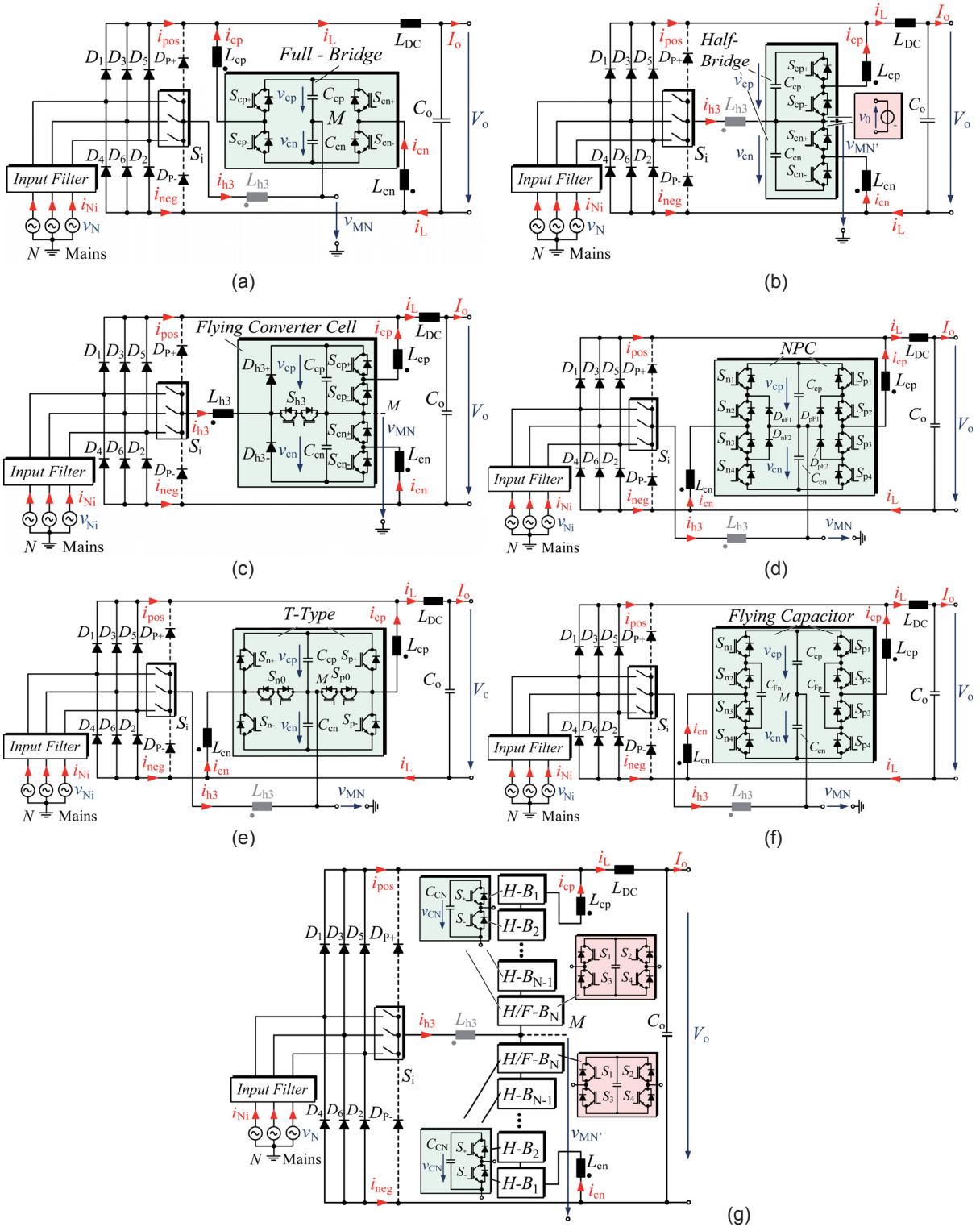

Fig. 2: Add-on circuit extensions for passive diode bridge rectifiers based on the 3rd harmonic injection (THI) principle. (a) THI using full bridge converter cell which yields sinusoidal input/mains currents and shows the lowest complexity of all introduced solutions. (b) THI based on two half-bridges in series connection [9] which show reduced DC voltage levels (~50% compared to the full-bridge solution), however cannot guarantee a $THD_i < 5\%$ for non inductive loads and low converter switching frequency $f_s < 20\text{kHz}$. The behavior of this circuit could be improved by adding two (virtual) negative voltage sources (red) in each path of the half-bridge which, however, means a vast increase in complexity of the overall system. (c) A THI using a "Flying" Converter Cell Topology as introduced in [2],[10],[11] allows further reduced DC voltage levels (~33% compared to the half-bridge solution). (d)-(f) THI based on three-level converter topologies NPC [12], T-Type or Flying Capacitor used for generation of injection currents i_{cp}, i_{cn} and i_{h3}. (g) Multi-Cell implementation can be advantageously used to reduce size of injection inductors and input filter or is applicable for medium voltage rectifier systems.

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Instead, in order to optimize the mentioned current distortions and minimize the DC-voltage level of the shaping cells an unidirectional 3-level bridge can be added, which is directly connected to the current injection network ($S_{\mathrm{i,ab}}$) via L_{h3} (Topology C, **Fig. 2c**) – generally referred to as *Flying Converter Cell* (FCC) Active Rectifier [2]. The midpoint voltage v_{MN} now can be controlled such (by an additional voltage controller) that a reduction of the DC-voltage levels from $600\mathrm{V_{DC}}$ to $400\mathrm{V_{DC}}$ is possible. The additional 3-level bridge furthermore allows voltage balancing of both capacitor branches (C_{cp}, C_{cn}) instead of lossy balancing resistors. Due to reduced DC voltages of the FCC, $600\mathrm{V}$ IGBTs, GaN or SiC switching components are applicable. This topology therefore is a promising for applications which rely on very high switching frequencies (e.g. for systems of very high power density) where switching losses are dominant in comparison to conduction losses. Most obvious drawback of the FCC is its higher complexity, the increased number of switches and control effort compared to Topology A and B.

Input current distortions as appearing for Topology B can be furthermore avoided if the current shaping cell consists of two 3-level converter branches. Feasible circuit opportunities offering satisfying mains input current distortion characteristics may be e.g. the neutral point clamped (NPC), T-Type or Flying Capacitor three-level converter shown in **Fig. 2d-f** (Topologies D, E, and F). All of these proposed 3-level converter cells result in a $600\mathrm{V_{DC}}$ DC-voltage for each cell capacitor.

The Flying Capacitor 3-level converter solution (Topology F), causes almost twice as much capacitor volume than Topologies D and E due to its additional capacitor banks. Moreover, two further voltage sensors and controllers are necessary in order to guarantee fixed DC voltage levels.

The T-Type Converter Cell variant (Topology E) yields low complexity and least number of switches compared to D and F. Different to the bidirectional "midpoint-switches" S_{n0}, S_{p0} where $1200\mathrm{V}$ devices are sufficient, the high-side and low-side semiconductors $S_{\mathrm{n+/-}}$ and $S_{\mathrm{p+/-}}$ have to be implemented as $1700\mathrm{V}$ IGBTs (including switching transients and safety margins) due to required $600\mathrm{V_{DC}}$ DC voltage levels of each cell capacitor as each semiconductor has to block the full DC voltage ($2\mathrm{x}600\mathrm{V_{DC}}$) of the cell which results in reduced attractiveness of this circuit concerning switching losses and switching frequency range of the total active system.

Compared to the Flying Capacitor cell solution, the NPC 3-level converter arrangement (**Fig. 2d**) shows less capacitor bank volume and advantageously $1200\mathrm{V}$ IGBTs or SiC-MOSFETs can be applied for all semiconductors. This topology, however, expects the largest number of semiconductor devices as additional diodes are required to directly clamp the converter to the cell's midpoint (M).

Fig. 2g depicts a THI-based system realized as multi-cell converter stage. The current shaping network consists of $2\mathrm{x}N$ half-bridge cells (marked green) where N denotes the number of half-bridges per injection leg. Optionally, a single switching cell (e.g., the innermost cells connected to the midpoint M can be designed as full-bridge converter (marked red). With this, it is possible to generate an output voltage of the cell chain which may show minor negative values. Consequently, current distortions originated by the voltage across L_{cp}, L_{cn} and duty cycle limitations finally leading to input/mains current distortions as described before can be avoided. This concept (which can also be implemented such, that only two cells, i.e. a full-bridge cell and a half bridge cell are combined), therefore is of interest especially for low switching frequency applications ($f_{\mathrm{s}} < 20\mathrm{kHz}$) or for medium-voltage systems.

Advantageously the N cells are operated in interleaved PWM mode, i.e., the PWM carrier signals have to be phase shifted by $2\pi k/N$ ($k = 1,2,3\ldots N$) resulting in a significant current ripple and/or inductor size reduction due to the ripple cancellation (the maximum current ripple shows a $1/N^2$-dependency). The semiconductor switches of each half/full-bridge are stressed with a DC-link voltage of only $600\mathrm{V}/N$. Therefore, the application of ultra-low-$R_{\mathrm{DS,on}}$-low-voltage MOSFETs would be possible for higher values of N, whereas in case of $N=2$ (or for medium-voltage systems) fast $600\mathrm{V}$-IGBTs, SiC-MOSFETs or GaN power switches are applicable.

Due to the series arrangement, each converter stage has to process the full current i_{cp} or i_{cn}. Even though the rated DC-link voltage of each half-bridge capacitor bank is reduced, its voltage ripple is mainly defined due to the predominant $300\mathrm{Hz}$ current ripple. The required DC link capacitance for each cell hence is increasing for an advanced number of cells to achieve equal relative maximum voltage ripple rate.

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TABLE I: Overview of proposed topologies concerning applying semiconductor device voltage ratings (V_{DS}), applicable devices (Appl. Dev.) and number of switches and diodes (No. of Sw., D.)

	V_{DS}	Appl. Dev.	No. of Sw., D.
Top. A:	1200V	I	4, 0
Top. B:	600V	I, S	4, 0
Top. C:	400V(S) 800V(D)	I, S, G	6, 2
Top. D:	600V	I, S	8, 4
Top. E:	1200V	I	12, 0
Top. F:	600V	I, S	8, 0
Top. G:	600V/N	I, S, G	4N, 0

TABLE II: Calculated current stress of required switches, internal and external diodes of most promising proposed topologies (Top. B-D) for 10kW nominal output power.

	I_{avg}	I_{rms}		I_{avg}	I_{rms}
Topology B (half-bridge con. to L_{cp})					
S_{cp+}	1.1A	2.7A	D_{cp+}	1.1A	2.6A
S_{cp-}	0.7A	1.9A	D_{cp-}	2.3A	4.6A
Topology C (half-bridge con. to L_{cp})					
S_{cp+}	2.1A	4A	D_{cp+}	1.3A	2.9A
S_{cp-}	0.4A	1.5A	D_{cp-}	1.4A	3.5A
(3-level bridge)					
S_{h3}	1.9A	3.5A	$D_{h3+/-}$	0.7A	2.4A

TABLE I summarizes the previously mentioned facts on applicable devices (Appl. Dev.), number of switches and diodes (No. of Sw., D.) and required semiconductor voltage ratings (V_{DS}) for a DC-link voltage (V_c) of 600V (Topology A,B,D-G) or 400V (Topology C). Letters I, S and G denote IGBT, SiC and GaN power devices.

3. Capacitor Bank Volume

As discussed in the previous section, capacitor design appears to be a crucial topic. The capacitor bank volume of the injection cell may connote a critical figure of merit for a volume optimized converter design regarding high switching frequency considerations.

Capacitor volume of each proposed topology is mainly defined by the 150Hz and 300Hz spectral components of the injection current (i_{cp}, i_{cn}) (and therefore nominal output power P_o). Capacitor design considerations for THI systems thus are almost independent of the cells switching frequency f_s but are determined by the appearing low-frequency (150/300Hz) DC link ripple voltage component. Consequently, electrolytic capacitors are used and not foil capacitors which would show much higher voltage ripple due to their lower capacitance. **Fig. 3a** gives a line-up of required capacitor values and volumes (for one capacitor stage C_{cp} or C_{cn}) of all proposed active rectifier add-on solutions for a relative DC link voltage ripple of 5% and a nominal output power of 10kW (considering EPCOS B43501 capacitor series).

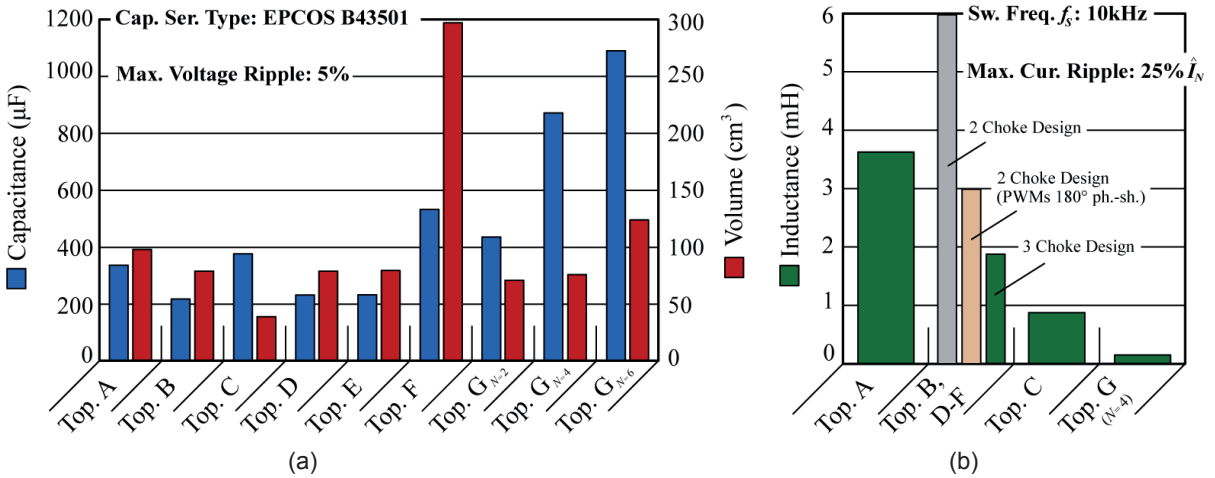

Fig. 3: Topology analysis for 10kW output power of dedicated (a) capacitor design considering EPCOS B43501 for a relative voltage ripple of 5% and (b) inductance design for a switching frequency of 10kHz and a maximum current ripple of 25% of the mains input peak current.

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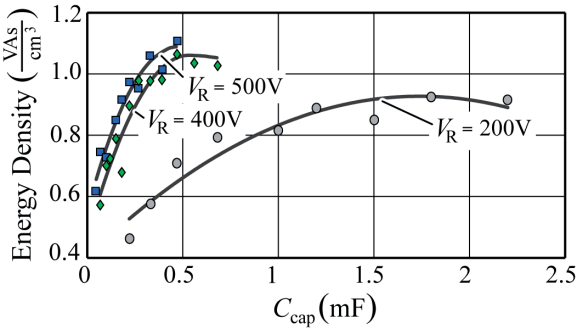

Fig. 4: Energy density analysis depending on rated voltage and capacitance of EPCOS B43501 electrolytic capacitor type series. the maximum energy density can be found for capacitor types at the highest possible voltage level. 400/500V types give much higher Ws/cm^3 than 100/200V capacitors.

As previously mentioned and also stated in **Fig. 3a**, Topology F (Flying Capacitor 3-level assembly) results in highest volume, due to its additional capacitors required for achieving $+V_c$, 0V and $-V_c$ at the output of the converter. Topology A,B and D-F suffer from an increased volume because a maximum voltage of typically ≈450V is given for electrolytic capacitors and hence a series connection is required at the topology-defined DC-link voltage level of 600V. It has to be emphasized that the Flying Converter Cell active rectifier (Topology C) shows the lowest capacitor volume of all discussed topologies. Due to its 400V DC-link a single 450V rated voltage capacitor is sufficient (no capacitor series connection required) which minimizes the total volume of the cell.

EPCOS B43501 capacitor series has been evaluated regarding energy density, rated voltage and capacitance and shows that the maximum energy density can be found for capacitor types at the highest possible voltage level, i.e. 400/500V types give much higher Ws/cm^3 than 100/200V capacitors (**Fig. 4**). A multi-cell arrangement as proposed in **Fig. 2g** therefore tends to lack attractiveness for increased number of cells due to expected growth of capacitor volume.

4. Inductor Design

Design of the injection inductance L_c is performed for 10kW output power which results in inductor peak (neglecting current ripple), rms and avg current values of $12.3A_{pk}$, $6.1A_{rms}$ and $1.64A_{avg}$, respectively (for L_{DC} of 2.25mH).

Results of the inductor design for a switching frequency of 10kHz are given in **Fig. 3b**. Two conspicuities can be observed from this bar plot. Obviously, Topology B, and Topology D-F conform in inductance design characteristics, which is mainly based on parity of their duty cycles (note that three-level bridges primarily act as two level converters if affecting 300Hz filter output current ripple is neglected for design procedure). As illustrated in **Fig. 3b** there are three alternative inductor design procedures which are valid for Topology A,B, and D-G: (i) a standard 2 choke implementation which assumes all PWM signals being synchronized (grey); (ii) as (i) but PWM carrier signals of both injection legs operated at 180° phase shift leading to a 50% reduction of the inductance value; (iii) utilizing an additional choke L_{h3} in the third harmonic injection path (cf. **Fig. 2** - light grey) which allows an additional 40% inductance reduction for each choke (green). As Topology C in any case requires a third inductor due to its 3-level bridge leg connected to the AC-side, the inductor design considers an additional third choke for all remaining topologies too in order to achieve comparable results.

Top. A: Top. B & D-F: Top. C: Topology G (N = 4):

$$L_c = \frac{V_c(M+1)}{6 f_s \Delta I} \quad (2) \qquad L_c = \frac{V_c M}{3\sqrt{3} f_s \Delta I} \quad (3) \qquad L_c = \frac{V_c\left(M\frac{\sqrt{3}}{2} - \frac{1}{3}\right)\left(1 - M\frac{\sqrt{3}}{2}\right)}{f_s \Delta I} \quad (4) \qquad L_c = \frac{V_c}{80 f_s \Delta I} \quad (5)$$

M is the modulation index and defined as 0.8125. It has to be noted that the equations parameter V_c is $400V_{DC}$ considering Topology C and $600V_{DC}$ for Topology A, B, D-G.

5. Current Stress

Current stress calculations have to be accomplished numerically as zero-crossings of i_{cp} and i_{cn} cannot be characterized in a closed analytical way. **TABLE II**, therefore, contains calculated values of the most promising current injection circuits (Topology B and Topology C), considering complexity, semiconductor components, voltage stress of components and capacitor and inductor design for a 10kW output power with a DC-side smoothing inductance L_{DC} of 2.25mH.

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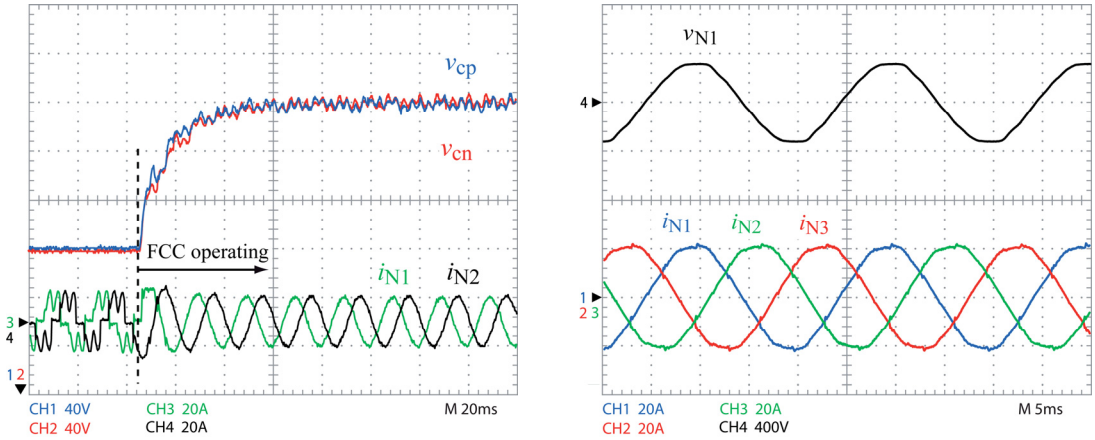

(a) (b)

Fig. 5: Experimental results of a $10\text{kW}/10\text{kHz}$ active rectifier system as published in [10] using FCC topology. (a) Transition from passive to active mode operation at 10kW rated output power. Input current quality improvement from 48% to 2.2%. The measured power factor increases from 0.905 to 0.998. (FCC's DC link voltages v_{cp} and v_{cn} rise up to 400V level (balanced by control). The initial charging process is performed during startup operation. (b) Sinusoidal input currents for activated FCC operation.

6. Experimental Results

Fig. 5 illustrates measurement results taken from a 10kW laboratory prototype system (cf., **Fig.6**) of a passive diode bridge enhanced by "Flying" Converter Cell (FCC) topology (running at a switching frequency of 10kHz) verifying the applicability of the proposed concept as an add-on option for existing passive rectifier systems and demonstrating the proper operation of the designed system.

Fig. 5a depicts the transition from passive to active mode operation of the total rectifier at 10kW rated output power. Input current THD_i is improved from 48% to 2.2% and the power factor increases from 0.905 to 0.998. Mains input currents i_{N1}-i_{N3} show sinusoidal shape according to the mains voltage v_{N1} (**Fig. 5b**).

7. Conclusion

Different types of DC-side enhanced passive rectifier circuits for low-harmonic input currents and improved power factor have been discussed and benchmarked. Voltage/current stress of semiconductor components, number of switches and external diodes and design of capacitive and inductive elements have been chosen as preselecting appraisal criterions. As most promising topologies can be summarized:

- *Topology B :*
  (+) Minimum number of switches.
  (+) Low in complexity.
  (-) Can be used only for switching frequencies >20kHz (low switching frequency requires higher L_c values leading finally to current distortions permitting THD_i > 5%.
  (-) Increased capacitor volume due to the required series connection of electrolytic capacitors.
  (-) GaN not applicable due to its DC-voltage level of 600V. 1200V SiC or IGBTs necessary.

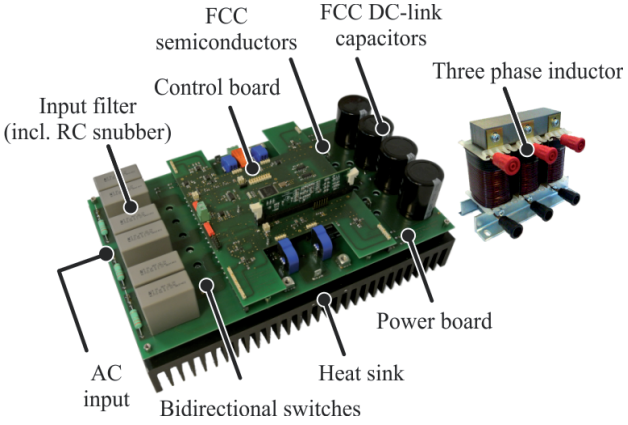

Fig. 6: Laboratory demonstrator of a 10kW active rectifier system based on FCC topology ($400\text{V}_{\text{LL,rms}}$/ 50Hz mains). The powerboard mainly comprises all high voltage components and connectors/power terminals (including, DC Link capacitors, AC side Filter structure, current measurement units,...), IGBTs and corresponding gate drives. The controlboard conveying digital signal processor (DSP), complex programmable logic device (CPLD), overvoltage and overcurrent protection, filter structures etc. A rather small switching frequency of 10kHz has been used as this prototype should serve as a down-sized demonstrator for power levels of $> 200\text{kW}$. Advantageously a three-phase coil can be used for L_{cp}, L_{cn}, L_{h3} to minimize the system volume.

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- *Topology C ("Flying Converter Cell"–FCC):*
  (+) applicable also for lower switching frequencies (IGBTs, higher power levels).
  (+) minimum capacitor bank volume due to reduced DC-voltage of the injection cell.
  (-) Higher complexity.
  (-) Increased number of semiconductor components due to additional 3-level bridge leg.

The inductance design for Topology B can be further optimized if a supplementary coil (L_{h3}) is implemented which noticeably reduces the inductance value of each coil and hence results finally in an improved THD_i.

Topology G (multi-cell implementation) would be interesting for high-power medium-voltage systems with individual $400/800\text{V}$ DC link cells and $600/1200\text{V}$ IGBTs. A modified version based on only $N=2$ cells (400V DC link and 600V IGBTs or GaN-MOSFETs, however, seems to be attractive also for low-voltage mains (400V_{LL}) and will be analyzed in a future paper.

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