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Normally-off GaN-HEMTs with p-type gate: Off-state degradation, forward gate stress and ESD failure

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ABSTRACT

This paper reports an analysis of the degradation mechanisms of GaN-based normally-off transistors submitted to off-state stress, forward-gate operation and electrostatic discharges. The analysis was carried out on transistors with p-type gate, rated for 600 V operation, developed within the European Project HIPOSWITCH. DC measurements, thermal analysis by transient interferometric mapping (TIM), and transmission line pulse (TLP) were used in combination to achieve a complete description of the degradation and failure processes.
The results of this investigation indicate that: (i) the analyzed devices have a breakdown voltage (measured at 1 mA/mm) higher than 600 V; in off-state, drain current originates from gate–drain leakage for drain voltages (V_{DS}) smaller than 500 V, and from vertical leakage through the conductive substrate for higher drain bias. (ii) step-stress experiments carried out in off-state conditions may induce instabilities in both drain–source conduction and gate leakage. Failure consists in the shortening of the gate junction, and occurs at V_{DS} higher than 600 V. (iii) in forward bias, the p-type gate is stable up to 7 V; for higher gate voltages, a time-dependent degradation is detected, due to the high electric field across the AlGaN barrier; (iv) TIM analysis performed under short-circuited load conditions revealed hot spots at the drain side of the channel in the access region, thus indicating that these regions may behave as weak spots under high bias operation. Cumulative device degradation under such repeating pulses has also been revealed. (v) TLP tests were carried out to evaluate the voltage limits of the devices under off-state and on-state conditions. The results described within this paper provide relevant information on the reliability issues of state-of-the-art normally-off HEMTs with p-type gate.

1. Introduction

Gallium nitride represents an excellent material for the fabrication of transistors for application in the power conversion field; transistors based on GaN have superior performance, thanks to the high mobility (>1200 cm^2/Vs) of the bi-dimensional electron gas (2DEG), which results in very low on-resistance (R_{on}). In addition, the $R_{on}Q_g$ product (where Q_g is the gate charge) of GaN transistors is smaller than 1 Ω nC [1], and this results in a significant reduction of switching losses with respect to conventional power devices. Another important advantage of using GaN is the high expected reliability: GaN has a breakdown voltage of 3.3 MV/cm, and – for this reason – transistors with breakdown voltages in the kV range have already been fabricated. By exploiting the outstanding performance of GaN, power converters with efficiency higher than 99% have already been demonstrated [2], thus confirming the excellent potential of GaN for the power electronics field. As indicated in [3], it is the first time (since 60 years) that a new higher performance technology can compete with its silicon counterpart in terms of costs: GaN can be grown heteroepitaxially on a foreign silicon substrate, and can be processed in Si-compatible manufacturing lines. SiC substrates are also used when thermal conductivity and lattice quality (rather than cost) are major needs, such as – for instance – in the aerospace and RF fields.

Thanks to the intrinsic and piezoelectric polarization, GaN transistors are normally-on devices, with typical threshold voltages in the range between −6 V and −2 V. To reach normally-off operation, several approaches have been proposed, including the recess of the AlGaN layer under the gate [4], the use of F-implantation [5], and the use of a p-type gate [1]. The latter approach has the advantage of permitting to reach threshold voltages higher than 1–1.2 V, and to modulate the channel conductivity through hole injection [6].

Over the last three years, several research institutes and industrial partners have been involved in the FP7 project HIPOSWITCH (GaN-based normally-off HIgh POwer SWITCHing transistor for efficient power converters); one of the goals of this project was the development of normally-off GaN power FETs with a p-type GaN gate.

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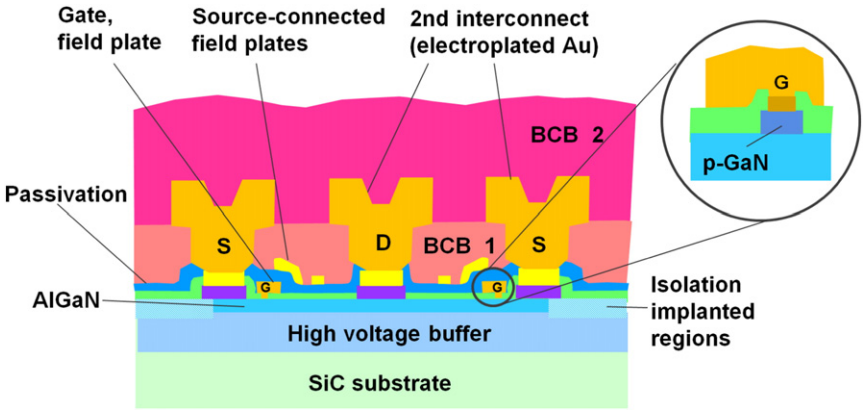

Fig. 1. Schematic cross section of the active transistor region, showing the basic material stack and the principal geometry of the devices studied.

The aim of this paper is to give an overview on the technological steps used for the fabrication of normally-off devices within the HIPOSWITCH project; in addition, we describe the degradation issues of the state-of-the-art transistors delivered at the end of the project. The paper is structured as follows: Section 2 gives a detailed description of the technological steps used for the growth and processing of the devices. Section 3 describes the issues related to self heating; based on Transient Interferometric Mapping (TIM) measurements we present data on the heat distribution, and on the related reliability issues. Section 4 describes reliability limits of the devices, by presenting results on breakdown tests and step-stress characterization carried out in off-state conditions and with a positive gate bias. In addition we present results on the failure mechanisms of normally-off HEMTs submitted to drain–source and gate–source electrostatic discharge (ESD) events.

2. Device fabrication and basic characteristics

For this study we used normally-off AlGaN/GaN HEMTs with p-GaN gate. The high voltage buffer structure is based either on AlGaN back-barrier or on iron compensation doping (GaN:Fe). The GaN-based layers were grown on 3″ n-type or semi-insulating SiC substrates in a multi-wafer MOCVD reactor. The top p-type GaN layer was overgrown in a separate MOCVD reactor, and acts as gate for transistor normally-off characteristic [1]. All remaining p-GaN areas are selectively removed from the wafer surface by dry-etching. RTP annealing of any etch damage has been done at 500 °C. Ohmic source and drain contacts consist of a Ti/Al/Mo/Au metallization, annealed at 830 °C and yield contact resistances <0.4 Ω mm. Au–Ni ohmic contact formation on top of the p-type GaN gates was done at 530 °C. The devices were isolated against each other by means of nitrogen implantation and then SiN_x-

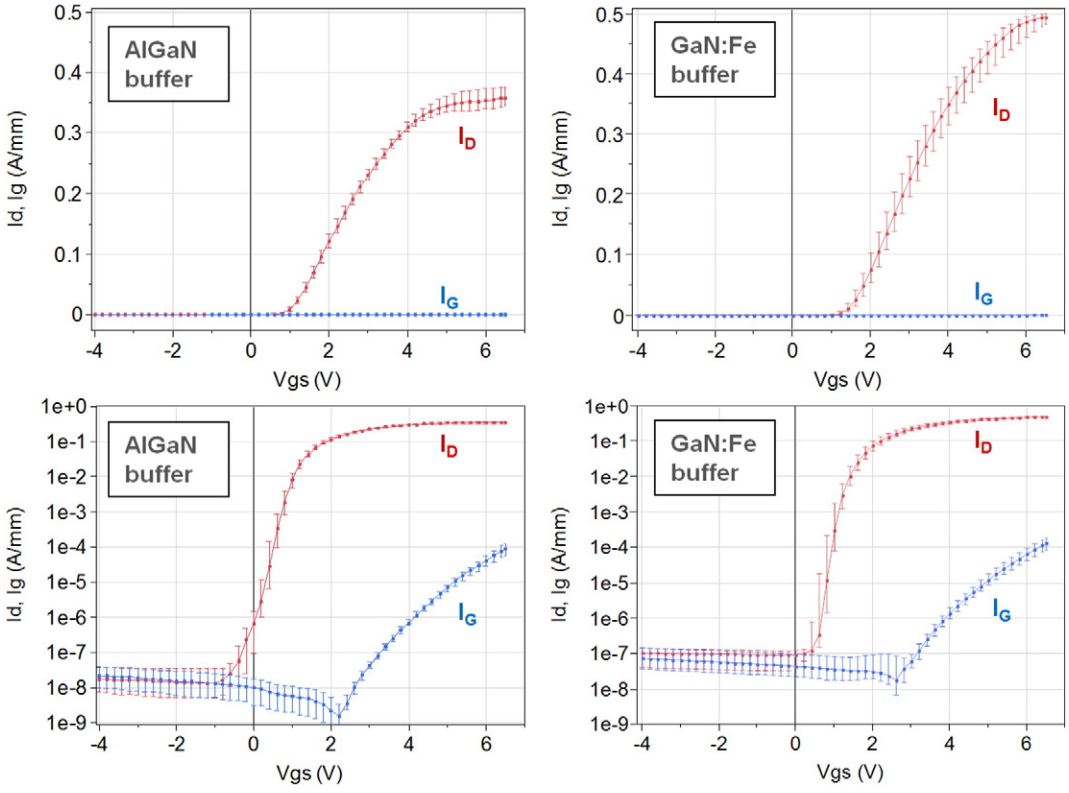

Fig. 2. Transfer characteristics and gate current (linear representation on top, logarithmic representation on bottom) of p-GaN gate HFETs based on an AlGaN buffer (double heterostructure, left) and on an iron-doped GaN buffer (single heterostructure, right). The median currents with quantiles of 30 devices spread over a 3″ wafer are shown. Device gate width is 2.1 μm (left) and 3.2 μm (right). Gate drain separation is 15 μm and $V_{DS} = 10$ V.

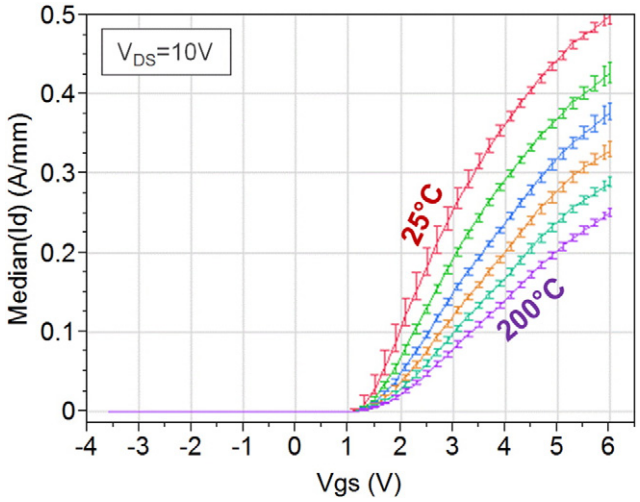

Fig. 3. Transfer characteristics measured at increasing temperature levels (25 °C, 60 °C, 95 °C, 130 °C. 165 °C and 200 °C) on one of the analyzed samples with Fe-doped buffer.

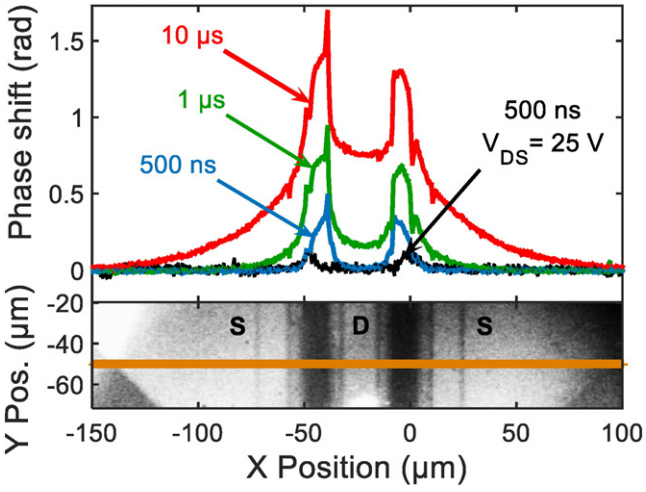

Fig. 5. Top: Phase distribution across the two fingers at different time instants; V_{DS} = 200 V. Average current = 80 mA. The device gate width is 0.25 mm and L_{GD} = 10 µm. Bottom: backside infrared picture of the middle part of the device where the scan was performed.

passivated. After Au based gate, source and drain-finger metallization, the structures were fully covered with 2.6 µm benzocyclobutene (BCB). This insulation layer was opened in the source and drain fingers for electroplating 5 µm Au on the fingers and for the creation of bond pads on top of the BCB layer outside the active transistor area. Crossing of source-connected over gate-connected metal lines allowed the fabrication of multiple-finger transistors. Finally, the devices were fully passivated with a second 6 µm thick BCB layer. To prevent surface sparking at high voltage levels, this BCB layer was opened at the source, drain and gate contact pads only. Fig. 1 shows a schematic cross-section. 70 mΩ/600 V transistors with up to 120 A pulse current and a gate charge as low as 15 nC have been realized with combining 134 gate fingers to a device with 214.4 mm gate width [7,8].

Pattern definition was done by i-line stepper optical lithography. The gate length is 1.3 µm and the source–gate separation is 1.0 µm. The gate–drain distance is L_{GD} = 15 µm. Device characteristics were taken from 2-finger or 8-finger transistors with 0.25 mm, 2.1 mm, 3.2 mm or 8.4 mm gate width. The dc measurements were collected on a large amount (30) of devices per wafer, in order to evaluate the variability of the electrical parameters.

The normally-off behavior of the processed devices is shown in the transfer characteristics in Fig. 2 for both used buffer structures. The threshold voltage is close to 1 V, and remains stable up to 200 °C, as shown in Fig. 3 (see further details on this in [9]). The device on-state is considered for V_{GS} = 5 V, to keep the gate current lower than 20 µA/mm.

The scaling of breakdown voltage with gate–drain separation is 40 V/µm for the AlGaN buffer devices and 50 V/µm for the GaN:Fe-buffer devices. Fig. 4 reports the typical switching characteristics measured (at 600 V) for one of the analyzed devices demonstrating fast switching with dV/dt = 10 kV/µs.

3. Heat distribution and TIM mapping

The characterization of heat distribution and of the thermal properties of the devices was carried out by Transient Interferometric Mapping (TIM) measurements [10]. For TIM measurements devices with 0.25 mm gate width were biased with a constant V_{DS} ranging from 25 V to 200 V and the gate-to-source voltage (V_{GS}) was pulsed from −5 V (off-state) to +5 V (on-state) for 10 µs. The load line was given by a 17 Ω resistor in series with the transistor. This stressing mode mimics a short-circuit load condition with simultaneous high voltage and high current. This is not a state that devices are supposed to reach in normal operation, but it is relevant from a reliability point of view. Indeed nowadays' power devices are expected to survive a few pulses in this condition [11–12]. In TIM, an IR laser beam (λ = 1.3 µm) focused on the device active area from the polished backside probes the change in refractive index induced by temperature. The resulting phase shift is recorded during each single electrical pulse. 20 pulses are applied at the same scanning position to improve the signal to noise ratio. The pulse repetition frequency is low enough (1 Hz) so that the device can cool

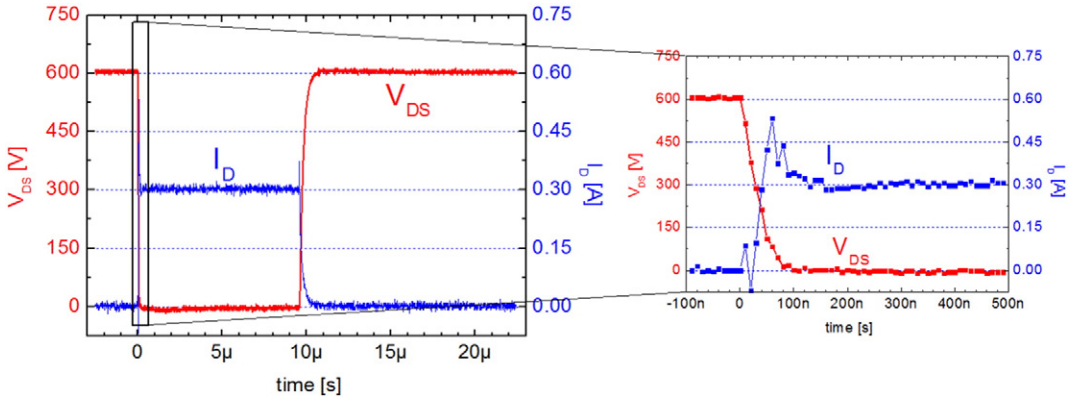

Fig. 4. 600 V/0.3 A switching transient of a p-GaN gate transistor with GaN:Fe buffer on Si–SiC substrate in a set-up with 2 kΩ resistive load. The device gate width is 3.2 µm. The right graph shows the switching event in increased time resolution.

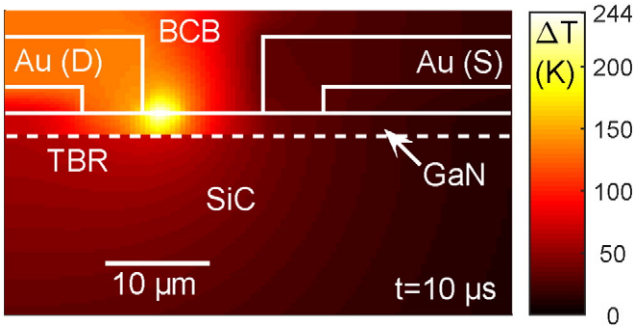

Fig. 6. Temperature simulation results at the end of 10 μs long pulse at 200 V stress. Only half of the structure was simulated.

down to room temperature between consecutive pulses. Under such conditions, the phase shift distribution is directly related to 2D heat energy distribution [10]. Using the TIM data, one can therefore extract the power dissipation distribution and thus 3D temperature distribution can be calculated using thermal modeling. Between line scans performed at different drain biases, 3-terminal DC-IV characteristics were measured to check the device for cumulative damage.

Fig. 5 shows the phase shift distribution across the two device fingers for different time instants during heating at $V_{DS} = 200$ V. In this particular device the two fingers show nearly the same power dissipation but there are devices where the deviation in power dissipation in the two fingers is about 10–20%. Within each of the fingers, the power dissipation distribution is higher towards the drain side of the channel in the access region. This is a common result for drain voltages higher than 50 V. For lower voltages, the power dissipation is mostly seen near the gate location, see also Fig. 5. This supports observations from other groups in various time domains [13–15]. For absolute temperature estimation, thermal simulations were performed taking into account the shape of the power distribution from the TIM data, and thermal parameters including thermal boundary resistance as in [16]. The maximum temperature increase at the end of the 10 μs pulse for $V_{DS} = 200$ V (cf. Fig. 5) is 244 K, see Fig. 6.

The transfer characteristics of the device from Fig. 5, which have been measured after each scan, are presented in Fig. 7 (the total number of pulses at each V_{DS} bias is indicated). The device did not suffer major degradation after the scans. However, some of the studied devices did suffer from cumulative degradation due to the repetitive stressing. Fig. 8 shows transfer characteristics where an increase in the OFF-state drain current is seen after 20,000 pulses at $V_{DS} = 25$ V, as well as an

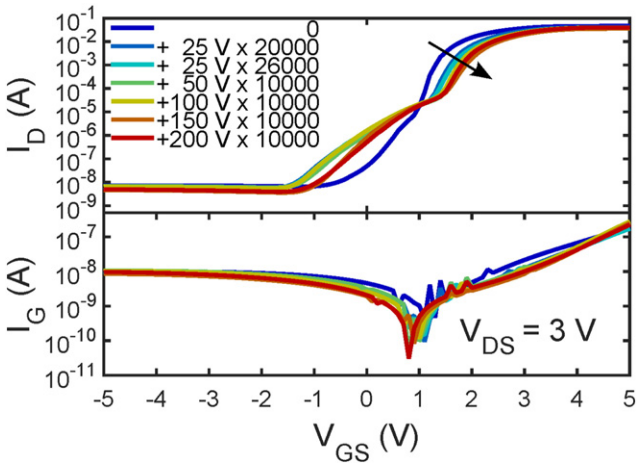

Fig. 7. 3-terminal DC transfer characteristics of the device from Fig. 3 monitored after each TIM scan. The legend lists the TIM scans applied to the device, with V_{DS} and number of pulses; "+" means cumulative stress.

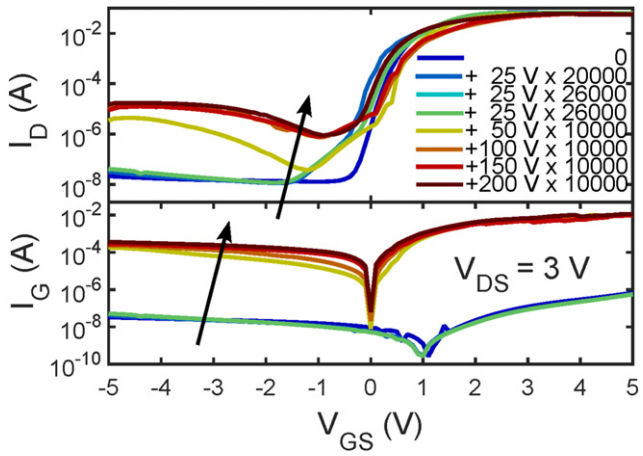

Fig. 8. 3-terminal DC transfer characteristics monitored after each TIM scan of a device with early cumulative damage.

increase of the gate leakage current by several orders of magnitude after the scans at 50 V.

Another type of cumulative degradation effect can be seen in the optical properties of the device: the measured amplitude of the reflected light intensity from the device depends on the total stress. As shown in Fig. 9, the value of the amplitude is nearly constant in the first scan ($V_{DS} = 50$ V), whereas in subsequent scans at higher V_{DS}, two low reflectivity regions are visible. This effect can be produced by delamination of the polymer passivation layer due to mechanical stress caused by localized thermal expansion. However, no direct correlation between the electrical cumulative damage and these optical reflectivity features has been found. This reflectivity change has no direct incidence on the TIM phase signal, except for a decrease of the signal to noise ratio. When the reflectivity becomes very low, spatially localized artifacts can indeed appear in the phase signal.

Finally, in some cases, the devices have experienced destructive thermal breakdown during TIM scans. Fig. 10 shows the drain current and gate voltage waveforms of a destructive pulse where the failure occurs at $t = 2$ μs during application of a first pulse at $V_{DS} = 200$ V. Fig. 11 is the optical picture from the topside after this catastrophic failure showing metal burnout.

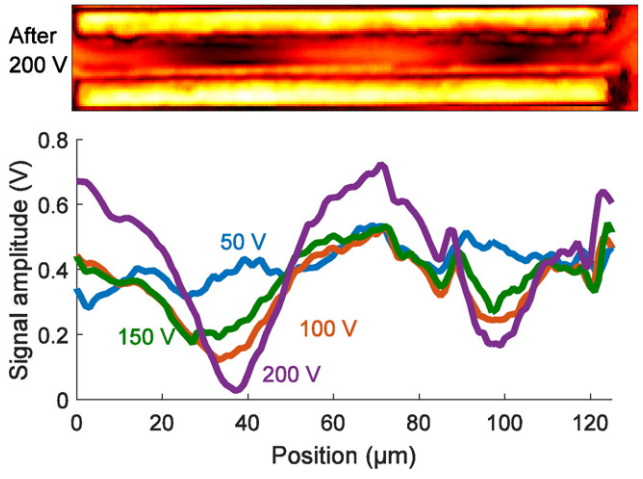

Fig. 9. Top: 2D reflectivity scan after cumulative damage after TIM scan at $V_{DS} = 200$ V. The yellow parts are the high reflecting source and drain contacts. Bottom: Line reflectivity scan after TIM scans at different V_{DS}, showing the evolution of the cumulative damage due to passivation layer delamination.

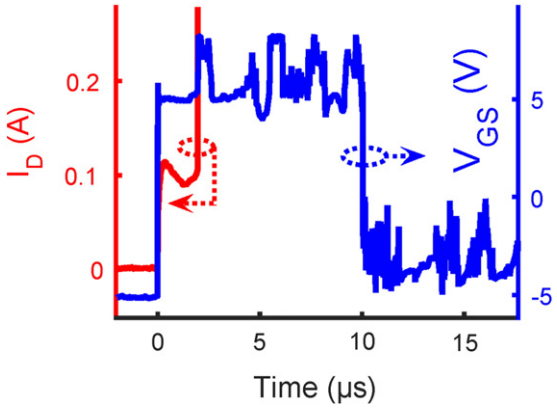

Fig. 10. Drain current and gate voltage waveform during single shot damage of a device (V_{DS} = 200 V).

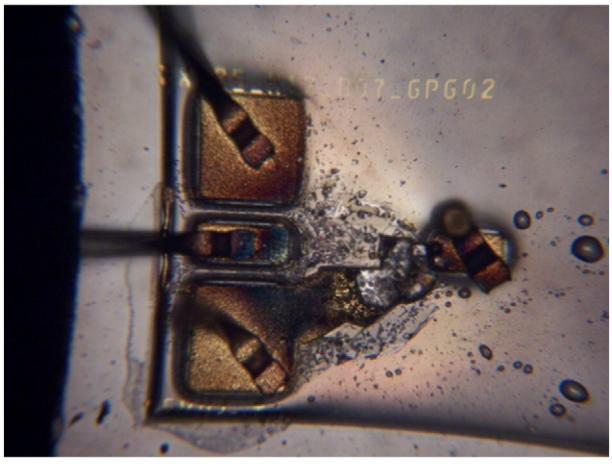

Fig. 11. Top-side view of a typical single shot damage of a device.

4. Reliability issues

This section reports on the results of the stress tests carried out in the off-state and with a positive gate voltage on the devices. In addition, we report representative results on the failure mechanisms of normally-off HEMTs submitted to ESD pulses.

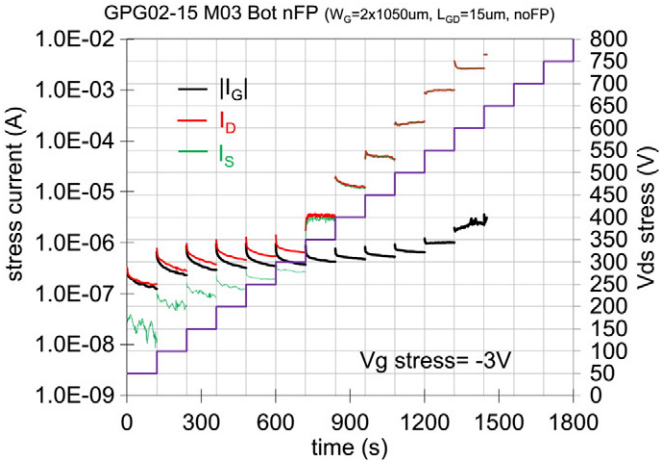

Fig. 13. Variation of gate, drain and source current during off-state step stress for one of the analyzed devices. The device gate width is 2.1 mm. The device has a double heterostructure buffer.

4.1. Off-state degradation

Before the execution of the off-state stress tests, the leakage characteristics of the devices were characterized by dc measurements. Fig. 12 reports representative results, showing the variation of the gate, drain, and source current with increasing drain bias for the devices with double heterostructure and with Fe-compensated buffer; gate voltage was fixed to −3 V (corresponding to off-state) for the execution of the measurements. The devices under tests have a gate–drain spacing of 15 μm. For the DH devices, for low and moderate drain voltages (V_{DS} < 400 V) drain current mostly originates from the leakage of the reversely-biased gate junction. When the drain bias exceeds 400 V, drain–source leakage shows a considerable increase, thus giving the dominant contribution to drain current (it is worth noticing that the breakdown current remains below 1 mA/mm [17] in the whole analyzed voltage range). A source–drain leakage path can either go via the buffer layers, indicating punch through [18,19], or vertically through the GaN layers and the (conductive) substrate. The vertical leakage current measurements on separate structures on the wafer (not shown here for sake of brevity) reveal the vertical leakage path via the conductive substrate as dominant source–drain path [8]. On the other hand, the devices with Fe-compensated buffer has a better confinement

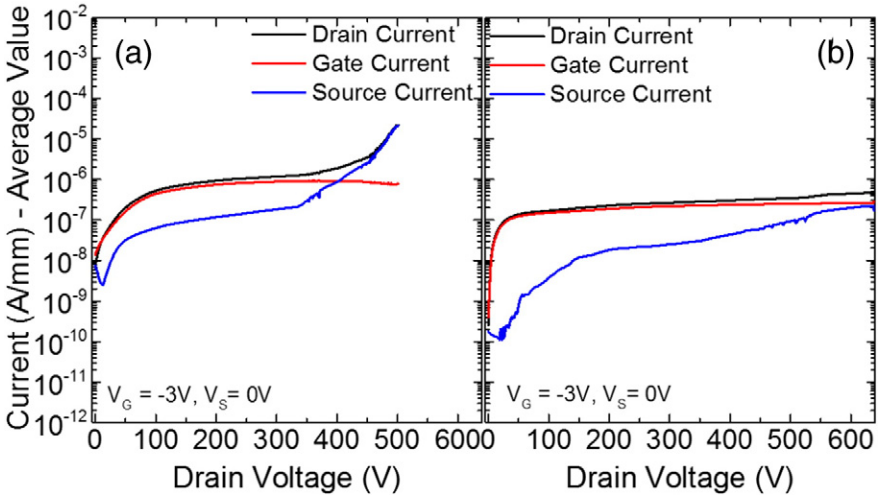

Fig. 12. Non-destructive breakdown characterization (left) on a device with double heterostructure and (right) on a device with Fe-compensated buffer. Each curve is the average on 8 devices.

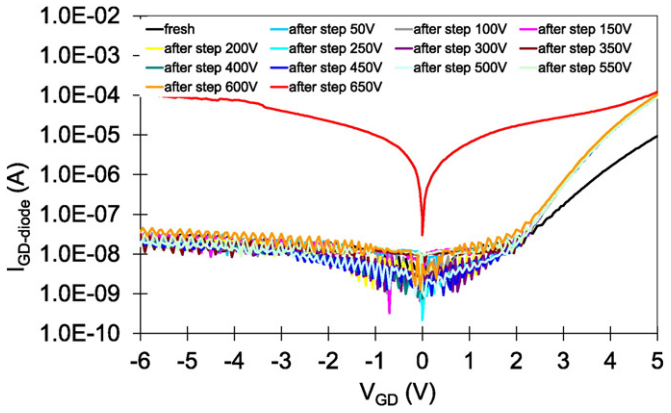

Fig. 14. Current–voltage curves measured during the step-stress in Fig. 11. The device has a double heterostructure buffer.

and isolation, and drain leakage remains well below 1 μA/mm up to $V_{DS} = 650$ V.

After this preliminary characterization of the sub-threshold leakage characteristics, we carried out a set of step-stress experiments to evaluate the stability of the devices under off-state conditions. The tests were executed with a negative gate voltage of −3 V (consistently with the results in Fig. 12), by increasing the drain bias by 50 V every 100 s until the failure. Representative results are shown in Fig. 13; during the initial stages of the step-stress experiment ($V_{DS} < 300$ V), source current is low, while drain current is almost equal to gate leakage (as shown also in Fig. 13). During each stage of the step-stress, gate current shows a gradual decrease, that can be ascribed to the trapping of electrons in the region under the gate [20–21]. On the other hand, for stress voltages higher than 400 V drain–source leakage becomes dominant, and the measurements reveal an increase in the noise superimposed to drain current. Catastrophic failure occurs at $V_{DS} = 650$ V for this specific device.

The I–V curves of the gate diode were monitored after the execution of each stage of stress; the results (Fig. 14) indicate that the gate–drain diode is stable up to a stress voltage of $V_{DS} = 600$ V. A sudden degradation of the devices was found only for higher stress voltages, resulting in a significant increase in gate leakage and in the failure of the devices. The results described above indicate that the analyzed device technology is stable up to 600 V under dc conditions, in the off-state.

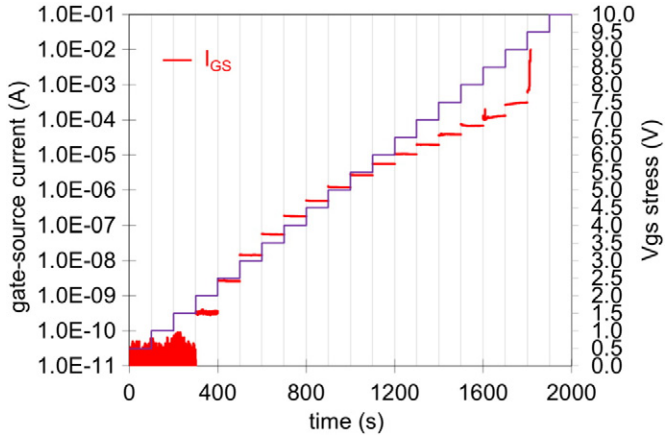

Fig. 15. Results of a step-stress experiment carried out on one of the analyzed samples, by submitting the gate–source junction to increasing positive voltage levels. The device gate width is 0.25 mm. The device has a single heterostructure buffer.

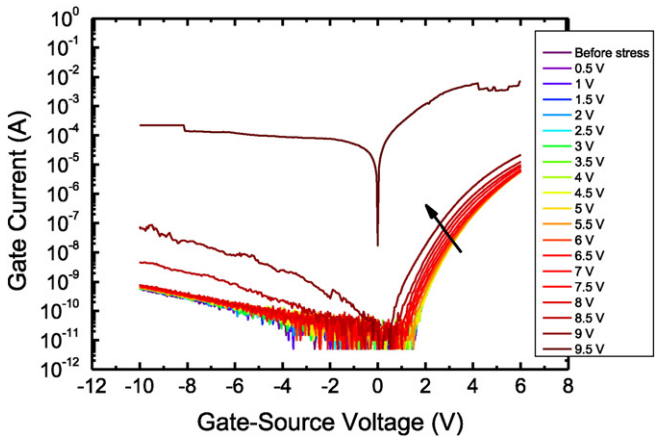

Fig. 16. I–V curves of the gate–source diode of a sample submitted to a step-stress with increasing (positive) gate voltage (same sample as in Fig. 13). The device has a single heterostructure buffer.

4.2. Degradation of the gate junction under forward bias

The devices analyzed within this paper have a p-type gate material; so far, no extensive analysis of the degradation of the gate junction of normally-off HEMTs with p-type gate has been published in the literature. For this reason, we analyzed the stability of the gate diode by means of a set of positive V_{GS} stress tests. A preliminary step-stress experiment was carried out by positively biasing the gate–source junction (with floating drain); the voltage was increased by 0.5 V every 100 s. The results (Figs. 15 and 16) indicate that the gate–source diode remains stable for stress voltages smaller than 7 V, i.e. within the operating limits of the analyzed devices. Higher stress voltages were found to induce an increase in the noise superimposed to stress current (see Figs. 15 and 16 for stress voltages higher than 7 V), and the increase in the reverse and forward leakage current of the gate junction (Fig. 16).

To better investigate the physical origin of the degradation of the p-type gate junction under forward bias, we carried out a set of constant voltage stress tests; the stress voltage was fixed to 8.5 V, and several devices coming from the same wafer were stressed. Fig. 17(a) reports the variation of gate current measured on one representative device: during the constant voltage stress, gate current showed a step-like variation (two main steps are visible in Fig. 17(a)), and increased from 4×10^{-5} A/mm (measured at the beginning of the stress test) to 6×10^{-4} A/mm (measured after 1000 s). The device in Fig. 17(a) showed a catastrophic failure after 6300 s of stress. EL micrographs collected at different times (t_1 and t_2, see Fig. 17(b) and (c)) indicated that the step-like increase in gate leakage corresponds to the generation of hot-spots, i.e. of localized defective paths. This degradation mechanism can be due to the time-dependent degradation of GaN/AlGaN heterostructure (see [20–22]), to the time-dependent breakdown of the dielectric in proximity of the gate, or to the crowding of gate (forward) current in proximity of localized paths. For longer stress times, a catastrophic failure is observed (Fig. 17(a)), possibly indicating a time-dependent breakdown. The time to failure (TTF) was found to be Weibull distributed (not shown here for sake of brevity), with a shape parameter $\beta = 0.6$.

4.3. ESD failure

Other relevant failure mechanisms can occur when ESD pulses are applied to the gate–source junction or to the drain terminal. These conditions were analyzed by carrying out set of ESD tests, by using a custom transmission line pulser (TLP) with pulse width of 100 ns. The TLP tests were carried out in two different configurations, i.e. by applying ESD

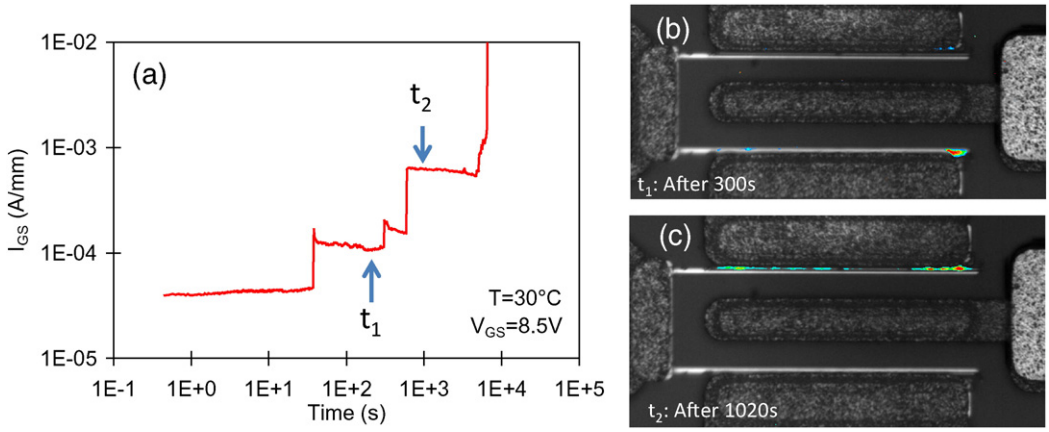

Fig. 17. (a) Variation of gate-current during the execution of a constant voltage stress with positive bias on the gate junction. Panels (b) and (c) represent false-color images of the EL signal measured at two different moments of the stress test. The device has a single heterostructure buffer.

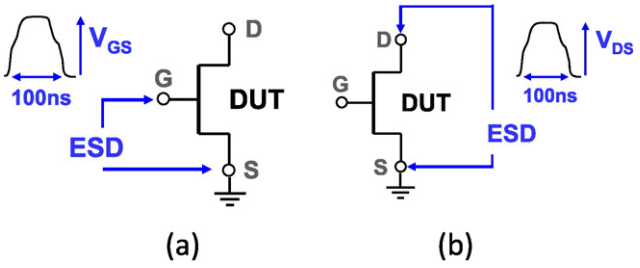

Fig. 18. Schematic representation of the conditions used for the TLP testing of the devices.

pulses on the gate–source diode, with floating drain (Fig. 18(a)), and by applying positive bias pulses on the drain terminal, with grounded source and floating gate (Fig. 18(b)). Several test structures (at least 5 per wafer) were tested to evaluate the uniformity of the failure modes and mechanisms.

Fig. 19 reports the results of TLP tests carried out in reverse-bias conditions on the gate–source diode; the gate junction remains stable until the failure, which occurs around $V_{GS} = -230$ V. The micrographs collected after failure indicate the existence of two different damaged regions. Such regions are possibly located in correspondence of pre-existing localized defects, either depending on the process [20] or on the presence of dislocations under the gate edge [23]. The results in Fig. 19 suggest that failure possibly occurs at the source-side of the gate, which is subject to high electric field, and then the damage extends to the whole source–drain area due to the high dissipated power.

Fig. 20 refers to the case where the TLP pulses are applied between drain and source with gate floating; the device has a threshold voltage $V_{th} = 1$ V, and has a normally-off behavior. However, when fast pulses are applied to the drain, the gate voltage can increase above V_{th} due to the capacitive coupling between the gate and drain terminal, thus turning on the devices. For this reason – when tested with floating gate – the transistor can reach current levels in the order of 2–4 A. The failure is reached – possibly due to the high dissipated power – for drain voltages in excess of 450 V. It is worth noticing that the sub-threshold drain source leakage remains stable and smaller than 100 nA until the failure.

5. Conclusions

In summary, we have described the technological steps used within the HIPOSWITCH project for the fabrication of normally-off transistors with p-type gate. In addition, we have presented an extensive analysis of the thermal properties and of the robustness of these devices, that have been submitted to off-state stress, forward gate bias stress, and electrostatic discharges. More specifically: (i) TIM analysis revealed the presence of hot spots at the drain side of the channel in the access

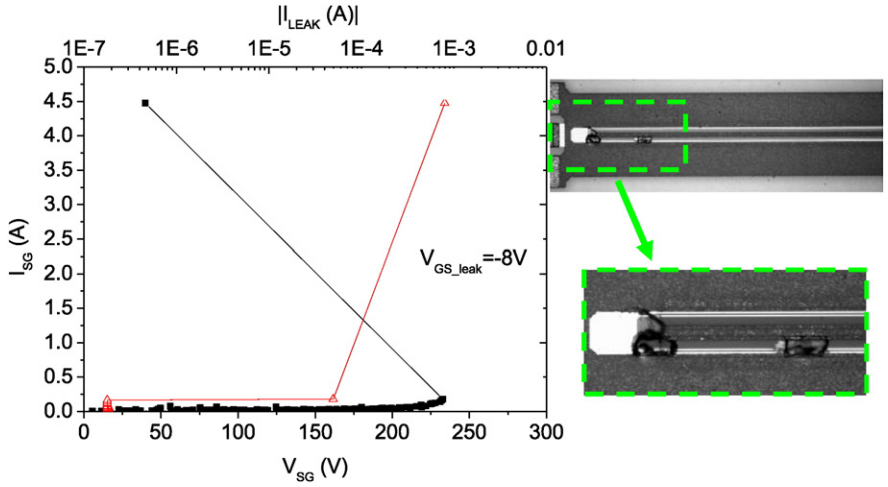

Fig. 19. Results of TLP testing carried out by pulsing the gate–source junction, with floating drain. Gate-pulse current and voltage in black. The gate leakage current I_{leak} for $V_{GS} = -8$ V (red) is plotted against the gate pulse current after every pulse. The device gate width is 3.2 mm. The device has a single heterostructure buffer.

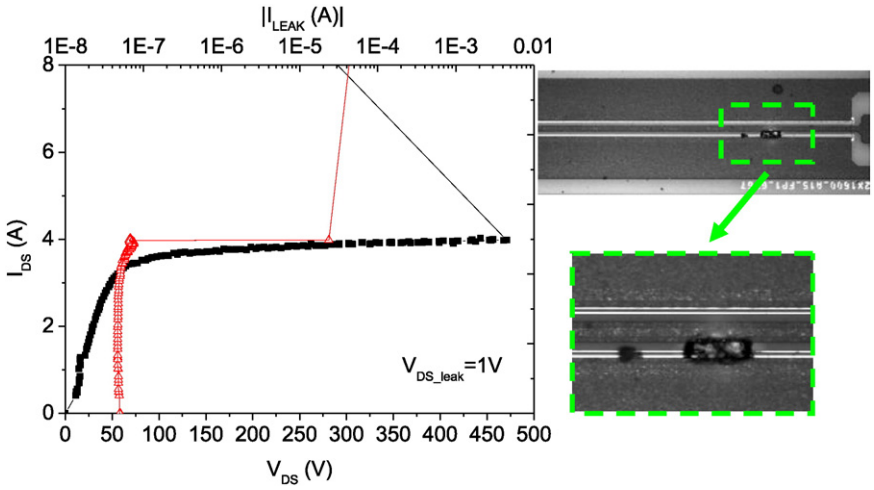

Fig. 20. Results of TLP testing carried out by pulsing between drain and source, with floating gate. Drain-pulse current and voltage in black. The drain leakage current I_{leak} for $V_{DS} = 1$ V (red) is plotted against the drain pulse current after every pulse. The device gate width is 3.2 mm. The device has a single heterostructure buffer.

region. (ii) The analyzed devices have a breakdown voltage higher than 600 V, as demonstrated by dc breakdown measurements and by constant voltage stress tests. (iii) The p-type gate shows a significant degradation only for voltages higher than 7 V. The degradation process is time-dependent, and is ascribed to the generation of defects within the AlGaN layer, that is subject to high electric fields. (iv) TLP tests carried out by pulsing both the gate and the drain allow identifying the operational limits of the devices in pulsed operation. The results presented within this paper provide information on the properties and technological issues of state-of-the-art transistors for application in power electronics. Future investigations will aim (i) at evaluating the impact of the buffer/substrate structure on the thermal performance of the devices; (ii) at understanding the correlation between the structural properties of the p-GaN/AlGaN layers and the related robustness, through specific testing; (iii) at investigating the impact of processing, layout and geometry on the electrical performance, breakdown and ESD robustness of the devices.

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