Silicon-based RF ICs up to 100 GHz: Research Trends and Applications

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Abstract

This paper presents recent advances in circuit design which evaluate the high-speed and low-power potential of state-of-the-art CMOS and SiGe bipolar technologies.

In 0.13 μm CMOS a 17 GHz ISM/WLAN RF front-end with only 130 mW power consumption is described. An injection locked frequency divider with a power consumption as low as 3 mW at 40 GHz is presented. A fully integrated 2:1 multiplexer IC which operates up to 50 Gb/s data rate has been realized in CMOS.

A 100 Gbit/s amplifier in a 200 GHz/275 GHz f_T/f_{max} SiGe bipolar technology with 16 dB gain has been realized. Finally, a 65 GHz - 95 GHz double-balanced mixer for 77 GHz automotive radar applications is discussed.

1 Introduction

Current indium phosphide (InP) bipolar integrated-circuits support high-performance mixed-signal applications at frequencies up to 200 GHz and beyond [1, 2]. The high cut-off frequencies and high breakdown voltages present a unique combination which addresses some major issues. In the meantime, silicon bipolar and CMOS technologies are not standing still. Silicon germanium (SiGe) has brought substantial improvements in bipolar circuit performance [3, 4, 5, 6, 7]. Recently, CMOS is capturing a significant portion of wireless RF and wireline applications with the promise of lower costs and increased integration scale at highest frequencies [8, 9, 10, 11].

This work summarizes recent circuit results in 0.13 μm standard bulk-CMOS and in a production-near 200 GHz/275 GHz f_T/f_{max} SiGe bipolar technology.

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2 A 17 GHz ISM/WLAN RF front-end with only 130 mW power consumption in 0.13 μm CMOS

With growing interest in broadband wireless communication systems and faster and high-performance transceivers at data rates of 100 Mbit/s to 1 Gbit/s and beyond, submicron CMOS is particularly attractive for RF and digital baseband processing because of its low power consumption and high integration scale. Emerging short-range applications, such as a high-speed wireless USB 2.0 interface for example, will rely on a low power consumption for mobile systems.

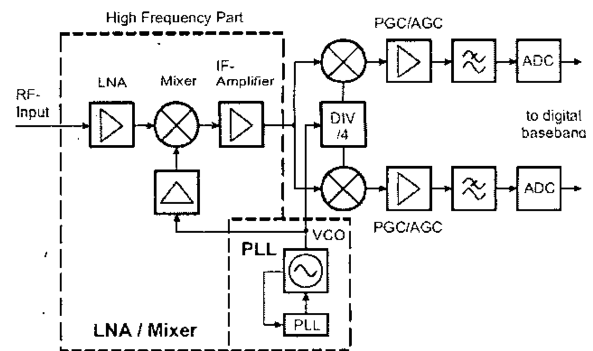
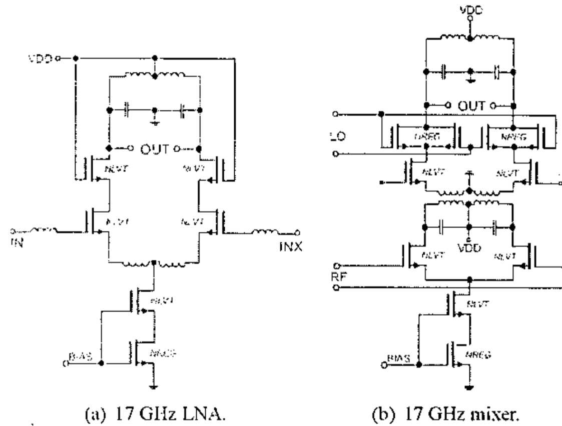


Figure 1: 17 GHz ISM/WLAN RF frontend block diagram [12, 13].

Fig. 1 shows the block diagram of an integrated RF frontend for 17.1-17.3 GHz ISM band application. The high frequency part of the RF transceiver consists of a LNA and mixer [12] and a high-performance PLL [13]. The concept of the dual conversion (Fig. 1) results in a large

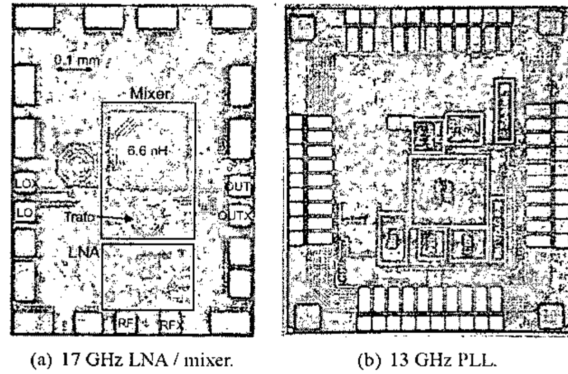
frequency separation between the RF and LO frequencies and avoids the generation of I/Q signals at the first LO frequency.
LNA and mixer design is one of the main challenges, since this circuit determines the total gain, noise figure and linearity performance of a receiver. Fig. 2 shows a simplified schematic diagram of the 17 GHz LNA and mixer in 0.13 μm CMOS.



(a) 17 GHz LNA. (b) 17 GHz mixer.

Figure 2: 17 GHz LNA / mixer schematic diagram [12].

The LNA core in Fig. 2(a) consists of a cascoded, inductively degenerated common source input stage. Inductive degeneration is employed at the common source node of the LNA to achieve a real valued input impedance and low noise figure. The LNA-output is loaded by an integrated LC-tank to increase the gain. Due to the high frequency of 17 GHz all inductors can nicely be integrated without significant area penalty (see chip photograph Fig. 3(a)). A simplified schematic diagram of the mixer is shown in Fig. 2(b). The classical Gilbert-type mixer was preferred to achieve acceptable gain, low noise figure and high linearity. To overcome problems caused by the low supply voltage of 1.5 V in 0.13 μm CMOS, a fully differential integrated transformer was connected between the input transconductance stage and the mixer switching pairs. This topology effectively doubles the voltage headroom available for the circuit design and enables the insertion of cascode transistors to improve the linearity and to control the current in the mixer switching stage. Fig. 3(a) shows the chip photograph of the LNA / mixer. The block diagram of the LNA / mixer is shown in Fig. 1.
In Tab. 1 the measured performance of the 17 GHz LNA / mixer is summarized.
The block diagram of the PLL is shown in Fig. 4. The PLL is completely integrated including VCO, prescaler, phase frequency detector, charge pump, loop filter, biasing, delta-sigma modulator and a JTAG controller [13]. The PLL uses a multi-modulus prescaler with a division rate of 212...217 to allow effective fractional-N synthesis and delta-sigma modulation. Aiming at a fully integrated high performance 17 GHz transceiver including LNA and output driver, special care was invested to avoid substrate crosstalk, so a differentially tuned LC-VCO was implemented.



(a) 17 GHz LNA / mixer. (b) 13 GHz PLL.

Figure 3: 17 GHz LNA mixer and 13 GHz PLL chip photograph [12, 13].

Table 1: 17 GHz LNA / mixer measurement results [12].

Parameter	Value
Power supply	1.5 V
Total power consumption	70 mW
LNA power consumption	5.2 mW
Mixer power consumption	27 mW
LO-Driver power consumption	12 mW
IF-Amplifier power consumption	25.8 mW
IF frequency	3.4 GHz
LO frequency	13.95 GHz
RF frequency	17.35 GHz
Power gain	34.7 dB
Noise figure SSB	6.6 dB
CP_{1dB} (input)	-39 dBm
IIP3	-34.4 dBm
3 dB bandwidth	200 MHz
Testchip die area	0.88 mm^2
Technology	0.13 μm CMOS

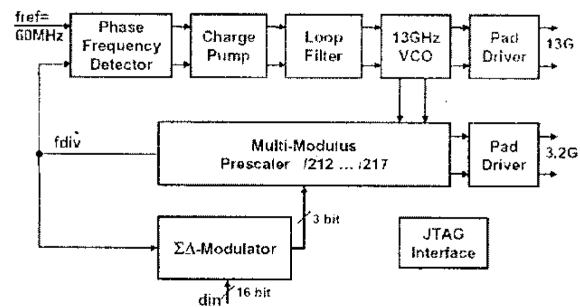


Figure 4: 13 GHz PLL block diagram [13].

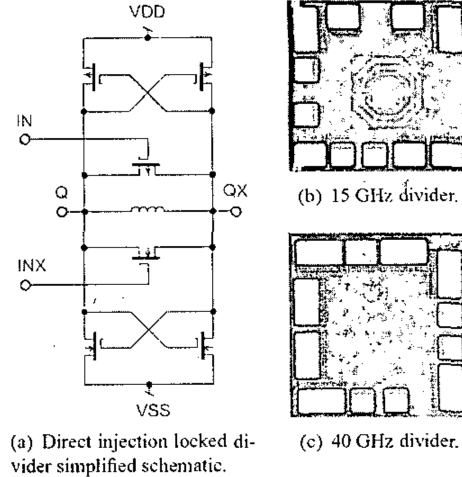
Table 2: 13 GHz PLL measurement results [13].

Center frequency	13 GHz
VCO tuning range	8 %
Reference frequency	60 MHz (64 MHz for N=200)
Inband phase noise (@ fvco/4)	-100 dBc/Hz
RMS Phase error (@ fvco/4) (10kHz to 100MHz)	1.6 deg (N=214.5044) 3.0 deg (N=214.992)
Power supply	1.5 V
Total Power consumption VCO Div/4 Prescaler Loop Filter Charge pump Others. incl. digital	60 mW 5 mW 40 mW 1 mW 5 mW 3 mW 6 mW
Testchip die area	1.8 mm by 1.6 mm
Technology	0.13 μm CMOS

In Tab. 2 the performance of the PLL is summarized [13]. The total power consumption of LNA / mixer and PLL is only 130 mW in 0.13 μm CMOS at 17 GHz.

3 40 GHz, 3 mW low-power injection locked frequency divider in 0.13 μm CMOS

RF Phase locked loops are widely used in wireless and wireline applications as frequency synthesizers or clock sources. Crucial high frequency PLL-components are the voltage controlled oscillator (VCO) and the high frequency dividers. Main concern for VCO-design is low phase noise and low power consumption. Main concern for the frequency divider is lowest power consumption and high frequency capability. High frequency dividers can be realized using CML-logic, using dynamic logic, using a Miller divider or through the injection locking of oscillators. Miller-dividers and CML dividers have been realized up to very high frequencies, unfortunately with high or very high power consumption. Dynamic logic frequency dividers feature a very small power consumption, but the maximum frequency of operation is limited to a few GHz. Injection locked oscillators consume generally less power than CML- or Miller-dividers due to the tuned nature of the circuit. One disadvantage of injection locked oscillators is the limited input bandwidth (or input locking range), which fortunately is not very relevant in LC-VCO based PLL's, as LC-VCO's anyway feature a limited tuning range. The main disadvantage of today's widely used CMOS differential injection locked oscillator topology is found in the large input capacitance and in its small input locking range. A CMOS low power direct injection locking scheme [14] for LC-oscillators is presented in Fig. 5 to divide highest frequency signals with lowest input capacitance.



(a) Direct injection locked divider simplified schematic.

(b) 15 GHz divider.

(c) 40 GHz divider.

Figure 5: Direct injection locked divider simplified schematic diagram. 15 GHz and 40 GHz injection locked divider chip photograph [14].

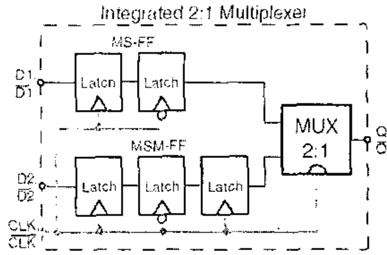
The proposed topology consists of MOS-switches directly coupled to the tank. The concept is verified with two fully integrated injection locked oscillators aiming at different frequencies. The measured frequency locking characteristics and phase noise clearly verifies the circuit implementation. A CMOS low power injection locked oscillator performs highest frequency division by two consuming only 3 mW from 1.5 V supply voltage. The measured circuit divides 41 GHz by two with a locking range of 1.5 GHz. A second oscillator aiming at 15 GHz features a total locking range of 14.2-17 GHz at a power consumption of 23 mW. The increased locking-range of this divider results in increased power consumption [14]. The measurement results are summarized in Tab. 3.

Table 3: Injection locked divider performance [14].

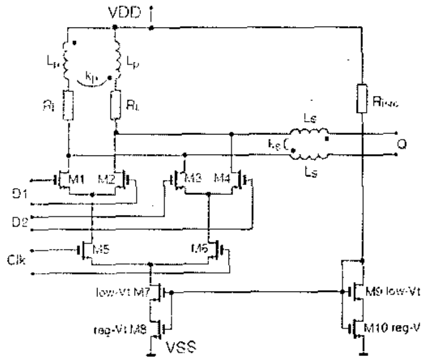
Technology	0.13 μm CMOS	
Supply voltage	1.5 V	
Power Consumption	3 mW	23 mW
Locking Range	40.5 - 42 GHz	14.2 - 17 GHz

4 A 50 Gb/s 2:1 Multiplexer in 0.13 μm CMOS

Data multiplexers (MUX) are key blocks in high-speed data communication systems. Current 2:1 MUX already achieve operating speeds of 50 Gb/s in 90 nm CMOS [10]. A fully integrated 2:1 multiplexer IC which also operates



(a) 2:1 MUX block diagram.



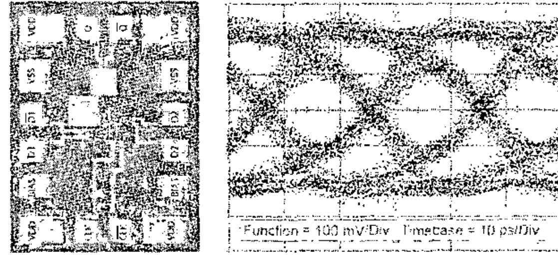
(b) 2:1 MUX core schematic diagram.

Figure 6: 50 Gb/s 2:1 MUX in 0.13 μm CMOS: block diagram and MUX core schematic diagram [15].

at 50 Gb/s data rate has been realized in standard 0.13 μm bulk-CMOS technology [15].

Fig. 6 shows the block diagram and the schematic diagram of the core multiplexer circuit. The 2:1 MUX IC consists of a master-slave flip-flop (MS-FF), a master-slave-master flip-flop (MSM-FF) and a multiplexer stage (MUX 2:1). The MUX stage uses series gating between clock and data input. All transistors in the MUX stage data path are of the same size and are 3/5 the width of the clock transistors. The MUX stage uses 70 Ω poly-silicon load resistors which is a compromise between high voltage swing and reasonable output matching. The tail current is set to 7 mA. To enhance the operating bandwidth of the multiplexer, inductive shunt peaking and series peaking is used. The output network acts as a filter which consists of various parasitic capacitances, load resistors, bond inductances and on-chip inductors L_p and L_s. The inductor L_s is in series to the output and needs therefore a high Q-factor while the Q-factor of the inductor L_p is determined by the load resistors R_L. To reduce capacitance to substrate only the top metal is used. The spacing between the turns is kept wide to reduce turn-to-turn parasitic capacitance.

For measurement the 2:1 MUX IC is bonded on a Rogers RO4003 microwave substrate. The multiplexer is tested with two pseudo-random bit sequences (PRBS of 2^7-1). The input voltage swing is 2 x 500 mV_{pp}. The sinusoidal



(a) Chip photograph. (b) 50 Gb/s measured eye diagram.

Figure 7: 50 Gb/s 2:1 MUX in 0.13 μm CMOS: chip photograph and measured eye diagram [15].

clock signal has a voltage swing of 2 x 400 mV_{pp}. Fig. 7 shows the measured eye diagram of the differential output signal at a data rate of 50 Gb/s. Tab. 4 shows the performance summary of the MUX.

Table 4: 50 Gb/s 2:1 MUX measurement results [15].

Power supply	1.5 V
Total power consumption	98 mW
Maximum data rate	50 Gb/s
Output voltage swing (50 Ω)	2×100 mV_{pp}
Testchip die area	0.63 mm by 0.47 mm
Technology	0.13 μm CMOS

5 A 100 Gbit/s amplifier in SiGe bipolar technology

A broadband amplifier with 16 dB gain and a 3-dB bandwidth of 62 GHz has been realized in a 200 GHz f_T, 275 GHz f_{max} SiGe bipolar technology [16, 17]. Broadband amplifiers are very important building blocks for a large variety of applications, including wireless transceivers, mm-wave applications and optical communication systems. In general, they are based on a lumped [18, 19, 20] or on a distributed concept [21, 22, 18].

The circuit diagram of the broadband amplifier based on

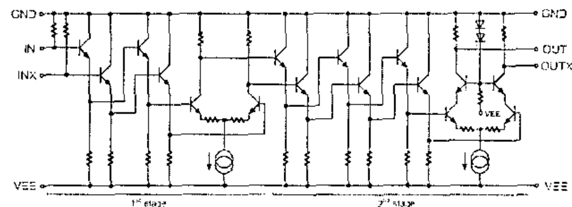
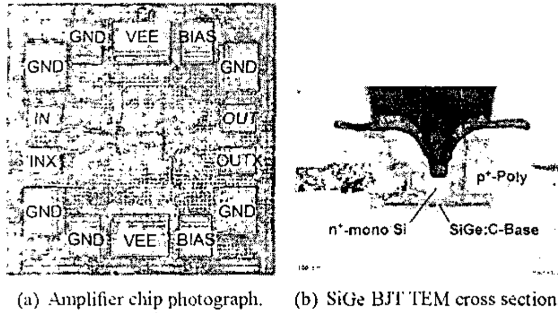


Figure 8: 62 GHz, 16 dB gain broadband amplifier schematic diagram [16].

lumped elements realized in this work is shown in Fig. 8. The amplifier is based on a fully differential design and consists of two stages. 50 Ω on-chip resistors are provided at the input and the output for broadband matching. In addition, emitter degeneration and low load resistors are used for increasing the 3-dB bandwidth at a well-defined gain. Carefully adjusted transistor sizes and currents enable a flat transfer function and a high bandwidth. The differential amplifier of the second stage is implemented as cascode configuration in order to prohibit avalanche breakdown of the output transistors. The cascode stage additionally minimizes the Miller effect, thereby bandwidth is increased.



(a) Amplifier chip photograph. (b) SiGe BJT TEM cross section.

Figure 9: Chip photograph of the 62 GHz, 16 dB gain broadband amplifier in SiGe (chip size: 550 μm × 550 μm) [16] and TEM cross section of the emitter-base complex of a SiGe transistor with effective emitter width of 0.14 μm [17].

The chip photograph of the amplifier is shown in Fig. 9(a). The amplifier is fabricated in a preproduction SiGe bipolar technology [17]. The transistors have a double-polysilicon self-aligned emitter-base configuration with a minimum effective emitter width of 0.14 μm. A TEM cross section of the emitter-base complex is given in Fig. 9(b). The SiGe:C base of the transistors has been integrated by selective epitaxial growth. The emitter contact exhibits a monocrystalline structure. The transistors manufactured in this technology offer a transit frequency f_T of 200 GHz, a maximum oscillation frequency f_{max} of 275 GHz and a ring oscillator gate delay of 3.5 ps. Current density for maximum f_T and f_{max} is at about 8 mA/μm^2. The collector-emitter breakdown voltage BV_{CE0} is 1.7 V. The technology provides four copper metallization layers, two different types of polysilicon resistors, a TaN thin film resistor and a MIM capacitor.

The single-ended low-frequency gain is 10 dB and the 3-dB bandwidth is 62 GHz. The differential gain is 16 dB. The current consumption is 155 mA at a supply voltage of -5 V. Degradation of S_{22} at about 50 GHz can be observed. In the case of a single-ended excitation together with an inductance in the supply path this behavior can be verified by simulations. In differential operation such an inductance will have no effect.

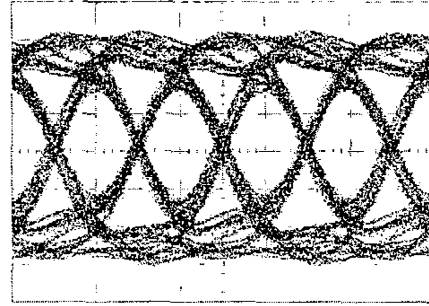


Figure 10: 100 Gb/s (250 mV/div, 5 ps/div) [16].

Table 5: Broadband amplifier measurement results [16].

SiGe bipolar technology, min. eff. emitter width, ring osc. gate delay	200/275 GHz f_T/f_{max} 0.14 μm 3.5 ps
Bandwidth (3 dB)	62 GHz
Differential gain	16 dB
CP_{1dB} (input)	-9.5 dBm
IIP3	+2.1 dBm
Supply voltage	-5.0 V
Supply current	155 mA
Chip size	550 μm × 550 μm

In Fig. 10 the measured output eye diagram for a 100 Gbit/s excitation signal is shown. A high-performance PRBS-generator chip [6] and the broadband amplifier chip have been mounted closely on a substrate. Short bond wires connect the outputs of the PRBS-generator and the amplifier inputs. The clear output eye diagram at a data rate of 100 Gbit/s demonstrates the feasibility for high-speed communications. Tab. 5 shows the performance summary.

6 A 65 GHz - 95 GHz double-balanced mixer for automotive radar front-ends in SiGe bipolar technology

An active mixer for down-conversion with a conversion gain of more than 24 dB and single-sideband (SSB) noise figure of less than 14 dB in the frequency range from 76 GHz to 81 GHz has been realized [23]. The gain is >22 dB from 65 GHz up to 95 GHz with slightly decreased noise performance.

A simplified circuit diagram of the mixer is shown in Fig. 11. The mixer consists of a mixer core, an LO buffer, a balun at the RF input and an IF buffer. The mixer core is based on the Gilbert-mixer. The mixer has a double-balanced structure and utilizes differential LO and RF sig-

nals. Transistor sizes and bias currents are optimized in order to obtain a good compromise between gain, linearity and low noise figure. The size of the switching transistors is designed at the current density for maximum f_T, whereas the RF transistors are designed for minimum noise contribution. The differential signals required for LO and RF inputs of the mixer core are generated by the LO buffer and a LC balun, respectively. The LO buffer consists of a differential amplifier which provides a differential output signal from the single-ended input.

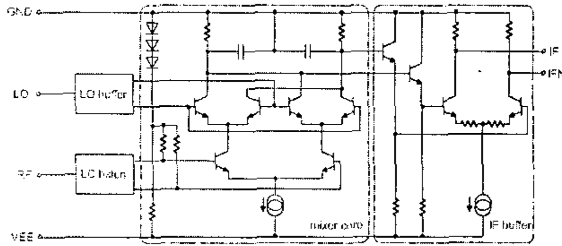
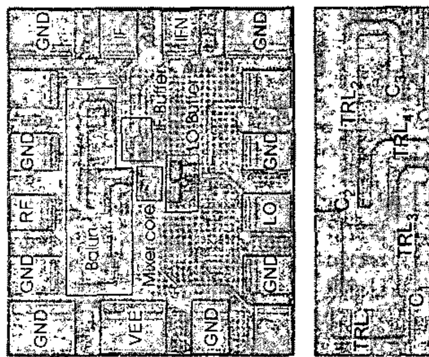
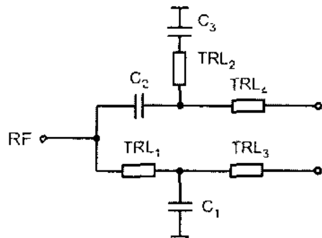


Figure 11: Simplified circuit diagram of the mixer (GND = 0 V, VEE = -5 V) [23].



(a) Mixer chip photograph.

(b) Detailed view of the LC balun.



(c) Schematic diagram of the LC balun.

Figure 12: Chip photograph of the mixer (chip size: 550 μm × 450 μm), detailed view of the LC balun and schematic diagram of the LC balun [23].

Fig. 12(a) shows the chip photograph of the mixer. Building blocks and important pads are indicated in the photograph. The LC balun (Fig. 12(b)) is placed directly at the RF input, followed by the mixer core. The LC balun consisting of the transmission lines TRL_1 and TRL_2 and the MIM-capacitors C_1 and C_2 (Fig. 12(c)). This balun converts the unbalanced RF signal to a balanced signal and provides an impedance transformation for 50 Ω matching at the RF input. Capacitor C_3 is required to achieve an RF ground at TRL_2. The LC balun was designed based on the calculation of a lumped element balun [24]. Then the inductances were substituted with transmission line TRL_1 and TRL_2 [25]. Further optimization was done using an EM-field simulator.

The mixer is fabricated in a SiGe bipolar technology which is based on the process technology presented in [26]. The transistors have a double-polysilicon self-aligned emitter-base configuration with an effective emitter width of 0.18 μm. The SiGe:C base of the transistors has been integrated by selective epitaxial growth and the transistors exhibit a monocrystalline emitter contact. The transistors manufactured in this technology offer a transit frequency f_T and a maximum oscillation frequency f_{max} of more than 200 GHz and a ring-oscillator gate delay of 3.7 ps. The technology provides four copper metallization layers, two different types of polysilicon resistors and a TaN thin film resistor.

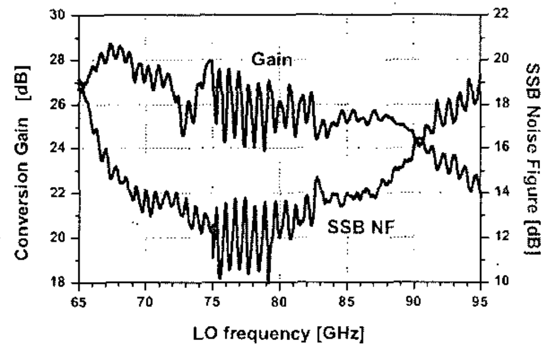


Figure 13: Measured conversion gain and SSB noise figure versus LO frequency. IF frequency is 500 MHz, LO power is 2 dBm [23].

In Fig. 13 the measured conversion gain and SSB noise figure versus LO frequency of the mixer at a constant IF frequency of 500 MHz are shown. The LO input power is set to 2 dBm at the center frequency. The measured conversion gain is higher than 24 dB and the SSB noise figure is lower than 14 dB at the frequency range from 72.3 GHz to 82.5 GHz. The mismatch of the mixer RF input and the noise source output result in a ripple seen in the measurement plot. The V-band noise source (frequencies below 75 GHz) exhibits a better match than the W-band noise source (frequencies above 75 GHz). Tab. 6 shows the performance summary of the mixer.

Table 6: Mixer performance summary [23].

SiGe bipolar technology, min. eff. emitter width, ring osc. gate delay	>200 GHz f_T, f_{max} 0.18 μm 3.7 ps
Conversion gain	>24 dB (65.0 - 90.8 GHz) >22 dB (65.0 - 94.9 GHz)
SSB noise figure	<14 dB (72.3 - 82.5 GHz) <16 dB (66.5 - 90.0 GHz)
CP_{1dB} (input)	-30 dBm
Supply voltage	-5 V
Supply current	60 mA
Chip size	550 μm × 450 μm

7 Summary

Silicon-based RF ICs have been realized to demonstrate wireline, wireless and sensor applications up to 100 GHz. Finding the right match between circuit techniques and process technology is a major issue to push the circuit performance to the limits. Further advances in process technologies and circuit design will result in continuing the upward shift of the frequency limits in silicon.

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