An 84 GHz Bandwidth and 20 dB Gain Broadband Amplifier in SiGe Bipolar Technology

Saverio Trotta, *Student Member, IEEE*, Herbert Knapp, *Member, IEEE*, Klaus Aufinger, Thomas F. Meister, Josef Böck, Bernhard Dehlink, *Student Member, IEEE*, Werner Simbürger, and Arpad L. Scholtz

***Abstract*—This paper reports on the design, fabrication, and characterization of a lumped broadband amplifier in SiGe bipolar technology. The measured differential gain is 20 dB with a 3-dB bandwidth of more than 84 GHz, which is the highest bandwidth reported so far for broadband SiGe bipolar amplifiers. The resulting gain bandwidth product (GBW) is more than 840 GHz. The amplifier consumes a power of 990 mW at a supply of −5.5 V.**

***Index Terms*—Broadband amplifier, SiGe.**

I. Introduction

BROADBAND amplifiers are widely used in high-speed communication systems. Different techniques are used to design wideband amplifiers. In distributed amplifiers, the input and output capacitances of the transistors are incorporated in transmission lines, thus eliminating their low-pass characteristic and increasing the bandwidth. With the advent of monolithic inductors, inductive peaking techniques have become feasible in integrated circuits: the capacitance that limits the bandwidth resonates with an inductor, thereby improving the bandwidth [1], [2]. Recently a distributed amplifier with a bandwidth of 81 GHz [3], an 80 GHz output driver with inductive peaking [4], and a lumped broadband amplifier with a bandwidth of 62 GHz [5] in SiGe Bipolar and BiCMOS technology have been reported. This paper discusses design considerations for inductorless broadband amplifiers based on the properties of the transistor in common collector configuration. The theory has been validated by a four-stage amplifier which shows a measured 3-dB bandwidth of 84 GHz and a differential gain of 20 dB.

II. Circuit Design

The amplifier is fully differential. It is based on a cascode topology. The cascode is a multiple-device configuration that is useful in high-frequency circuit design. It shows little high-frequency feedback through the base-collector capacitance (negligible Miller effect) with a very large 3-dB bandwidth. A broadening of the bandwidth of the cascode can be achieved by driving this stage with cascaded emitter-followers (EFs) [5]. The EFs shift down the level of the signal to drive the lower differential pair in the cascode with the proper DC-level. It can be shown that the voltage gain of the capacitive loaded EF, sketched in Fig. 1, has a frequency dependence that is analogous to the frequency dependence of the transfer function of an *RLC* series resonant circuit [6]

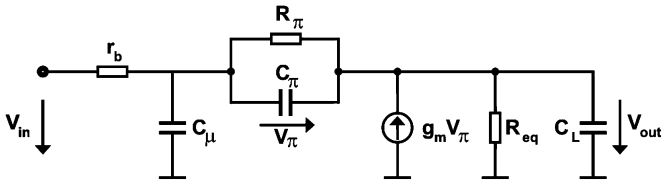

Fig. 1. Small-signal model of a capacitive loaded emitter-follower.

$$A(j\omega) \approx \left\{1+j\omega\left[r_bC_\mu+\left(\frac{1}{g_m}+\frac{r_b}{\beta}\right)C_L+\frac{r_bC_L}{\omega_T R_{\rm eq}}\right]-\omega^2\frac{r_bC_L}{\omega_T}\right\}^{-1} \quad (1)$$

with a resonant frequency

$$\omega_r=\sqrt{\frac{\omega_T}{r_bC_L}} \quad (2)$$

and a damping factor

$$\delta=\left(\frac{C_\mu}{2C_L}+\frac{1}{2r_bg_m}+\frac{1}{2\beta}\right)\omega_T+\frac{1}{2R_{\rm eq}C_L}. \quad (3)$$

Here, ω_T is the cutoff frequency of the transistor, $R_{\rm eq}$ denotes the parallel connection of the output resistance of the transistor and the load resistance, and C_L is the capacitive load at the output. The voltage transfer function (1) of an EF therefore depends on the transistor parameters, the current, and the load. Simulated examples for different current values and different capacitive loads are plotted in Fig. 2. The simulation results show that the voltage peak in the transfer function is shifted to high frequencies by reducing C_L. Since the transconductance g_m is proportional to the current, the peak can be damped by lowering the current. Since the capacitive loaded EF in Fig. 1 behaves like a second order system, high quiescent current and large capacitive load conditions should be avoided in order to keep the damping factor large enough to prevent oscillations and instability.

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S. Trotta was with Infineon Technologies. He is now with the Freescale Semiconductor GmbH, D-81829 Munich, Germany. He is also with the Vienna University of Technology, A-1040 Vienna, Austria (e-mail: Saverio.Trotta@freescale.com).

H. Knapp, K. Aufinger, T. F. Meister, J. Böck, and W. Simbürger are with Infineon Technologies AG, D-81726 Munich, Germany.

B. Dehlink is with Infineon Technologies AG, D-81726 Munich, Germany. He is also with the Vienna University of Technology, A-1040 Vienna, Austria.

A. L. Scholtz is with the Vienna University of Technology, A-1040 Vienna, Austria.

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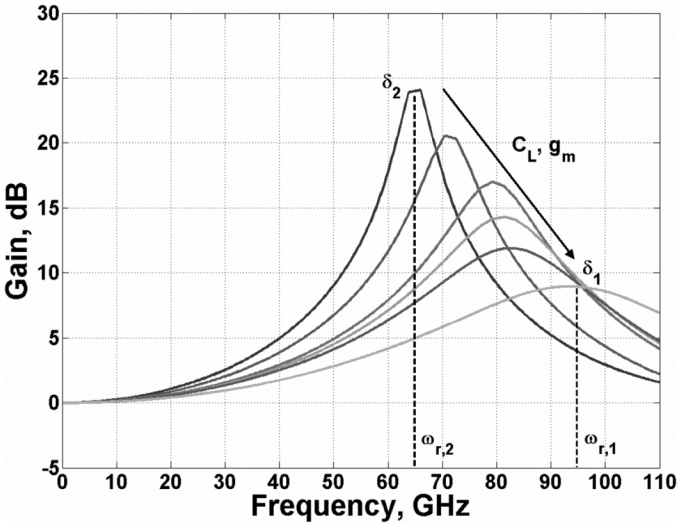

Fig. 2. Simulated capacitive loaded emitter-follower voltage gain for different load and g_m (current) values.

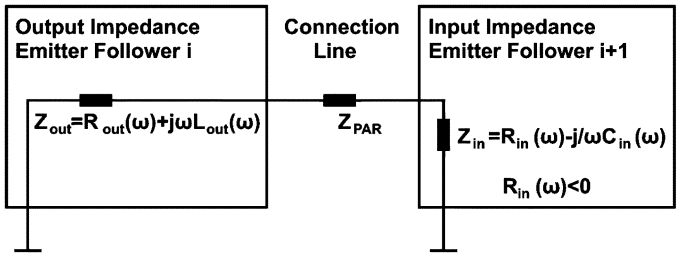

Fig. 3. Model of an emitter-follower driving another emitter-follower.

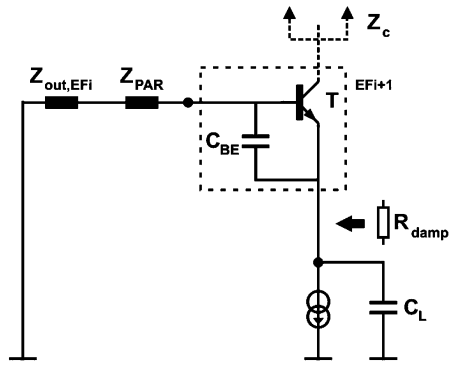

Fig. 4. Possible unstable configuration for the emitter-follower due to the parasitics $Z_{\rm PAR}$, C_L, $Z_{{\rm out},{\rm EF}i}$, and the base-emitter capacitance of T. A damping resistor can be added in order to overcome this problem.

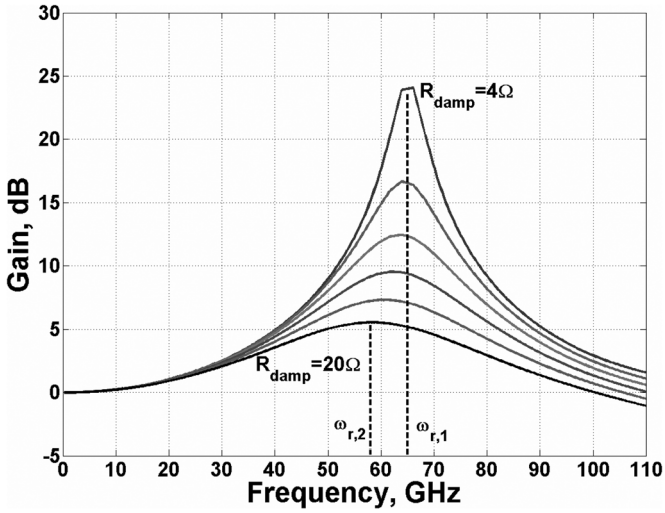

Fig. 5. Simulation results of the effect of a damping resistor on the voltage gain of an emitter-follower.

The gain-peak shown by the EFs in Fig. 2 at high frequencies combined with the frequency response of the cascode can result in an overall wider bandwidth. The main problem in using EFs to drive the cascode stage is potential instability, especially when more than one emitter-follower pairs are cascaded. By using the small-signal model, it can be shown that the output impedance of the EF is inductive if $1/g_m > r_b$. Special attention needs to be paid to the input impedance: it can be found that, besides having negative reactance, the real part can also become negative at high frequencies [7]. These properties of the EF can cause sustained oscillations or ringing during switching transients [8]. In cascaded EFs, oscillations can be triggered by the inductive output impedance of the driving EF (possibly supported by an inductive behavior of the connection line) and the capacitive input impedance (combined with a negative real part) of the loading EF, see Fig. 3. In this case, the parasitic inductance unfortunely helps to move the complex and conjugate poles of the voltage transfer function to the imaginary axis, bringing the EF into unstable region. The inductive output impedance of an EF in series with the input reactance of the next EF and the inductance of the connection line can form an *LC*-tank, as shown in Fig. 4. In this configuration, oscillations and instability result at frequencies where $R_{\rm in}(\omega) + R_{\rm out} < 0$ [9]. To prevent this, small resistors can be added in series with the emitter or the base of the transistor, transforming its input impedance and causing energy loss, thereby damping oscillations [10]. The main drawback of this solution is that the resistors shift the gain peak to lower frequencies. A simulated example is presented in Fig. 5.

In this paper, we propose a design methodology to avoid the instability. The frequency at which the real part of the input impedance of a common collector, modeled in Fig. 1 (or a common emitter), starts to become negative can be expressed in a first approximation, neglecting C_μ, by

$$\omega_0 = \sqrt{\frac{\omega_T}{\beta_0 \left(R_{\rm eq} C_L - 1/\omega_T\right)}} \tag{4}$$

where β_0 is the low-frequency current gain of the transistor, and $R_{\rm eq}$ depends on the resistive load R_L at the output of the EF, as said above [6], [7]. The result in (4) shows that the time constant $\tau_L = R_{\rm eq} C_L$ must be small in order to shift ω_0 to high frequencies. The dependence of the input impedance on the output load is presented in Fig. 6(a) and (b). The simulations have been performed with different load time constants $\tau_1 > \tau_2 > \tau_3$.

The simulation results below show that it is possible to move ω_0 to very high frequencies [Fig. 6(a)] by reducing the load seen by the common collector at its output. Also the reactance will be

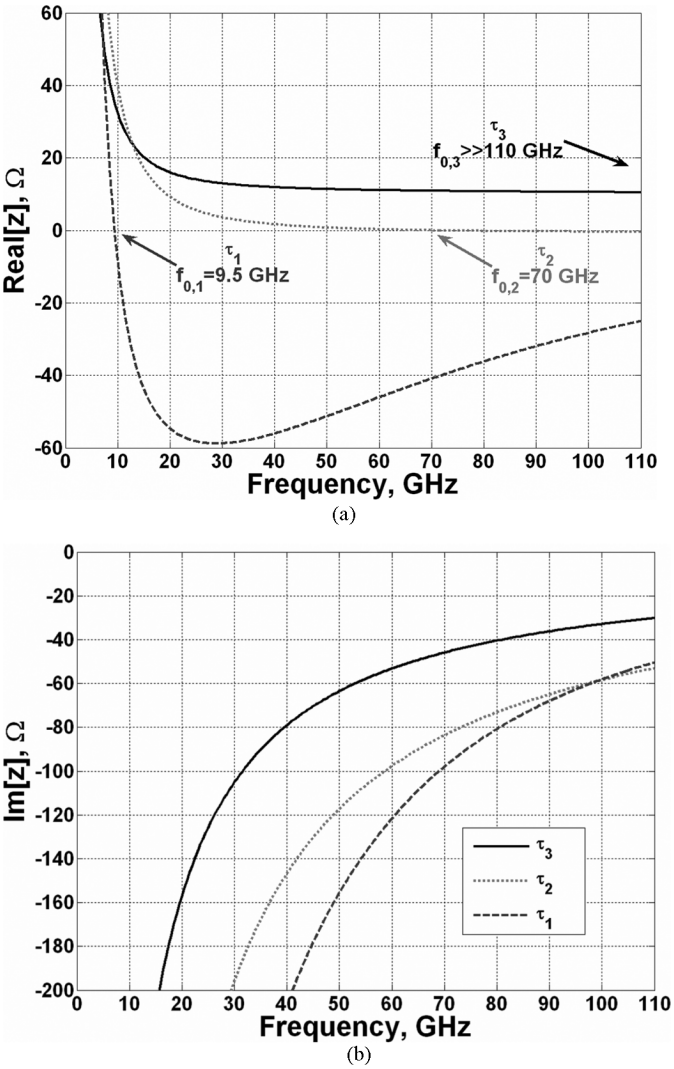

Fig. 6. (a) Simulated dependence of the real part of the input impedance of an EF on the time constant τ of the load. (b) Simulated dependence of the imaginary part of the input impedance of an EF on the time constant τ of the load.

less negative which means less energy in the *LC*-tank [Fig. 6(b)]. Suggested by the theory and the simulation results presented before, a cascade of four EFs has been designed by using the rule

$$A_i^{\mathrm{EF}} > A_{i+1}^{\mathrm{EF}} \tag{5}$$

where A_i^{EF} indicates the size of the transistor and the index i refers to the stage number in the cascade. An amplifier stage is shown in Fig. 7. The parasitics $Z_{\mathrm{PAR},i}$ of the interconnection lines as well as the parasitic capacitance of the input and output pads have been considered during the design. Starting from the input, the emitter length of each subsequent EF transistor in the cascade is reduced. The current density is the same for each transistor and set to achieve the maximum ω_T. The voltage gain of each EF is shown in Fig. 8. According to (2), the first EF shows a gain-peak at very high frequencies. The gain-peak is damped and shifted to lower frequencies throughout the cascade. The reason for this is the dependence of the resonant frequency ω_r (2) and the damping factor δ (3) on C_L and r_b. The first transistor is the largest and sees a certain load at its output. The second transistor sees a smaller load at its output, but since the size is smaller than the first one, its base resistance will have a larger impact on the gain-peak. The same evaluation can be made for the third EF. The last one is very small and will show the largest base resistance. Moreover, it drives the transistor in the lower differential pair of the cascode. The transistors used in the cascode are quite large compared to the ones used as EFs. This explains the voltage gain behavior for the fourth EF shown in Fig. 8. The overall voltage gain of a cascade of these four EFs is presented in Fig. 9. The circuit simulated is the amplifier stage proposed in Fig. 7. The parasitics of the interconnection lines (Z_{PAR}) have been modeled during the simulations by means of *LC* networks. The bias network used for the first two emitter-follower pairs helps to improve the bandwidth. It has not been used for all the EF pairs because the feedback provided by this network through four EFs can cause strong ringing or oscillations during switching transients. From the simulation results, it can be seen that the combination of a cascode with the driving stage described above can result in a broadband amplifier with very flat frequency response. Moreover, the bandwidth of the cascode stage has been further broadened by means of resistive emitter degeneration (R_{deg} in Fig. 7) and a dynamic bias for the common base stage. The two bases are cross-connected to the collectors of the last emitter-follower pair. In each half period, the voltage across the base-collector junction of the conducting transistor in the differential pair is increased, reducing the Miller effect. Therefore, the bandwidth is increased. As shown in Fig. 9, the voltage gain for the complete amplifier is less than 6 dB. In order to increase it, four amplifier stages have been cascaded. The load resistor of the last stage is 75 Ω. The signal is applied to the output pads via 50 Ω transmission lines, implemented as microstrip lines. By using four EFs there was not enough headroom to use a current source for the cascode. For this reason, resistors have been used as current sources. The voltage reference, V_{ref} in Fig. 7, is generated on chip and can be adjusted externally.

III. Technology

The broadband amplifier is manufactured in an advanced SiGe:C bipolar process based on the technology presented in [11]. The process uses shallow and deep trench isolation. The transistors have a double-polysilicon self-aligned emitter base configuration with a SiGe:C base which is integrated by selective epitaxial growth. The transistors are fabricated using 0.35 μm lithography. The minimum effective emitter width is 0.18 μm. In comparison to [11], the transistors used for the fabrication of this circuit have a pedestal collector with lower dopant density resulting in a cutoff frequency f_T of 180 GHz, a maximum oscillation frequency f_{MAX} of 250 GHz, a reduced base collector capacitance, and an increased collector base breakdown voltage. The maximum f_T is obtained at a current density of 5 mA/μm^2. The chip photograph is presented in Fig. 10. The size of the IC is 700×900 μm^2, but the active area occupies only 210×260 μm^2. The interconnection lines between the EFs have been designed as short as possible in order to reduce the influence of the their parasitics on the behavior of the amplifier.

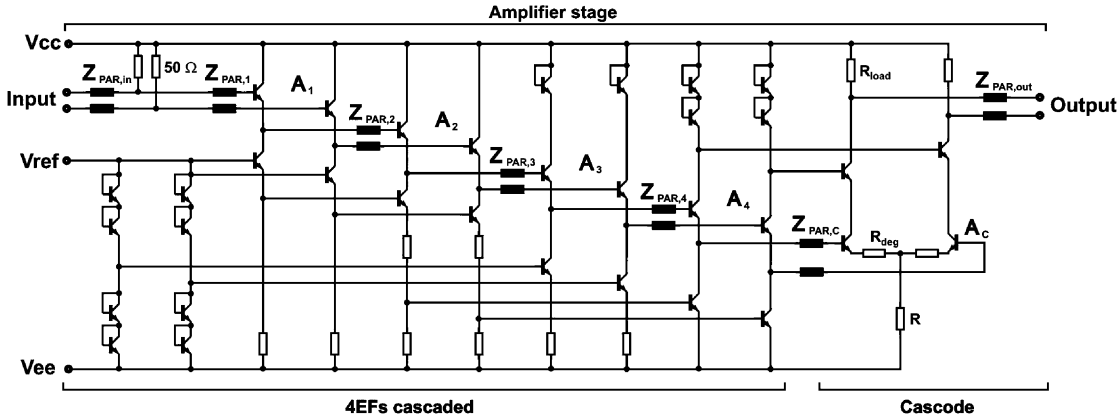

Fig. 7. Amplifier stage. The 50 Ω input impedance is used only in the first stage. $A_1 = 6.1 \times 0.18\ \mu\text{m}^2$, $A_2 = 5.2 \times 0.18\ \mu\text{m}^2$, $A_3 = 4 \times 0.18\ \mu\text{m}^2$, $A_4 = 3.1 \times 0.18\ \mu\text{m}^2$, and $A_C = 14.2 \times 0.18\ \mu\text{m}^2$. $Z_{\text{PAR},i}$ model the parasitics of the interconnection lines.

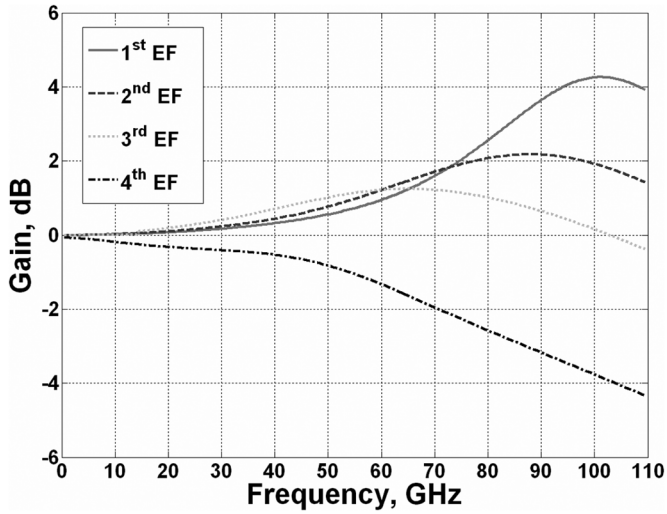

Fig. 8. Simulated voltage gain versus frequency for each emitter-follower.

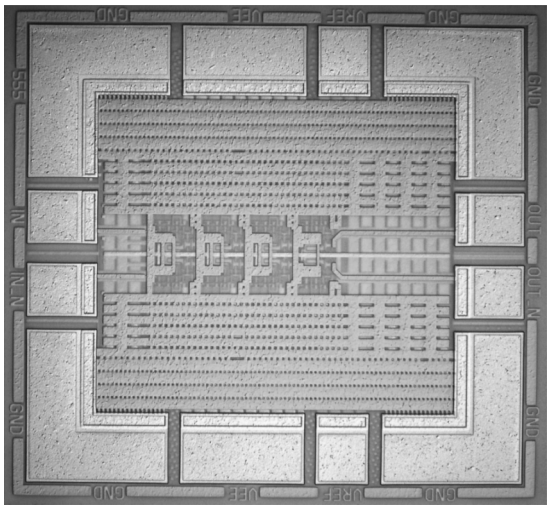

Fig. 10. Chip photograph of the four-stage broadband amplifier.

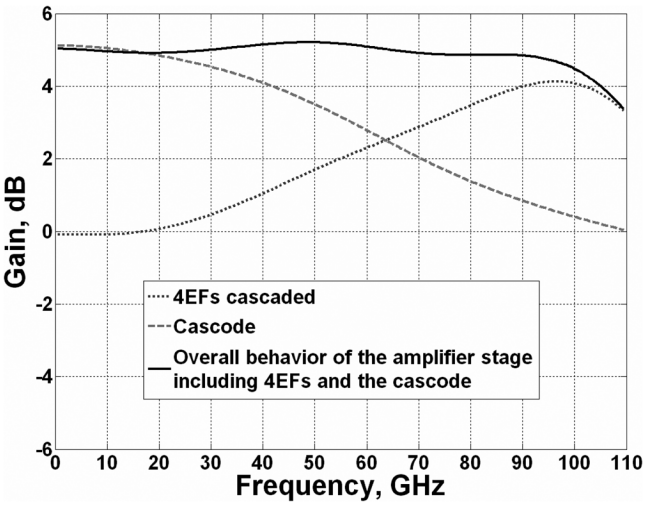

Fig. 9. Simulated voltage gain versus frequency: the cascade of four EFs, the cascode, and the amplifier stage.

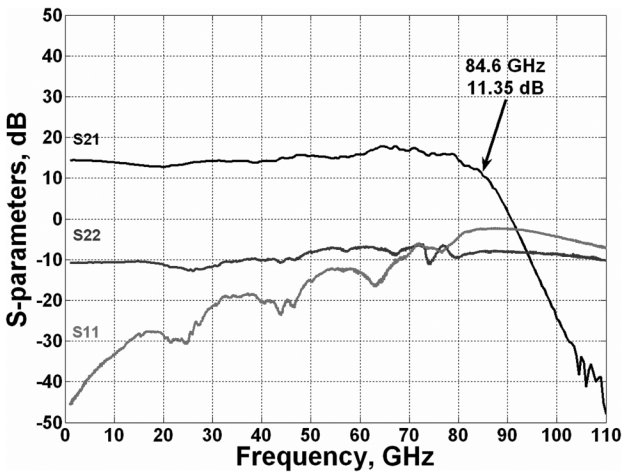

Fig. 11. Single-ended measurement of the S-parameters (differential gain is 6 dB higher).

IV. Experimental Results

The fabricated circuit has been carefully characterized by S-parameter measurements and by applying high data rate signals to the chip. All measurements were performed at a supply voltage of −5.5 V while the current consumption was 180 mA.

S-parameter measurements were performed single-ended using an Agilent vector network analyzer. The chip was mounted on a substrate to provide the supply voltage. The substrate was put on a probe station where the input and output pads were contacted by probes. Fig. 11 shows the single-ended

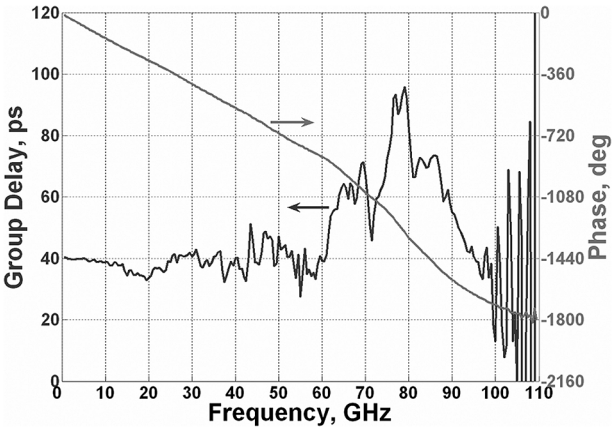

Fig. 12. Phase and group delay variation of S21 versus frequency.

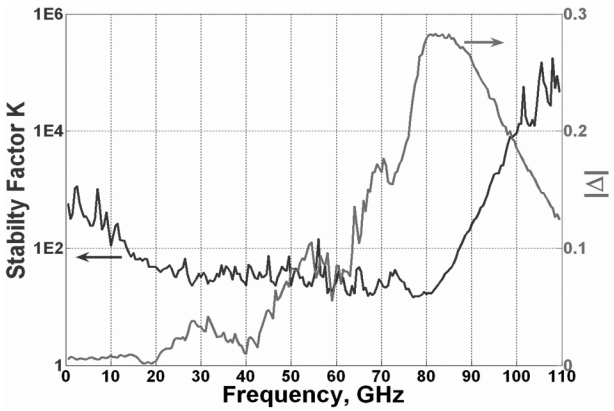

Fig. 13. Stability factor K and $|\Delta|$ versus frequency.

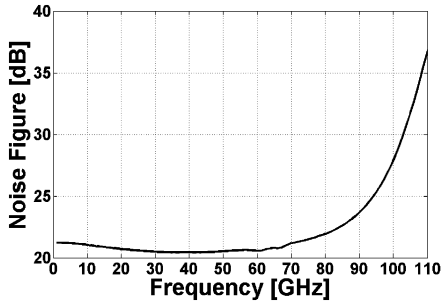

Fig. 14. Simulated noise figure versus the frequency.

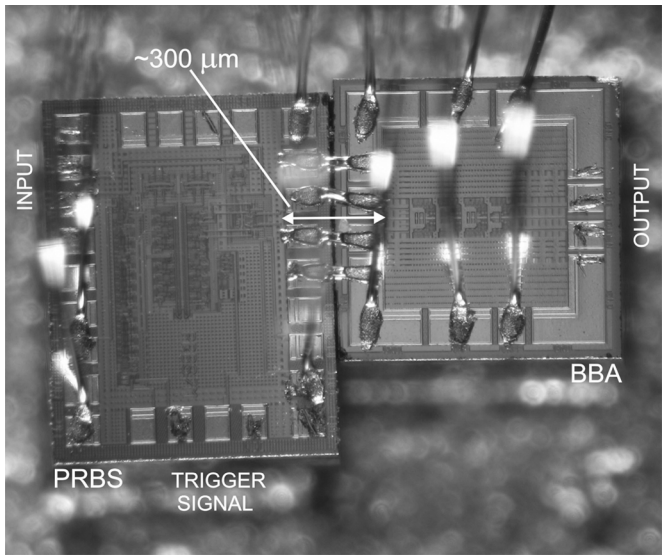

Fig. 15. Large signal test setup.

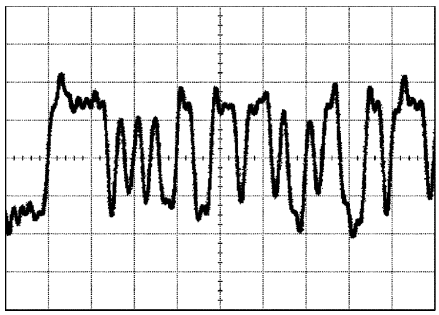

Fig. 16. On-wafer measured differential 100 Gb/s output signal of the 2^7-1 PRBS generator. x-axis: 50 ps/div; y-axis: 100 mV/div.

measured gain, and the input and the output return loss at a 50 Ω source and load impedance. The single-ended low-frequency gain is 14 dB. The average differential gain is 20 dB with a gain ripple of ±2 dB. The 3-dB bandwidth is 84.6 GHz. The degradation of the input matching at high frequency is mainly due to the input impedance $Z_{\rm in}$ of the first EF. The shunt combination of the 50 Ω on-chip input impedance, the parasitic capacitance of the input pad, the parasitic inductance of the interconnection line between the pad and the input of the first EF, and $Z_{\rm in}$ forms a low-pass filter. This effect could be reduced by using an inductor in series with the 50 Ω impedance, but, as already discussed above, this can trigger instability effects. The effect of the higher return loss at high frequencies, which results in a reduced voltage swing of high-speed signals, was taken into account. The gain provided by the EFs compensates for the drop, equalizing the signal. The phase of S21 varies linearly with frequency up to 60 GHz, indicating small variations in the group delay, as shown in Fig. 12. Simulations indicate that the degradation of the group delay at 80 GHz is partly due to the heating of the mounted chip and partly due to the steep roll-off of the gain. The stability of the amplifier was evaluated by means of the stability factor K and $|\Delta|$ (see Fig. 13). Finally, since the noise performance of the amplifier influences the additive random jitter in the output signal, the simulated noise figure (NF) for the four-stage amplifier is shown in Fig. 14. As expected, the noise figure is quite flat over the 3-dB bandwidth and starts to rise when the gain of the broadband amplifier drops (see also Fig. 11).

In order to test the broadband amplifier with large amplitude and high data rate signals, a pseudo-random bit sequence (PRBS) generator chip [13] was mounted close to the amplifier on a substrate, as shown in Fig. 15. Short bond wires connected the outputs of the PRBS generator and the amplifier inputs. A single-ended clock signal was applied to the PRBS source via a 40 GHz probe. The differential output signal has been measured via a 67 GHz GSSG probe with a 70 GHz sampling oscilloscope, 86100A from Agilent. The precision timebase module, which allows the sampling oscilloscope to provide results with

TABLE I
OVERVIEW OF BROADBAND AMPLIFIERS IN DIFFERENT TECHNOLOGY REPORTED IN LITERATURE

Ref.	*Technology*	*Dimension*	f_T/f_{MAX}	*BW*	*Gain*	*GBP*	*Power Consumption*	*Topology*
		[µm]	**[GHz]**	**[GHz]**	**[dB]**	**[GHz]**	**[mW]**	
[3]	SiGe HBT	0.13	200/200	81	13	362	495	distributed amplifier
[5]	SiGe HBT	0.18	200/275	60	16	379	770	differential buffered cascode
[14]	InP D-HBT	0.5	337/345	>110	17	>750	222	distributed amplifier
[15]	InP HEMT	0.13	160/270	94 110	14.5 7.5	500 >260	NA NA	distributed amplifier distributed amplifier
[16]	InP HEMT	0.1	160/300	180	5	320	NA	distributed amplifier
[17]	CMOS	0.18	50	39.4	20	394	250	distributed amplifier
[18]	SOI CMOS	0.12	196/230	90	11	320	210	distributed amplifier
[19]	CMOS	0.09	NA	80	7.4	190	120	distributed amplifier
This work	SiGe HBT	0.18	200/275	>84	20	>840	990	differential buffered cascode

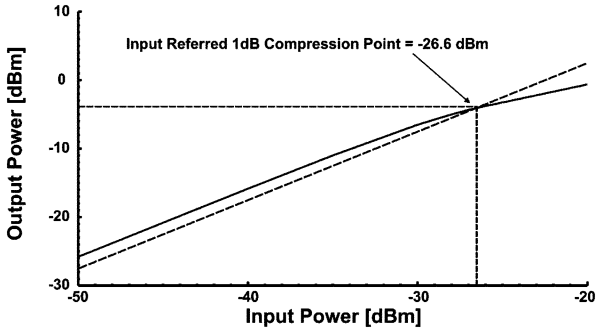

Fig. 17. Simulated input-referred 1 dB compression point.

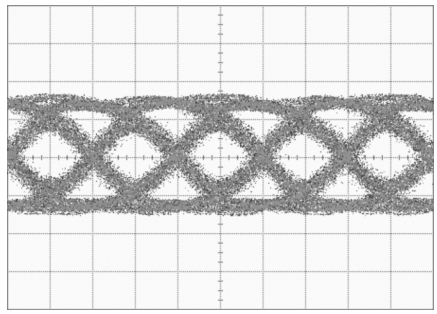

Fig. 18. Measured differential 80 Gb/s eye diagram. x-axis: 6.3 ps/div, y-axis: 500 mV/div. The precision timebase is off.

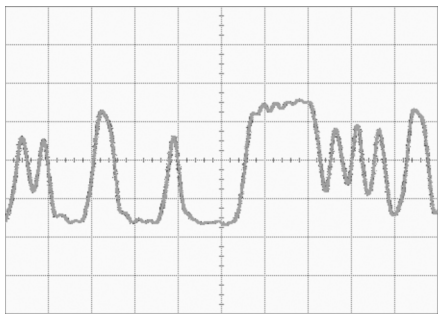

Fig. 19. Measured differential 80 Gb/s bit pattern. x-axis: 50 ps/div, y-axis: 500 mV/div.

improved timebase jitter and resolution by more than a factor of five [12], could not be used to trigger the oscilloscope. The on-wafer measured output signal from the PRBS at 100 Gb/s is reported in Fig. 16 [13]. The amplitude of the this signal is about 300 mV_{pp}. According to the simulation result presented in Fig. 17, the input-referred 1 dB compression point of the amplifier at 60 GHz is -26.6 dBm. This means that the amplifier in this case is working in limiting mode. The differential eye diagram and the bit pattern of the output signal of the broadband amplifier at 80 Gb/s are plotted in Figs. 18 and 19, respectively. The broadband amplifier is still capable of generating an output signal which shows a very good eye diagram even if the high-speed signal provided by the PRBS is slightly degraded due to the bond wires and its self-heating due to the mounting. A simulated example that shows the influence of the bond wires at the input of the amplifier on the bandwidth is reported in Fig. 20. The bond wires have been modeled as inductors of 150 pH. The low-pass behavior of the inductors reduces the bandwidth by 5 GHz. In this first test chip, the amplifier and especially the EFs were not designed to compensate for the drop of the gain at high frequencies due to the bond wires. Moreover, a different length for the two bond wires can result in a different phase shift for

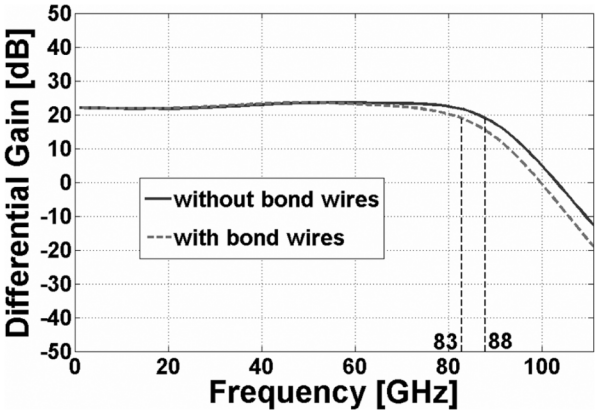

Fig. 20. Simulated influence of the bond wires on the bandwidth of the broadband amplifier.

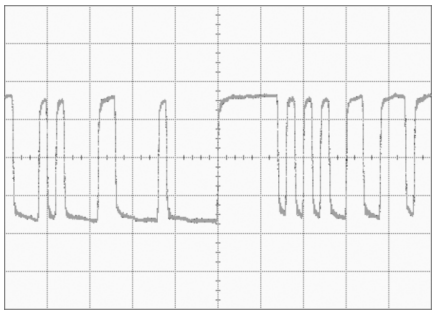

Fig. 21. Measured differential 10 Gb/s bit pattern. x-axis: 500 ps/div, y-axis: 500 mV/div.

the two signals, which can also degrade the quality of the output signal of the amplifier.

In order to prove that the design technique used to develop the amplifier can avoid ringing, we show in Fig. 21 also a measured bit pattern at 10 Gb/s. At both data rates, the step response is damped. The amplitude limit of the differential output signal is 1.5 V_{pp}.

V. Conclusion

In this paper, design considerations for broadband amplifiers have been proposed. A test chip has been developed and fabricated in SiGe bipolar technology. A comparison with state-of-the-art broadband amplifiers is given in Table I. The differential gain is 20 dB. The 3-dB bandwidth of the amplifier is 84 GHz, which is to the authors' knowledge the widest bandwidth for a broadband amplifier in SiGe bipolar technology reported to date. The resulting gain–bandwidth product (GBW) of more than 840 GHz is also, to our knowledge, the highest reported so far for single-chip amplifiers in any silicon-based technologies.

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Saverio Trotta (S'04) was born in S. Giovanni R., Italy, in 1976. He received the Laurea degree in electronic engineering from Politecnico di Bari, Italy, in 2003. He is currently working toward the Ph.D. degree at the Technical University Vienna, Austria.

In 2003, he was with Fraunhofer Institut, Erlangen-Nürnberg, Germany, where he was engaged in the development of high-speed digital ICs. From 2004 to 2007, he was with Infineon AG, Munich, Germany, where he was working in the research field of high-frequency integrated circuit design beyond 100 GHz in SiGe bipolar technology. He is now with Freescale Semiconductor, RF/IF Innovation Center, TSO-EMEA, Munich, Germany, where he is working on the design of integrated circuits for automotive radar applications.

Herbert Knapp (M'99) was born in Salzburg, Austria, in 1964. He received the Dipl. Ing. and Ph.D. degrees in electrical engineering from the Technical University Vienna, Austria, in 1997 and 2000, respectively.

He joined Siemens, Corporate Technology, Munich, Germany, in 1993, where he was engaged in the design of integrated circuits for wireless communications. From 2000 to 2005, he was with Infineon Technologies, Corporate Research. His research interests included the design of high-speed digital and analog circuits in CMOS and SiGe technologies. He is now with Infineon Technologies, AIM (Automotive, Industrial and Multimarket), Munich, Germany, where he is working on the design of integrated circuits for automotive radar applications.

Klaus Aufinger was born in Kirchbichl, Austria, in 1966. He received the diploma and the Ph.D. degrees in physics from the University of Innsbruck, Austria, in 1990 and 2001, respectively.

From 1990 to 1991, he was a Teaching Assistant with the Institute of Theoretical Physics, University of Innsbruck. In 1991, he joined the Corporate Research and Development of Siemens AG, Munich, Germany, where he investigated noise in submicron bipolar transistors. Now he is with Infineon Technologies, the former semiconductor group of Siemens, Munich, working in the field of device physics, technology development and modeling of advanced SiGe technologies for high-speed digital and analog circuits.

Thomas F. Meister received the diploma and the Ph.D. degrees in physics from the University of Aachen, Germany, in 1978 and 1981.

From 1981 to 1985, he was with the Kernforschunganlage Jülich, Germany, working in the field of statistical mechanics of solid/fluid interfaces. In 1985, he joined the Corporate Research and Development of Siemens AG, Munich, Germany. He is now with Infineon Technologies, the former Semiconductor Division of Siemens. At Siemens AG, he was first engaged in the physics of polysilicon emitters and in characterization and modelling of fast bipolar transistors. Since 1994, he has been working on the development of advanced SiGe bipolar devices and technology for high-speed applications like optical communication networks, wireless communications, and automotive radar systems.

Josef Böck was born in Straubing, Germany, in 1968. He received the diploma degree in physics and the Ph.D. degree from University of Regensburg, Germany, in 1994 and 1997, respectively.

He joined the Corporate Research and Development of Siemens, Munich, Germany, in 1993. He is now with Infineon Technologies, the former Semiconductor Division of Siemens. His research interests include the characterization and modeling of high-speed silicon and SiGe bipolar devices and process development for bipolar and BiCMOS SiGe technologies for high-speed applications like optical communication networks, wireless communications, and automotive radar systems. He has authored or co-authored more than 100 publications, serves as reviewer for several journals, and was a member of the technical program committee of the IEDM.

Bernhard Dehlink (S'05) received the Dipl.-Ing. (M.Sc.) degree in electrical engineering (with distinction) from the Vienna University of Technology, Vienna, Austria, in 2004. He is currently working towards the doctorate degree in electrical engineering at the Vienna University of Technology.

He joined Infineon Technologies AG, Corporate Research, Munich, Germany, where he develops ICs in SiGe for automotive radar applications as part of his doctoral thesis. His current research interests are in mm-wave IC design, mm-wave systems-on-chip, and automotive radar

Werner Simbürger received the Ph.D. degree in electrical engineering from the Vienna University of Technology, Austria, in 1995.

After working for Siemens, Corporate Technology, Microelectronics Division, Munich, Germany, as a Staff R&D Engineer, he became Head of the High Frequency Research Department at Infineon Technologies AG, Corporate Research, from 1999 to 2005. From 2005 to 2006, he was responsible for the RF CMOS SoC PA development (COSIC) at Infineon, Business Group Communication Solutions. In 2007, he joined the Infineon Automotive Power Semiconductor Division with focus on ESD protection robustness.

Arpad L. Scholtz was born on January 19, 1947, in Kecskemet, Hungary. In 1956, he moved to Austria and received the Austrian citizenship in 1960. He studied telecommunications at the Technical University of Vienna, where he received the Masters degree in 1972 and the Doctor degree in 1976, both with distinction.

From 1972 to 1982, he was an Assistant Professor for radio frequency engineering at the Institute of Communications and Radio-Frequency Engineering. Since 1982, he has also acted as a lecturer at the same Institute, and in 1992, he became an Associate Professor. He is author or co-author of more than 100 scientific publications. He teaches radio frequency engineering with emphasis on electronic circuit design, antennas, and point-to-point communications.