High-Efficiency Balanced Switched-Path Monolithic SiGe HBT Power Amplifiers for Wireless Applications

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***Abstract*— Modern wireless telecommunication systems require high-efficient, linear, low cost and long talk-time solutions. The proposed novel balanced circuit for power amplifiers provides a high efficiency at maximum as well as backoff output power levels and low sensitivity to load variations. To minimize the quiescent current at low output power levels, an adaptive current-mirror bias circuit can be effectively used. Experimental results for highly efficient, linear, multi-band and multi-mode, two-stage, balanced switched-path SiGe HBT power amplifiers, intended to operate across the DCS 1800, PCS 1900, WCDMA 850 / 1900 / 2100 frequency bands, exhibit a peak power-added efficiency of ≥ 50 % at 33 dBm and ≥ 20 % at 16 dBm of output power with a minimum quiescent current of 12 mA.**

I. Introduction

Modern wireless communications systems, such as GSM / EDGE, CDMA 2000 or WCDMA, foresees the power amplifier (PA) to deliver a wide range of output powers with high efficiency as well as linearity. The power amplifiers are designed for the highest power level with maximum available efficiency, however tend to operate less efficiently at lower power levels, which shortens the life of a battery and reduces talk time duration. Nonetheless, it is possible to use a mechanism for switching the power amplifier stages with proper connection to the load [1]. In such a configurable power amplifier, where each stage has its own output matching, the amplifier provides a variable output power from its corresponding combinations. It is assumed that each stage has 50-ohm input as well as output impedance and requires switches between stages. All these prerequisites make a fully monolithic integration extremely difficult. Additionally, it results in increase of size as well as cost of the entire power amplifier. Among the potential possibilities to improve efficiency are (i) mechanism for switching the segments of the active device to reduce the quiescent current at low power mode and (ii) to switch load network to provide different impedances at high and low output power modes [2]. However, improvement is not significant unless a pin-diode is used in the load network.

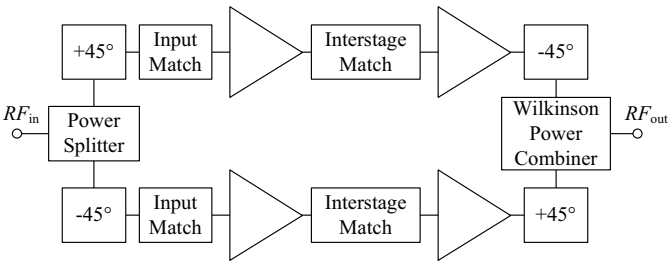

Fig. 1. Block diagram of power amplifier with improved linearity over load variations.

In addition to high efficiency, it is very important to keep a high linearity at high output power with varying load impedances. Fig. 1 depicts the circuit schematic of the power amplifier, having a 90-degree phase shift due to 45-degree shifters in each amplifying path, thereby improving the linearity over different load voltage standing wave ratio (VSWR) as compared to the conventional single-ended design [3]. This is due to the fact that each of the two transistors in a balanced power amplifier experiences opposite impedance change, i.e. higher impedance and lower impedance. The linearity holds for the lower impedance path with some beneficial increase in the output power. Thus, compared to a conventional single-ended design, only one half of the output signal experiences degrading linearity performance. However, in this case, there is no special mechanism for efficiency improvement at the back-off conditions.

Quadrature 90° hybrids can be used instead of phase shifters and in-phase power combiners / splitters. To increase efficiency in such a two-stage balanced power amplifier, the direct bypass connection can be made between two isolated ports of the 90° hybrids, as shown in Fig. 2 [4]. In this case, both high power paths are switched off, thus appearing as reflective impedances to the signal. As a result, the power from the second stage flows directly to the load, improving the efficiency at backoff (BO) considerably. However, two

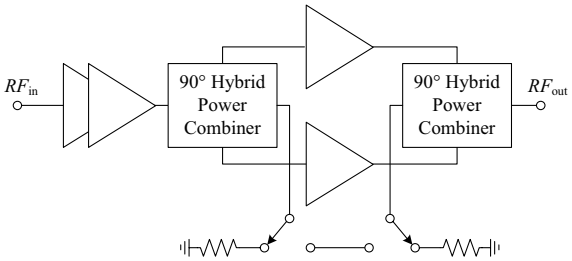

Fig. 2. Block diagram of balanced power amplifier with high efficiency at backoff.

additional switches are needed to connect both isolated ports in a low power mode and to connect each isolated port to the ballast resistor in a high power mode. The quadrature hybrid can generally be implemented with any lumped or transmission-line elements [5].

II. Balanced Switched-Path Power Amplifier

The circuit schematic of the proposed balanced switched-path power amplifier having high efficiency at different output power levels is shown in Fig 3. It incorporates an additional separate low power amplifying path, connected between the isolated ports of the 90° input hybrid power splitter and the 90° output hybrid power combiner. In the high power mode, the bias control unit provides proper biasing of the transistors in both balanced paths and switches off the biasing in a low power path. In this case, the output powers from both balanced paths combine in the output hybrid combiner and the low power path is isolated from the former, thereby providing high efficiency at high output power. For a matched hybrid branch-line combiner, power entering the input port 1 is divided between the output ports 2 and 3 with a 90° phase shift between these outputs and no power is delivered to the isolated port 4. In the low power mode, the bias control unit switches off the biasing of transistors in both balanced paths and provides proper biasing for a low power amplifying path.

A quadrature hybrid has an important advantage compared to in-phase splitters. At equal values of reflection coefficients from loads connected to the output ports 2 and 3, respectively, there is no reflection wave at the input port 1 and, consequently, input VSWR of a quadrature hybrid does not depend on the equal load mismatch level. In this case, all reflected power is dissipated in a 50-ohm ballast resistor connected to the isolated port 4. Similarly, for a quadrature combiner the reflected power from two inputs will flow to the load. As a result, the isolated port of the input hybrid becomes the input for a low power amplifying path, while the isolated port of the output hybrid works as its output 50-ohm port. Hence, high efficiency at lower output power levels can be achieved without any additional switches or pin-diodes to isolate high power balanced paths and low power path. Additionally, the adaptive biasing can be applied to the transistors in low power path to minimize quiescent current at very low output power levels, thus increasing efficiency 2 to 3 times as compared to the conventional balanced architecture. The bias control unit is operable to activate or deactivate the transistors. The quadrature hybrid can generally be implemented with any lumped or transmission-line elements. The number of stages in all power amplifier stages may be different depending on the required output power and power gain.

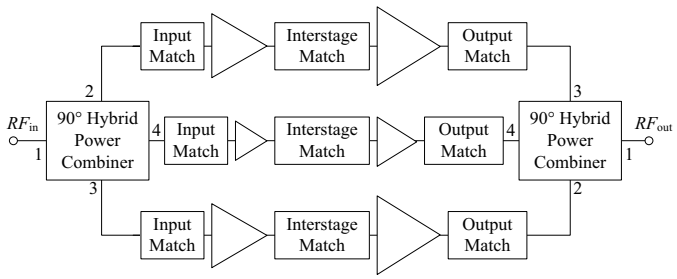

Fig. 3. Block diagram of balanced switched-path power amplifier.

III. Adaptive Bias Circuit

To provide an efficient linear power amplifier operation, it is necessary to minimize the quiescent current at backoff output powers since the maximum of the power density function for WCDMA standard occurs at an output power of about 30 dB below the saturation output power. As a current controlled device, the bipolar transistor at RF operation requires a dc base driving current, whose value depends on the output power and device parameters. From technology point of view, a bipolar device represents a parallel connection of the basic cells, important issue being the usage of ballasting series resistors to mitigate the current imbalance and possible device collapse at higher current density levels. Basic current mirror and emitter follower bias circuits can provide the temperature compensation over wide range of ambient temperatures, with very small reference current for the latter case [6]. However, adaptive bias circuit can control dc power consumption with varying output power, thus, greatly improving PAE when the output power is low and maintaining high linearity when output power is high [7]. Fig. 4 shows the schematic of the adaptive bias circuit where the value of the ballasting resistance R1 is chosen to minimize the sensitivity to the base bias current variations and its value is scaled with ballasting resistor R2 to the ratio of device areas Q2/Q1 in a reverse

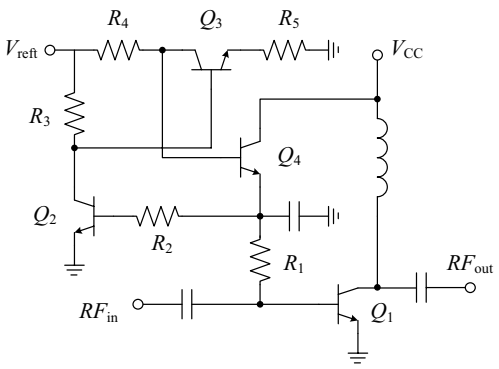

Fig. 4. Schematic of adaptive bias circuit.

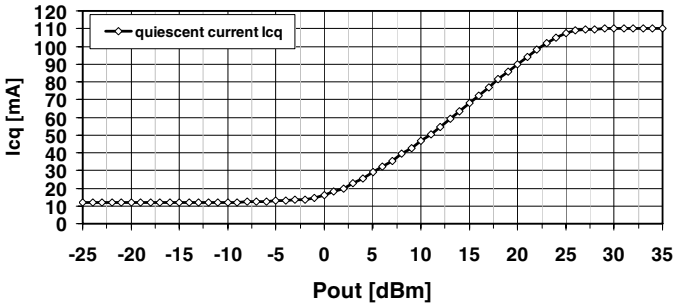

Fig. 5. Adaptive quiescent current versus output power.

proportion. A bypass capacitor is needed to isolate dc bias circuit from the RF path.

Since the RF transistor Q1 is biased to Class AB with a small quiescent current and its collector current is a function of the input power, the collector current of the current mirror device Q2 increases with input power. This increased current decreases the base voltage of the device Q3, thus decreasing its collector current. Then, this decreased collector current increases the base voltage of the device Q4 due to smaller voltage drop across the resistor R4 forcing its emitter current and the collector current of the RF device Q1 to increase. Thus, the quiescent current of the adaptive bias circuit is an increasing function of the input power. This provides high quiescent current at high output powers when high linearity with tradeoff efficiency is achieved and low quiescent current at low output powers when high linearity and increased efficiency are obtained. As an example shown in Fig. 5, the quiescent current I_{cq} varies from 110 mA at maximum $P_{\mathrm{out}} = 33$ dBm to 12 mA for low output power levels. The minimum value of quiescent current is defined by the values of resistors R4 and R5.

IV. Experimental Results

Using the Fig. 3 topology, low-band (LB) and high-band (HB) PAs were implemented covering the WCDMA 850 (band V) and PCS 1900 / WCDMA 1900 (band II) frequency bands, respectively. Both designs were implemented in a high breakdown voltage version of Infineon's 0.35-μm-SiGe HBT bipolar process [8] that is used for handset cellular transceivers. The collector-base breakdown voltage U_{cb0} is 20 V and the collector-emitter breakdown voltage U_{ce0} is 6 V. The process includes vertical PNPs, poly-Si resistors, MIM and MIS capacitors and a proprietary low-cost sinker technology on a highly doped substrate, yielding low-resistive and low-inductive connections to the substrate bottom side.

The chip layout of the WCDMA 850 PA MMIC is shown in Fig. 6. The die comprises the two-stage high power (HP) paths of 0° and 90°. Crosstalk between 0° and 90° HP paths degrade the performance with respect to output power, linearity and load sensitivity, thus, the two-stage low power (LP) path is placed between the mirror-imaged HP paths. All paths include input matching and interstage matching as well as the input hybrid in full version. Emitter area of first and second stage of each HP path and the LP path is 496 μm^2 and 4464 μm^2, 62 μm^2 and 248 μm^2, respectively. Main biasing circuitry like current mirrors is implemented on the die. In addition, space

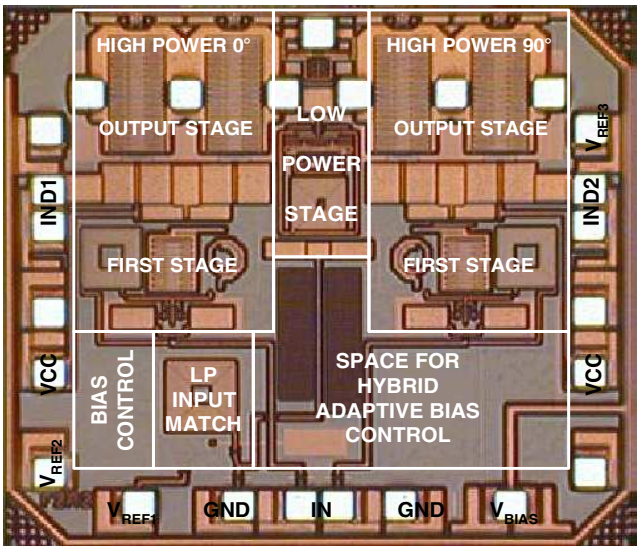

Fig. 6. Microphotograph of the low-band balanced switched-path SiGe HBT power amplifier MMIC.

is allocated for a more elaborate biasing and control circuitry including adaptive biasing, thus, the die size of 1.97 mm^2 is already the size of a fully featured SiGe PA. The interstage matching of the HP paths is implemented with two sections of a high-pass L-structure with series capacitor and a shunt inductor, realized as a bond wire (one from pad VCC, another from pad IND1 / IND2) in series with a short off-chip transmission line (TL). The matching structure is optimized for gain, bandwidth and efficiency, while reducing low frequency components and minimizing the tendency for oscillations.

The MMICs are intended for the integration in WCDMA modules including SAW, output matching, output hybrid, coupler and duplexer. For stand alone verification, the MMIC is mounted as bare die or in Infineon's 3.5×3.5 mm^2 VQFN-20 (Very thin Quad Flat package Non leaded) package on a standard FR4 board ($\epsilon_r = 4.1$@1.9 GHz). The 3.5 V collector bias voltages (VCC) are applied via short length 50 Ω microstrip (MS) transmission lines terminated with shunt SMD blocking capacitors. The output matching networks are realized with 50 Ω MS TLs and two low ESR (Electrical Series Resistance) shunt capacitors. Ceramic SMD hybrids with a loss of 0.5 dB, and a phase accuracy of ±3° were used at the input and output of the power amplifier.

The de-embedded (excess MS TL, SMA connectors) measurement results at 3.5 V supply are shown in Fig. 7. In HP-mode, a saturated output power P_{sat} of 31.5 dBm at a peak power-added efficiency $\mathrm{PAE}_{\mathrm{sat}}$ of 58 % and a WCDMA power with 3 dB backoff $P_{\mathrm{3dB\,BO}} = 28.5$ dBm at a $\mathrm{PAE}_{\mathrm{WCDMA}}$ of 41.5 % has been achieved. In LP-mode at 16 dBm a $\mathrm{PAE}_{\mathrm{WCDMA}}$ of 20 % has been achieved. The LP-mode has a saturated output power P_{sat} of 18 dBm at $\mathrm{PAE}_{\mathrm{sat}}$ of 30 % and operates at a quiescent current $I_{\mathrm{cq,LP}}$ of 14.5 mA including the reference current.

The high-band design uses the same circuit topology, floor plan, pinning and board layout, as described for the low-band MMIC. Table 1 summarizes the measurement re-

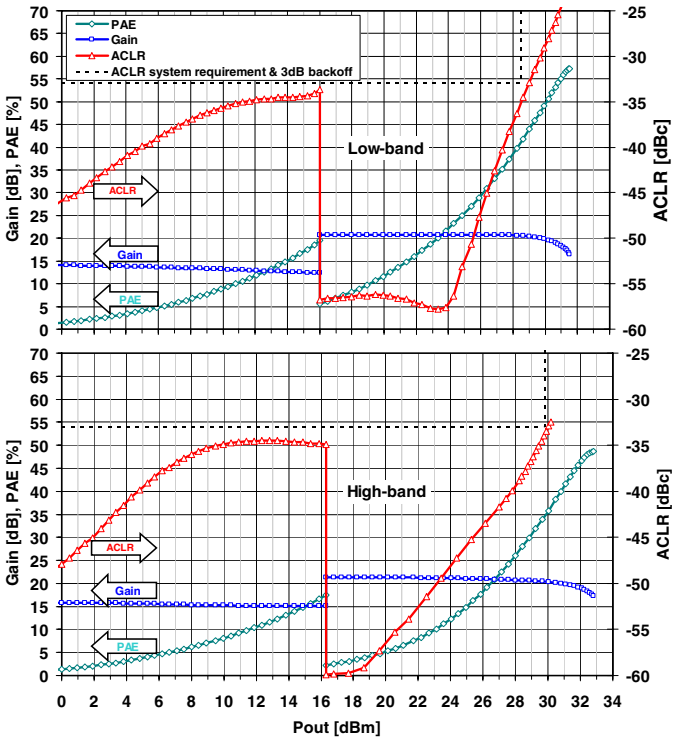

Fig. 7. Gain, PAE and ACLR versus output power (measurement) (top: low-band, bottom: high-band).

TABLE I

PERFORMANCE OF HIGH-BAND BALANCED SWITCHED-PATH SIGE HBT POWER AMPLIFIER (MEASUREMENT).

Frequency [MHz]	P_{out} [dBm]	PAE [%]	Gain [dB]	ACLR [dBc]
1850	33	48	17	–
	30	36	21	-35
	16	18	15	-35
	12	11	16	-35
	6	5	16	-37

sults of the PCS 1900 / WCDMA 1900 band. These results demonstrate the feasibility of the concept at high frequency bands. Similar results can also be achieved for the DCS 1800 and WCDMA 2100 bands. In a general case of multi-mode and multi-band application, our PA can easily be tuned to simultaneously cover the entire frequency range including constant-envelope DCS 1800 / PCS 1900 and non-constant envelope WCDMA 1900 / WCDMA 2100 bands providing high efficiency and linear operation.

Investigations of the PA's sensitivity to load variations in HP-mode were done with a passive load pull tuner. Fig. 8 shows the variation over a VSWR range of 1:1 to 4:1 and at an output power 1.5 dB above P_{WCDMA}. As shown, the PA output is well matched to a 50 Ω load. The variation over a 1.7:1 VSWR magnitude at the hybrid output reduces the output power by typ. $|P_{\text{VSWR}} - P_{\max}| = -0.7$ dB which is rather low in variation over phase of $P_{\text{VSWR}} = \pm 0.08$ dB. A VSWR of 1.7:1 at the hybrid output interface corresponds to a VSWR requirement of 2.5:1 at the antenna, assuming a total front-

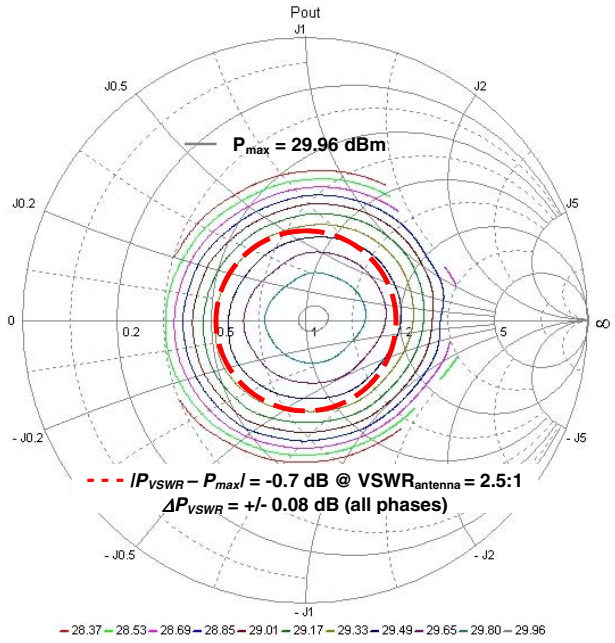

Fig. 8. Output power [dBm] vs. load variations at 1.85 GHz

end loss of 1.9 dB. The low load sensitivity demonstrates the usefulness of the proposed balanced switched-path concept.

V. CONCLUSIONS

The novel concept of a balanced switched-path power amplifier to obtain high efficiency and high linearity over a wide range of the output powers in low-voltage handset power amplifiers is presented. To minimize the quiescent current at low output powers, an adaptive current-mirror bias circuit can be effectively used. Experimental results for high efficiency, linear multi-band and multi-mode two-stage balanced switched-path SiGe HBT power amplifiers, intended to operate across DCS 1800, PCS 1900, WCDMA 850 / 1900 / 2100 frequency bands, with power-added efficiency of $\geq 50\,\%$ at maximum output power and $\geq 20\,\%$ at 16 dBm output power with a minimum quiescent current of 12 mA are shown.

REFERENCES

[1] J. Staudinger, "Applying switched gain stage concepts to improve efficiency and linearity of mobile CDMA power amplification," *Microwave J.*, vol. 43, pp. 152–162, Sept. 2000.

[2] A. V. Grebennikov, H. Jaeger, and E. P. Heaney, "High-efficiency cellular phone transmitters with reduced power consumption," in *Proc. European Conf. Wireless Technology*, 2002, pp. 115–118.

[3] S. W. Chang, H. J. Finlay, N.-S. Cheng, and B.-S. Park, "Load variation tolerant radio frequency (RF) amplifier," U.S. Patent 6 954 623, Oct., 2005.

[4] J. Klaren, C. J. Persico, S. Walter, and P. L. Chan, "Balanced power amplifier with a bypass structure," U.S. Patent 6 806 768, Oct., 2004.

[5] A. V. Grebennikov, *RF and Microwave Power Amplifier Design*. McGraw-Hill, 2004.

[6] T. Sato and C. Grigorean, "Design advantages of CDMA power amplifiers built with MOSFET technology," *Microwave J.*, vol. 45, pp. 64–78, Oct. 2002.

[7] Y. S. Noh and C. S. Park, "An intelligent power amplifier MMIC using a new adaptive bias control circuit for W-CDMA applications," *IEEE J. Solid-State Circuits*, vol. SC-39, pp. 967–970, June 2004.

[8] W. Klein and B. U. H. Klepser, "75 GHz bipolar production technology for the 21th century," in *Proc. ESSDERC*, 1999, pp. 88–94.