A Quad-Band GSM/EDGE-Compliant SiGe-Bipolar Power Amplifier with 35.9 dBm / 32.3 dBm Output Power at 56 % / 44 % PAE in Low/High-Band

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***Abstract* — A standard-compliant integrated quad-band GSM/EDGE radio frequency power amplifier for 824−915 MHz and 1710−1910 MHz has been realized in a 0.35-μm SiGe-Bipolar technology. The chip integrates two single-ended 3-stage power amplifiers and a bias-control circuit for power control, band select and mode dependent quiescent currents. At 3.3 V a saturated output power of 35.9 dBm is achieved at 830 MHz and 32.3 dBm at 1710 MHz. The respective peak PAE is 56 % for low-band and 44 % for high-band.**

***Index Terms* — Power amplifiers, Silicon bipolar, RF circuits, analog circuits, GSM, EDGE, mobile phone**

I. Introduction

Today's handset power amplifier (PA) products are dominated by III/V (GaAs HBT) semiconductors, integrated in a module package with embedded passives including most of the interstage and output matching [1], [2]. Control functions are usually realized by a separate CMOS die with logic and bias functions. Whereas III/V semiconductors offer very good RF performance in terms of efficiency, linearity and robustness, the integration of passives is a prohibitive costly issues. Silicon is proven to allow low cost integration of passive devices such as inductors, transformers [3] and capacitors [4] as well as a cost-efficient, low-inductance RF-ground [5]. Hence, using Si-based technologies further integration towards a single die is possible, including the integration of control functions. The main issues regarding the realization of Si and SiGe based PAs are the linearity required for upcoming EDGE phones and the ruggedness. In detail, the performance of the SiGe-HBT is limited by the avalanche breakdown voltage. According to the authors knowledge, no Si or SiGe based power amplifier fulfilling all GSM specifications such as noise at 20 MHz offset, ruggedness, output power and even the linearity requirements in EDGE mode with reasonable efficiency including all control currents, has been reported.

This work presents such a fully integrated power amplifier including all functional blocks on one die, except the output matching and the required collector chokes. The simplified circuit of the PA with emphasis on the RF stages is shown in Fig. 1. It consists of two PA cores, one for low-band (824-915 MHz) and one for high-band (1710-1910 MHz). In addition, a bandgap reference and a bias control logic for band-select and different current levels are integrated. Further, a power control loop, consisting of an operational amplifier, a loop filter and an off-chip PMOS transistor is integrated. The circuit includes a battery tracking to prevent loop saturation effects. The low-band RF core features a gain switching function to reduce the small signal gain in EDGE mode. This solution eases fulfilling the output noise specifications in combination with today's RF transceivers.

II. Technology

The design is implemented in Infineon's 0.35-μm SiGe-bipolar high-volume process [6] featuring a high voltage heterojunction bipolar transistor and a three layer Al-metalization with a 2.8 μm thick top layer. Further devices are a vertical pnp transistor, poly-Si resistors, MIM capacitors, MIS capacitors and inductors. The typical collector-base breakdown voltage is BVCB0 = 20 V and the collector-emitter breakdown voltage is BVCE0 = 5.5 V. An important feature is the additional lightly doped buried layer in the output transistor stage [7], protecting it from destruction in case of mismatch or over-voltage. In order to realize low-inductance at the HBT emitters to reduce feedback, a low-ohmic substrate connection (sinker) is implemented. The substrate has a resistivity of 15 $m\Omega\, cm$, resulting in a very low inductance compared to bondwires. Fig. 2 shows the die photograph of the fully integrated power amplifier. The die size is 2.9 x 3.0 mm^2 and shows further shrinkage potential.

III. Circuit Design

Fig. 1 shows the circuit diagram of the power amplifier. Starting with the low-band RF core (top), the PA

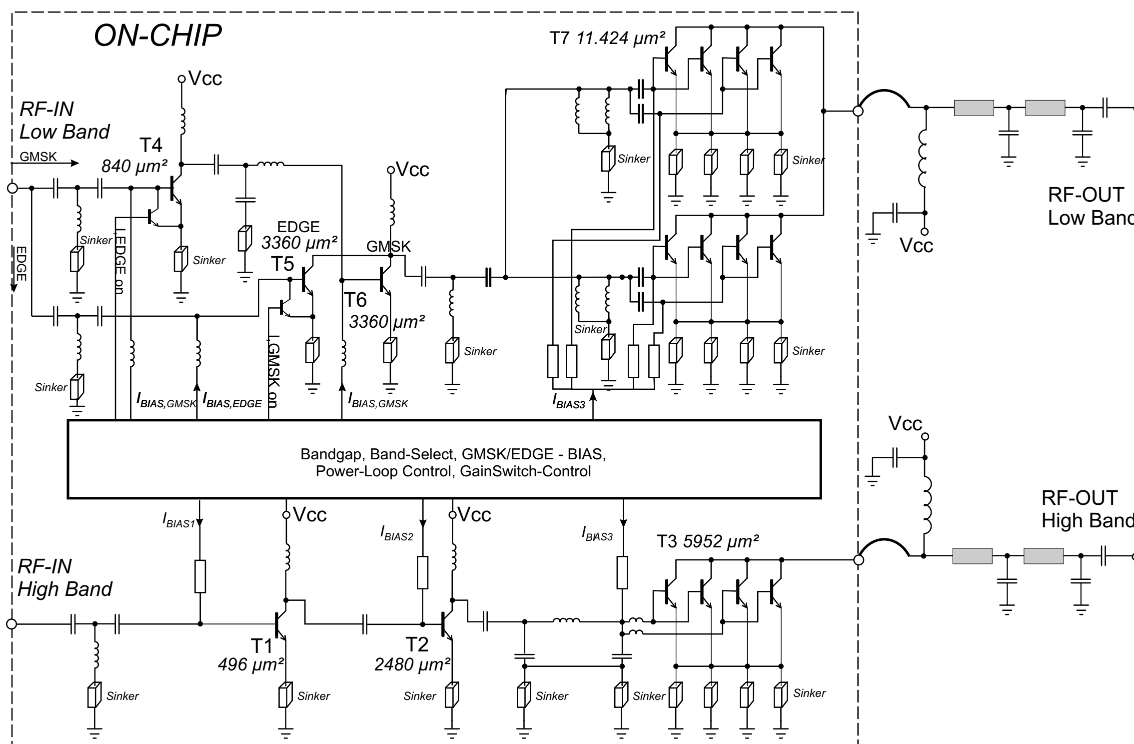

Fig. 1. Simplified circuit diagram of the integrated power amplifier with low-band path at the top and high-band path at the bottom.

represents a 2-stage amplifier in EDGE mode and a 3-stage amplifier in GMSK mode. The switching is done via bias currents. In addition transistors which shunt the RF signal at the base of the inactive transistor prevent undesired self-biasing in the disabled path. In GMSK mode the PA uses a high-pass type input matching for the input transistor T4. To achieve an acceptable noise performance, all low-band stages are biased using chokes which are on-chip except

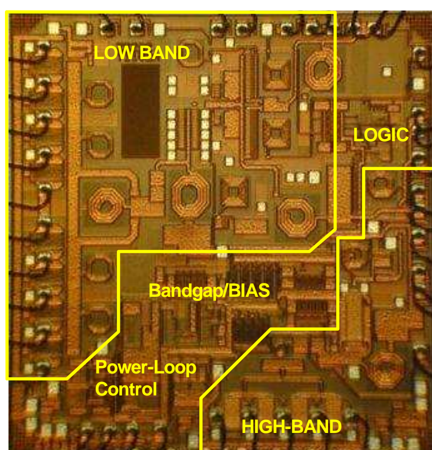

Fig. 2. Die micrograph of the power amplifier.

for the output stage. In EDGE mode the RF signal bypasses directly to the second stage (T5) with the first stage (T4) switched off. This results in a gain step of about -10 dB and offers a better noise performance. The creation of an RF matching that achieves a homogenous RF input current to each transistor cell is a design challenge. Hence, in the low-band a series capacitor is used in combination with four shunt inductors supplying the output stage which is split into 8 blocks, each biased with its own current mirror. In the high-band a physically asymmetric but electrically symmetric (L,C,R) fishbone structure facilitates the RF current distribution to the transistor blocks. The planar structure is optimized by EM simulations. The transistor blocks are layouted with base, emitter and collector stripes connected on both sides to improve the breakdown behavior. Thus, the effective transistor length with respect to current crowding is halved. In addition the ruggedness of a double-side connected 40 μm long emitter is even better compared to a single-side connected 20 μm one. Due to the extremely low base impedance of about 200 $m\Omega$ a wideband multi-stage matching with low losses is necessary to achieve the required driving power into the output stage. To overcome the considerably lower Q-factor available on a low-ohmic substrate, the interstage matching is realized using an inductive fishbone structure followed by an LC-type matching with planar inductors. To

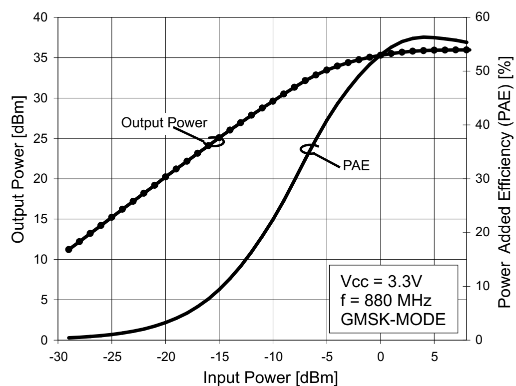

Fig. 3. Measured low-band power transfer characteristic.

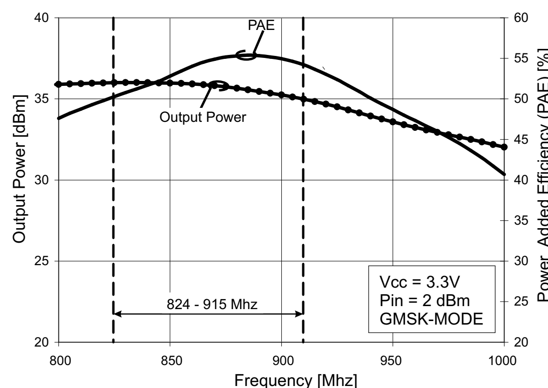

Fig. 4. Measured low-band power amplifier frequency response.

improve the quality factor, octagonal shaped coils are used. Further, the low-pass type matching shows lower losses. However, fishbone structures may exhibit instabilities like unwanted differential modes between transistor blocks, unless precautions like common-mode biasing are used. The major differences in the high-band design are the lower output power and the relaxed GSM noise specification by 10 dB. The system requires less dynamic range, thus a GSM/EDGE switch is omitted, and biasing feeds can be realized with resistors instead of lower noise inductors. Finally, the higher impedance level simplifies the interstage matching and reduces loss. Due to the higher frequency and the lower output power requirements, the output stage is optimized differently. Lower power allows the use of fewer transistors with wider emitter stripes for overall lower parasitic capacitance of the block. The improvement in parasitic capacitance exceeds the degradation of f_T caused by wider emitter stripes. To achieve an integrated emitter ballasting without the need of discrete resistors, the emitter stripe via placement is shifted to the emitter finger edges. Together with the asymmetric fishbone structure a high ruggedness is achieved. The result is comparable to [8] but with less efforts in technology.

IV. Experimental Results

For the test setup, the PA is packaged in a VQFN leadless package. The packaged PA is soldered onto an FR4 PCB featuring the RF-chokes for the collectors as well as two soldered EPCOS HQF capacitors. Ruggedness testing was performed using an automatic load-pull tuner. Under CW-operation and supply voltages of up to 4.5 V no damage or degradation at maximum output power occurred. For short-time operation tests (several bursts), the devices survived supply voltages of up to 6 V under 8:1 VSWR mismatch.

Fig. 3 shows the measured low-band power transfer characteristic. The maximum output power is 35.9 dBm at 3.3 V supply voltage and 830 MHz. The maximum PAE is 56%. The small signal gain can be reduced by 10 dB using the EDGE mode. However the maximum reachable output power remains the same. Fig. 4 shows the well-centered low-band frequency response with respect to output power and PAE.

The linearity for EDGE was tested using a Rohde& Schwarz SMIQ Generator and an FSIQ Spectrum Analyzer. Fig. 5 depicts the spectral mask level measurements at 400 kHz and 600 kHz vs. average input power levels which show sufficient margin. Additionally the EVM value is below the target of 5 %. A very important specification in the lower GSM bands is noise, whereas the high-band GSM specification is relaxed by 10 dB. The noise measurement result of the low-band is presented in Fig. 6. The high-band design yields very similar measurement results, thus not shown.

The high-band frequency response is shown in Fig. 7. The frequency centering of the PA turned out too low. The source of the decentering is found in the matching between the first and second stage. The resulting high-band power transfer characteristic is shown in Fig. 8. The respective EDGE efficiency is 26 % for 28.5 dBm output power. Finally Table I shows an overview of reported state of the art GSM PAs in comparison with this work.

Citation	This	[1]	[3]	[9]
Technology	SiGe	GaAs	SiGe	Si-LDMOS
Quad Band	✓	✓	900 MHz	✓
Pout [dBm] PAE [%]	35.9/32.3 56/44	35/33 50/49	35.7/- 59/-	35/33 53/48
EDGE	✓	✓	-	-
Noise [dBm]	-85	-87..-82	n.n.	n.n.

TABLE I
State of the Art PA comparison

V. Conclusions

We have demonstrated a standard-compliant quad-band GSM/EDGE RF power amplifier in a high-

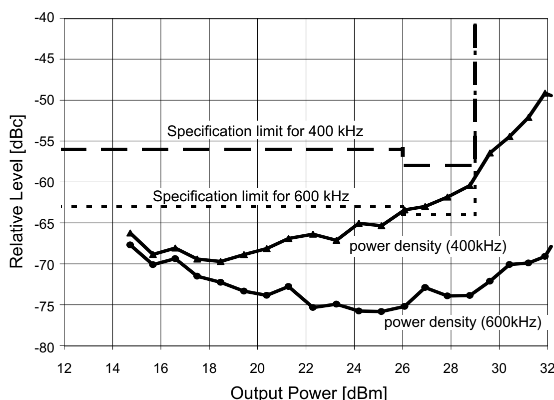

Fig. 5. Measured 400/600 kHz Spectrum Mask vs Input Power (Low-band)

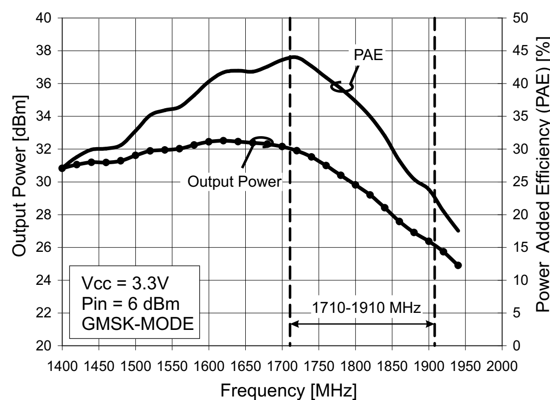

Fig. 7. Measured high-band power amplifier frequency response.

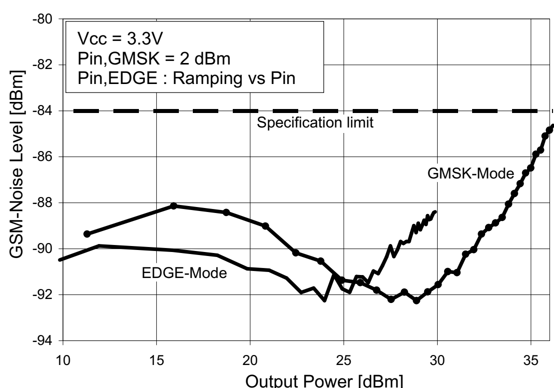

Fig. 6. Measured low-band 20 MHz noise output power.

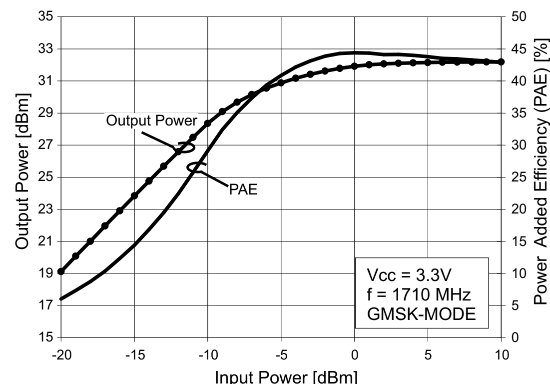

Fig. 8. Measured high-band power transfer characteristic.

volume 0.35 μm- SiGe technology. The chip integrates all interstage matching and control functions on one die and fulfills all standard-compliant specification parameters like output power, efficiency, linearity, noise and ruggedness found today only in III-V technology based modules. At 3.3 V a saturated output power of 35.9 dBm is achieved at 830 MHz and 32.3 dBm at 1710 MHz. The respective peak PAE is 56 % for low-band and 44 % for high-band. The measured 20 MHz noise performance succeeds the -85 dBm requirement for all input power levels.

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