

DESIGN METHODOLOGY FOR SIGNAL PROCESSING IN WIRELESS SYSTEMS

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ABSTRACT:

Design of modern wireless communication systems is increasingly inefficient. A lot of different problems arise, which require an improvement of currently used design methodologies. Significant increases in efficiency, reduction of time to market and improvement in quality can be achieved by adopting a consistent design methodology.

INTRODUCTION

Modern wireless communication systems require the deployment of highly sophisticated signal processing algorithms and increasingly complex protocols in shorter and shorter time periods [1]. Implementations of these systems are increasingly heterogeneous, incorporating diverse hardware components such as DSPs, FPGAs and ASICs, as well as software components at various abstraction levels, written in assembler, C, C++, Java, SystemC and other high as well as low-level languages.

SHANNON BEATS MOORE

According to Moore's Law the number of transistors that can be integrated on one chip is doubling every 18 months. However, the needed complexity to integrate future wireless communication systems is growing much faster than this available computational power. Therefore it will be not possible to use standard processors alone for the implementation of 3G and 4G systems.

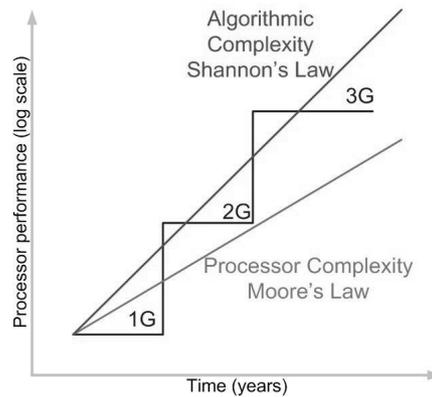


Figure 1: Shannon beats Moore

DESIGN PRODUCTIVITY GAP

Another additionally problematic point for the design process is the so-called design productivity gap. The number of transistors that can be integrated on one chip is growing more rapidly than the number of transistors that can be designed per staff month. History shows that this productivity gap occurred already several times and has been closed by raising the abstraction level of the used description, as with the introduction of place and route tools, hardware description languages, and hardware synthesis.

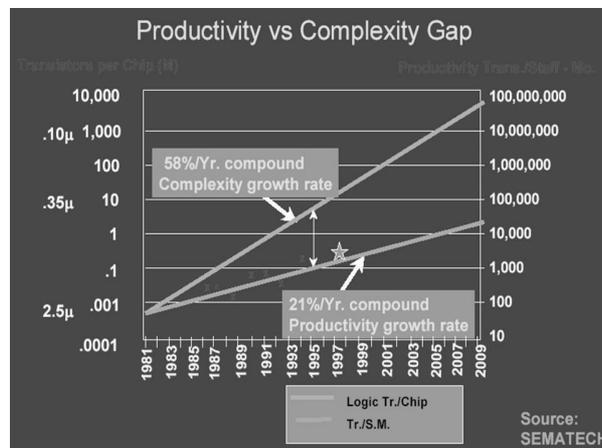


Figure 2: Design Productivity Gap

CURRENT DESIGN FLOW

The design process, leading from concept to realization, passes through three general levels of refinement, namely the algorithmic, the architectural and the implementation levels.

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Typically, three separate teams can be associated to one of these stages each [2], as shown in Figure 3.

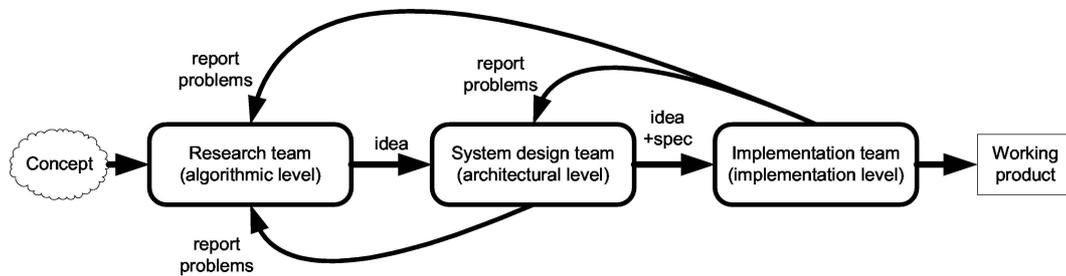


Figure 3: Different teams in the design flow.

In the design process, the three teams have necessarily distinct areas of expertise, to tackle each of the three stages. Inherently, each of the teams works with a dedicated set of tools on a system description that is optimized for their work. As such, this framework has several shortcomings. Firstly, descriptions of the system at the three stages of the design process are fundamentally different, making forward and backward communications between teams highly difficult. Consequently, system descriptions are constantly reformatted and rewritten by the corresponding experts to incorporate input from the other teams. This mode of operation is error-prone, slow and inefficient. The backward tracking of an error is nearly impossible.

Furthermore, the impeded communications between teams can lead to delayed discovery of design faults. As a rule of thumb, a fault that produces a cost of 1€ when found at the algorithm level will produce a cost of 6€ when discovered at the architectural level and even 100€ at the implementation level (Figure 4)[4].

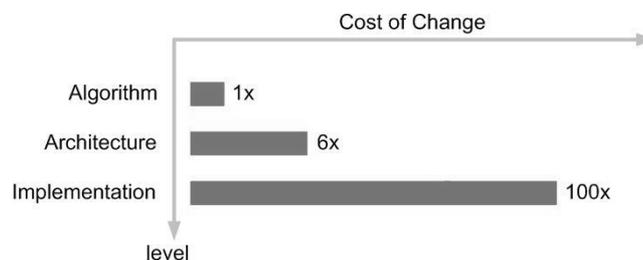


Figure 4: Cost of change

All the mentioned drawbacks of the current design process are especially severe in the wireless field. Increasing complexity of algorithms, such as in UMTS and EDGE, as well as the extremely tight time to market and cost requirements, together place a great burden on the design process. Complex designs must be produced quickly and correctly the first time.

FUTURE DESIGN FLOW

Clearly, significant increase in efficiency, reduction of time to market and improvement in quality can be achieved by providing a consistent design process (see Fig. 5). Such a process has to provide a unified design environment [5], supporting all teams equally and allowing them for working on a single system description. Thus, each team will apply its expertise and refine the description (single system description) on its way from concept to realization. However, at any point in time each team will have insight into the current description of the system, without translation, thus avoiding the communication obstacles.

In this improved process, each team still requires its usual set of tools. Hence, a unified design environment will have to seamlessly integrate all the existing tools required by all the three teams, as they are provided by many EDA tool manufacturers (for example, SPW from CADENCE, CoCentric System Studio form SYNOPSYS, or N2C from CoWare). The most important aspect of this integration is the binding of each tool to the single system description. Since there exists only one system description, but a great variety of tools, each with unique requirements, means of providing inputs for and incorporating outputs of all the tools must be provided.

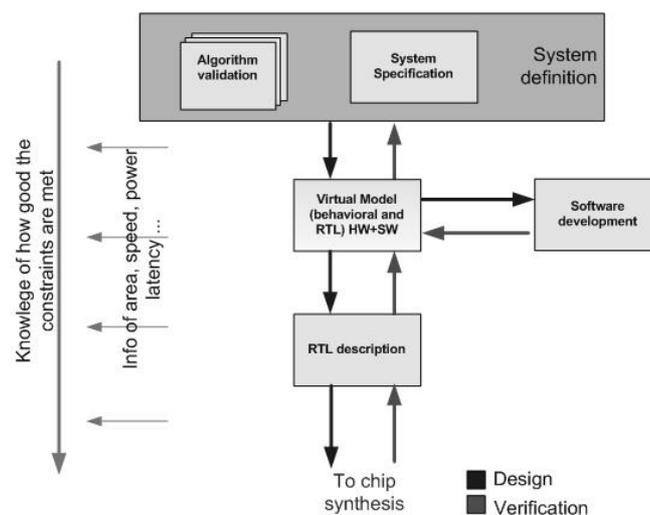


Figure 5: Consistent Design Flow

Even when all the currently available tools used by the three teams are integrated into a unified design environment, significant steps in the design process are not covered. These are the steps that are currently carried out manually and only made possible by the expertise and experience present in the three design teams. Completeness of any consistent design process hinges on its ability to allow these design steps to be performed on the single system description, either directly and manually by the corresponding experts, or automatically by newly available dedicated tools. Examples of such significant, yet manual or badly supported tasks are hardware/software partitioning, architecture mapping, bitwidth optimization, rapid/virtual prototyping, and consistent verification.

CONCLUSION

It has been shown that there is a tremendous need to improve the design process for wireless systems in order to be prepared to cope with the complexity of future systems. A single system description and a unified design environment for all teams in the design process has the potential to improve efficiency, reduce time to market, cut costs as well as to improve quality.

ACKNOWLEDGEMENT

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REFERENCES

1. V. N. Patel, C. K. Wiese, F. M. Hiemstra, and S. Himes, "Rapid Development and Commercialization of Products-A Business Imperative in the Global Telecommunication Landscape", Bell Labs Technical Journal, pp. 157-171, October-November 2000.
2. M. Rupp, A. Burg, and E. Beck, "Rapid Prototyping for Wireless Designs: the Five-Ones Approach," Signal Processing, Vol. 83, Issue 7, pp. 1427-1444, July 2003.
3. T. Grötter, S. Liao, G. Martin, and S. Swan, "System Design with SystemC", Kluwer Academic Publishers, 2002. ISBN 1-4020-7072-1.
4. R. S. Janka, "Specification and Design Methodology for Real-Time Embedded Systems", Kluwer Academic Publishers, 2002, ISBN 0-7923-7626-9.
5. P. Belanović, M. Holzer, D. Mičušik, and M. Rupp, "Design Methodology of Signal Processing Algorithms in Wireless Systems", Proc. of the International Conference on Computer, Communication and Control Technologies CCCT'03, Orlando, July 2003.