# Hardware Implementation and Characterization of SiC-Based Hybrid Three-Phase Rectifier Employing Third Harmonic Injection

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***Abstract*—A recently proposed third harmonic injection rectifier (two half-bridge legs) – serving as optional solution for passive three-phase diode bridge systems with LC output filter – is characterized by unity power factor ($\lambda \approx 1$) and low harmonic input currents ($\mathrm{THD} < 5\,\%$). The rectifier at hand, furthermore sticks out of the crowd due to a very low number of active and passive switches compared to similar power electronic circuits based on the same (third harmonic injection) principle. Additionally, the more and more establishing and reliable SiC-MOSFET allows an optimized design for higher switching frequencies without seriously impairing the efficiency of the total system. A proper design of active and passive components of the optional circuit is therefore required and several operating modes and optimization possibilities are existing. Besides basic considerations of control structures and topology limitations, also various implementation issues are discussed. Finally, experimental results of a laboratory prototype based on a 10 kW/72 kHz rectifier system using SiC-MOSFETs verifies the proper behaviour of the proposed upgrade.**

***Index Terms*—Three-Phase AC-DC Conversion, Third-Harmonic Injection, SiC-MOSFET**

## I. Introduction

Although, numerous promising AC-to-DC rectification circuits evolved during the last decades, recent developments and breakthroughs in the fields of wide band-gap devices heated up debates and discussions about already existing topologies. Rather unconventional rectifier circuits can also come handy again. Besides the very well known bidirectional three-phase six switch boost type (cf., [1]) or unidirectional VIENNA rectifier [2], one very promising solution to guarantee low harmonic input currents is based on the third harmonic principle (as described in [3] and [4]). This specific technique generally consists of two different circuits:

- current shaping circuit
- current injection stage.

Both circuits can be implemented as either passive or active setup. Converter systems based on the third harmonic injection principle can hence be classified into

- passive current shaping/passive current injection [5]–[8]
- active current shaping/passive current injection [9]–[12]
- passive current shaping/active current injection [13]
- active current shaping/active current injection [14]–[20].

Topologies which apply passive current injection and passive current shaping are generally limited in their minimum input current distortions by values close to 5 % (cf., [6]). This limitation is mainly evoked due to the passive implementation of both networks, as only sinusoidal wave shapes with multiples of the fundamental frequency can be generated. These currents are depending on the circuits resonance frequency which is defined due to capacitive and inductive components.

Circuits based on passive current injection and active current shaping are in principle limited in their performance due to similar issues. B6 output currents are indeed now controllable, the injection current is, however, still dependent on the LC injection network or appropriate transformer (YD, zig-zag, etc.). Topologies as the MINNESOTA rectifier therefore similarly suffer from limited input current distortions of approximately 4 %-5 % depending on characteristics of mains input impedance. Nonetheless, the output voltage of the circuit can be regulated, due to the active circuit directly connected to the adjacent passive diode bridge (dependent on the utilized DC/DC converter stage: buck-type, boost-type [9], buck+boost-type [11]).

One very promising solution for active injection and passive shaping is proposed in [13]. Series connected capacitors and a resistive delta or star connected network is used to facilitate properly shaped currents. Capacitors are used for blocking the DC components within the resistive network. The system can be designed to result in a $\mathrm{THD_i}$ of 0.6 %. The circuit then, however, suffers from a very poor efficiency (e.g. 90 % for the specified nominal operating point) due to the implemented resistors which form more than 80 % of the total system losses. If improved efficiency of the current shaping network is required, all resistors can hence be replaced by switching resistance emulators, which however will increase the complexity of the enhanced circuit.

Some rectifier circuits where both, the injection and shaping network are active solutions are listed in [14]–[19]. The SWISS rectifier for example offers sinusoidal input currents. Major drawbacks of this circuit are that (i) (at least) two active semiconductors have to process the full amount of output power and (ii) the structure cannot be used to extend an existing passive three-phase rectifier to a low harmonic input stage.

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A solution as proposed in [19] would allow such an upgrade for passive three-phase rectifiers. Due to the required 3-level NPC circuits a rather high number of active and passive switches is required. Therefore, a topology with two half-bridges connected in series (less number of switches) is discussed in this paper. If the third harmonic injection circuit is, however, going to serve as option/upgrade for a passive three-phase rectifier with LC output filter some major restrictions are applying in order to fulfill IEEE519/IEC61000-3-2 standards [21], [22]. Current shaping issues are hence going to be discussed in Section II.

## II. Operating Principle

### A. Basic Considerations

**Fig. 1(a)** depicts the passive three-phase diode bridge rectifier with LC output filter, upgraded by an additional circuit (active current shaping network and current injection device) based on the third harmonic injection principle. The current shaping network is realized by two half-bridge legs connected in series, whereas the output of the upper converter stage is connected to the positive bus bar and the output of the lower bridge leg linked to the negative output of the B6 (via two chokes $L_{\mathrm{cp}}$ and $L_{\mathrm{cn}}$, respectively). The interconnection between AC-side mains and midpoint $M$ of the shaping network is formed via three bidirectional switches $S_{\mathrm{i,ab}}$, which are in this specific case implemented as back-to-back IGBTs or SiC-MOSFETs. Also different solutions as reverse blocking IGBTs etc. are applicable. The output voltage $V_{\mathrm{o}}$ of the rectifier is defined due to the mains situation and calculates to

$$V_{\mathrm{o}} = \frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi}. \tag{1}$$

The DC-side smoothing inductance current $i_{\mathrm{L}}$ is characterized according to B6 output voltage $v_{\mathrm{rec}}$ and $V_{\mathrm{o}}$ and calculates to

$$i_{\mathrm{L}}(\varphi_{\mathrm{N}}) = I_{\mathrm{o}} - \frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\sum_{k}^{\infty}\frac{2}{(6k)^3 - 6k}\sin(6k\varphi_{\mathrm{N}}). \tag{2}$$

The current ripple of $i_{\mathrm{L}}$ is mainly defined by a 300 Hz spectral component, evoked due to the 300 Hz passive three-phase rectifier voltage $v_{\mathrm{rec}}$. The half-bridge leg connected to the DC capacitor $C_{\mathrm{cp}}$, has to facilitate a compensational current $i_{\mathrm{cp}}$, which completely suppresses the 300 Hz current ripple and guarantees sinusoidal wave shapes e.g.

$$i_{\mathrm{pos}} = \hat{I}_{\mathrm{N}} \cdot \cos(\varphi_{\mathrm{N}}) \quad \text{for} \quad \varphi_N \in \left[-\frac{\pi}{3} \ldots \frac{\pi}{3}\right]. \tag{3}$$

The current of the positive bus-bar $i_{\mathrm{pos}}$ is hence constituted by fractional parts of $\cos(\varphi_{\mathrm{N}})$, $\cos\left(\varphi_{\mathrm{N}} - \frac{2\pi}{3}\right)$ and $\cos\left(\varphi_{\mathrm{N}} - \frac{4\pi}{3}\right)$. $i_{\mathrm{pos}}$ is therefore now defined by $\max(i^*_{\mathrm{N1}}, i^*_{\mathrm{N2}}, i^*_{\mathrm{N3}})$ and hence results in

$$i_{\mathrm{pos}} = G_{\mathrm{e}}\frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi}\left(\frac{1}{2} + \sum_{k}^{\infty}\frac{(-1)^{k+1}}{(3k)^2 - 1}\cos(3k\varphi_{\mathrm{N}})\right). \tag{4}$$

Same assumptions are applicable for injection current $i_{\mathrm{cn}}$ and generated bus-bar current $i_{\mathrm{neg}}$. The third harmonic current $i_{\mathrm{h3}}$ is defined according to $i_{\mathrm{cp}} - i_{\mathrm{cn}}$ and similarly (as $i_{\mathrm{pos}}$ and $i_{\mathrm{neg}}$)

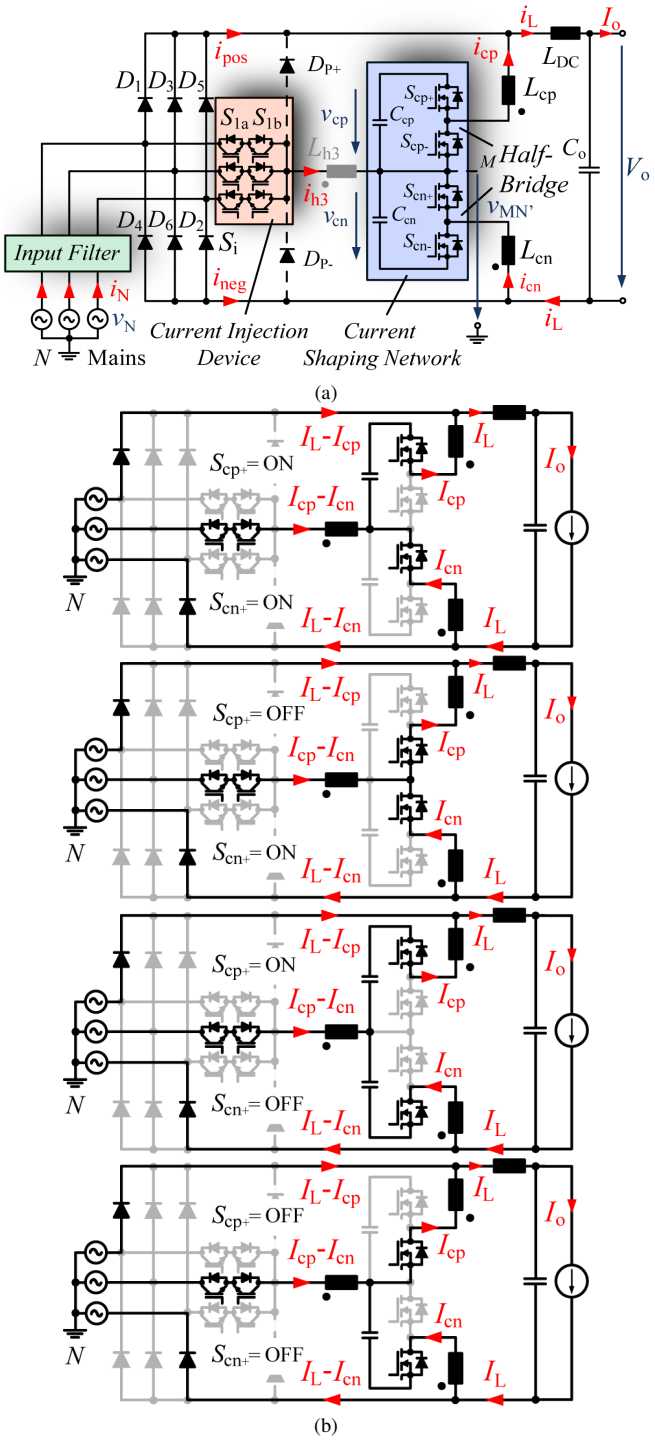



Fig. 1: (a) Passive three-phase rectifier with adjacent LC-output filter equipped by an optional third harmonic injection circuit with two half-bridge stages, three bidirectional switches in back-to-back arrangement and two/three (optional) injection inductors as proposed in [23]. (b) Feasible switching states of third harmonic injection based rectifier for the sector $\varphi_N \in [0 \ldots \frac{\pi}{3}]$.

results in sinusoidal wave shapes. This third harmonic current $i_{\mathrm{h3}}$ is going to be injected into the appropriates mains phase which is instantaneously not conducting current. Sinusoidal mains input current for e.g. phase 1 is therefore assembled

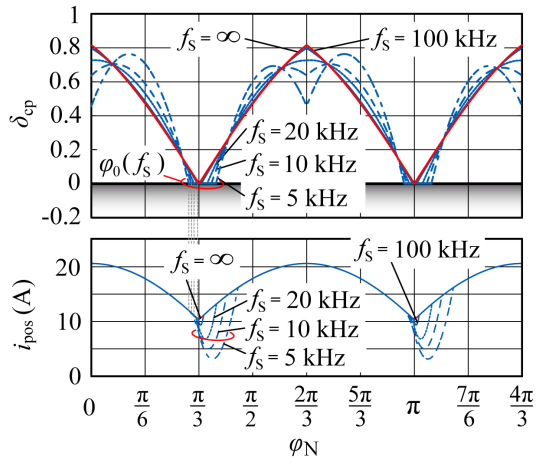



Fig. 2: (Top) – Ideal (red) and real duty cycles $\delta_{cp}$ considering voltage drop $v_{L,cp}$, for different switching frequencies (resulting in different inductance values – $f_s = 5\,\text{kHz} \mathrel{\widehat{=}} L_{cp} = 9.6\,\text{mH}$, $f_s = 100\,\text{kHz} \mathrel{\widehat{=}} L_{cp} = 480\,\mu\text{H}$), if two inductors and synchronized pulse width modulation signals are used. (Bottom) – Appropriate calculated current distortions (no voltage/current controller considered).

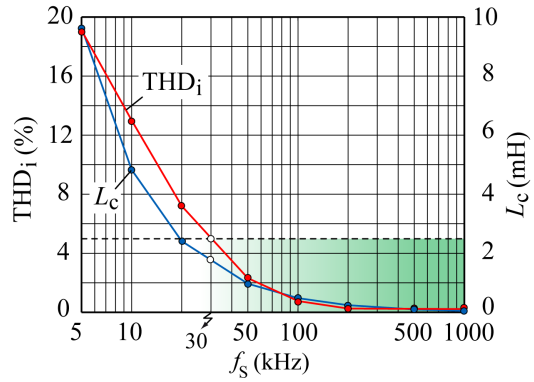



Fig. 3: Dependency of mains input current distortion $\text{THD}_i$ on injection chokes $L_{c\,\frac{p}{n}} = L_c$ and (hence) switching frequency $f_s$ (assumption: two inductors $L_{c\,\frac{p}{n}}$ and synchronized PWM).

according to the following sequence:

- $i_{N1} = i_{pos}$ for $\varphi_N \in [-\pi/3 \ldots \pi/3]$
- $i_{N1} = i_{h3}$ for $\varphi_N \in [\pi/3 \ldots 2\pi/3]$
- $i_{N1} = i_{neg}$ for $\varphi_N \in [2\pi/3 \ldots 4\pi/3]$
- $i_{N1} = i_{h3}$ for $\varphi_N \in [4\pi/3 \ldots 5\pi/3]$

Not only the sequence at hand but also **Fig. 1(b)** indicate that diodes of the passive rectifier are only switched with $f_N$(=50 Hz) and the bidirectional switches ($S_{i,ab}$) of the current injection device with $2f_N$(=100 Hz). Consequently, only the two half-bridge legs are operating with switching frequency $f_s$. All possible occurring switching states for one sector e.g. $\varphi_N \in [0 \ldots \frac{\pi}{3}]$, available for current shaping of $i_{pos}$ and $i_{neg}$, are therefore depicted in **Fig. 1(b)**.
Finally, it has to be mentioned that due to the low switching operation of the passive rectifier bridge, no high-frequency CM voltage appears at the output $V_o$.

### B. Fundamental Issues

As the main operating principle of the proposed third harmonic injection circuit has been discussed, some major operating boundaries are now going to be specified.
The required duty cycles for proper current shaping of the system are defined by

$$\delta_{cp}(\varphi_N) = \frac{v_{pos}(\varphi_N) - v_{h3}(\varphi_N)}{V_c} \quad (5)$$

$$\delta_{cn}(\varphi_N) = 1 + \frac{v_{neg}(\varphi_N) - v_{h3}(\varphi_N)}{V_c} \quad (6)$$

These functions are applying for an ideal consideration of $L_{cp}$ and $L_{cn}$. If $\delta_{cp}$ is now drawn for further investigation, the minimum of the function ($\delta_{cp,min} = 0$) can be found at multiples of $(2k-1)\pi/3$ and the maximum ($\delta_{cp,max} = M = \frac{3\hat{V}_N}{2V_c} = 0.8125$) at multiples of $2k\pi/3$ for $k \in \mathbb{Z}$ (cf., **Fig. 2** - (top) red waveform). For a non-ideal consideration of $L_{cp}$, an additional voltage drop has to be incorporated (depicted in **Fig. 2** - (top) blue waveforms for different values of $L_{cp}$) which results in an adapted minimum of

$$\delta_{cp,min} = -\omega_N L_{cp} \frac{\frac{3\sqrt{3}}{\pi\omega_N L_{DC}}\left(1 - \frac{\pi}{2\sqrt{3}}\right)\hat{V}_N + \frac{\sqrt{3}}{2}\hat{I}_N}{V_c} \quad (7)$$

As $(1 - \frac{\pi}{2\sqrt{3}})$ is $> 0$, $\delta_{cp,min}$ is always $< 0$ for $L_{cp} > 0$. Each half-bridge, however, is only able to facilitate a duty cycle range of $[0 \ldots 1]$, whereas "0" means upper switch ($S_{cp+}$) opened and lower switch ($S_{cp-}$) closed and vice versa. A duty cycle $< 0$ will hence inevitably lead to current distortions of positive and negative busbar currents $i_{pos}$ and $i_{neg}$, which is illustrated in **Fig. 2** (top - calculated duty cycles and bottom - resulting current distortions of $i_{pos}$ for different values of $L_{cp}(f_s)$). It is hence highly preferable to implement an injection choke whose inductance is specified as small as possible which can be achieved due to increased switching frequencies $f_s$ if a specific maximum current ripple of e.g. 30 % of the mains maximum peak current is allowed. According to **Fig. 3**, a $\text{THD}_i < 5\,\%$ can be achieved for a switching frequency of $\approx 30$ kHz. As already discussed in [23] the inductance value of $L_{cp}$ and $L_{cn}$ can be further reduced if a third inductor $L_{h3}$ is used. While the total volume of a three inductor implementation (if three independent chokes are utilized) hardly shrinks, the inductance value of $L_{cp}$ and $L_{cn}$ can be tremendously reduced by $\approx 70\,\%$ which can be expressed by

$$L_{c\,\frac{p}{n},h3} = \chi_L \cdot L_{c\,\frac{p}{n}}, \quad \chi_L = \frac{1}{2\sqrt{3}\left(\sqrt{3} - M\right)}. \quad (8)$$

This reduction mainly results due to the injection cell voltage $v_{MN}$ (characterized by voltage levels 0 and $\pm\frac{V_c}{3}$), which is no longer directly clamped to the AC-side mains which would result in $v_{MN} = v_3$. If the optimized inductors are considered in the design of the injection cell the minimum switching frequency, which is required to guarantee a $\text{THD}_i < 5\,\%$, can hence be improved to values in the range of $\approx 15 - 20$ kHz.
It has however be mentioned, that a proper design of the injection inductors is not the only stringent requirement for proper operation of the injection cell. Imbalance of mains input voltages is also evolving as noticeable issue for this type

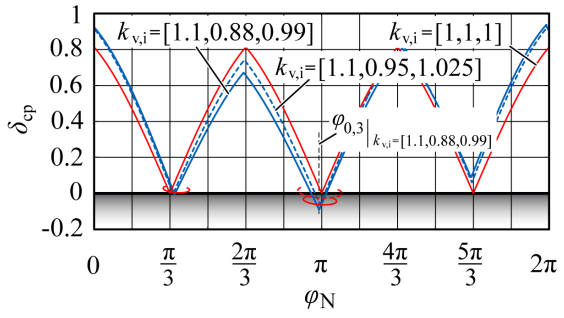



Fig. 4: (Duty cycles $\delta_{cp}$ ($L_{cp}$,$L_{cn}=0$) considering unbalanced (e.g. $k_{v,1}=1.1$ means $V_{N,rms}=230\,V+10\,\%$) mains voltages (red – balanced mains voltages $k_{v,i}=1$).

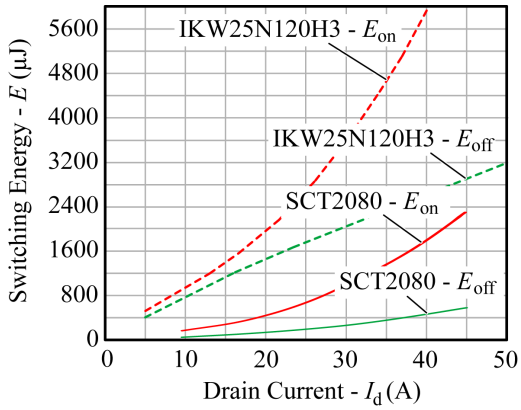



Fig. 5: Comparison of switching losses of an 1200 V/28 A (@100 °C) SiC-MOSFET (SCT2080KE - losses recorded @ 600 V DC voltage, $R_G=0\,\Omega$, $V_{GS}=18/0\,V$, $L=500\,\mu H$) and a 1200 V/25 A (@100 °C) IGBT (IKW25N120H3 (high speed switching series) - losses recorded @ 600 V DC voltage, $R_G=23\,\Omega$, $V_{GS}=15/0\,V$, $L$ =n/a).

of converter stage. For this investigation an ideal duty cycle is assumed, ignoring injection injection chokes ($L_{c\frac{p}{n}}\rightarrow 0$ ($f_s\rightarrow\infty$)). The variable $k_{v,i}$ is going to be introduced which includes the information of relative mains unbalance from the nominal $230\,V_{rms}$ (e.g. $k_{v,1}=1.1$ which results in a mains input voltage of $253\,V_{rms}$ and hence an increase of $10\,\%$). This is, however, directly affecting the duty cycle of both half-bridges ($\delta_{cp}$ and $\delta_{cn}$). The minimum of $\delta_{cp}$ is no longer characterized by 0. Considering the modified commutation time instants of the B6 the minimum of the duty cycle can be approximated by

$$\delta_{cp,min}\left(\varphi_{0,3}\right)\approx\frac{2}{3}M\left(k_{v,2}-k_{v,1}\right) \tag{9}$$

for the sector $\varphi_N\in\left[\varphi_{0,2}\ldots\varphi_{0,3}\right]$ which correlates with the sector $\varphi_N\in\left[\frac{2\pi}{3}\ldots\pi\right]$ for balanced mains voltages ($k_{v,i}=1$, also depicted in **Fig. 4** - red waveform). $\varphi_{0,3}$ is the altered commutation time instant next to $\pi$ and is defined by

$$\varphi_{0,3}=\frac{2\pi}{3}+\arctan\left(\frac{2k_{v2}+k_{v3}}{\sqrt{3}k_{v3}}\right). \tag{10}$$

**Fig. 4** depicts different duty cycles for varying imbalance of mains voltages with $k_v=[1.1,0.88,0.99]$ and $k_v$ =[1.1, 0.95, 1.025]. It can be seen that for the appropriate sector $\varphi_N\in[\varphi_{0,2}\ldots\varphi_{0,3}]$, the minimum duty cycle is of negative value if $k_{v,1}>k_{v,2}$. Again, it should be pointed out that each half-bridge is only able to facilitate a duty cycle between $[0\ldots1]$. Negative duty cycles, hence, lead to increased input current distortions and hence worsened $THD_i$.

### C. SiC-MOSFET or IGBT

The SiC-MOSFET is recently available for blocking voltages $\geq 900\,V$. This allows the implementation of SiC-MOSFETs for half-bridge legs with DC voltage levels $\geq 600\,V$ and offers an operation with increased switching frequency with lower switching losses compared to a conventional IGBT. This is also depicted in **Fig. 5** which shows a comparison of turn-on and turn-off energy losses of a SCT2080KE (SiC-MOSFET) and a IKW25T120H3 (reverse blocking IGBT) with very similar basic characteristics ($V_{max}=1200\,V$, $I_{d,max@100°C}\approx 25\,A-28\,A$). It can be observed that both, turn-on and turn-off switching energies of the SiC-MOSFET are significantly smaller than those of an IGBT. The SiC-MOSFET, furthermore, shows ohmic characteristics which will result in improved conduction losses (compared to an Si-IGBT). The implementation of a SiC-MOSFET hence leads to smaller and less expensive cooling system/volume (if SiC conduction and switching losses are smaller than that of an IGBT). The improved switching loss behaviour will hence lead to an increased efficiency of the total system compared to a conventional IGBT with approximately equal switching frequency. Similar to low-voltage MOSFETs the SiC-MOSFET is characterized by a parasitic body diode due to its physical implementation. As, however, this body diode is only conducting during the adjusted dead time of the half-bridge stage, no external diode is required and the SiC-MOSFET seems to be very well applicable for the chosen topology. The bidirectional switches can also advantageously be implemented by SiC-MOSFETs in order to reduce losses of the current injection stage. It has to be mentioned that the emerging GaN technology could also serve as promising solution for the current shaping network, however, is yet not commercially available for DC voltage levels greater than 650 V.

## III. Current Controller

In this section, current control of the proposed injection cell is briefly discussed. The third harmonic injection circuit consists of two half-bridge legs (cf., **Fig. 1(a)**). The half-bridge connected to $C_{cp}$ is therefore responsible for proper control of $i_{cp}$ and the converter stage linked to $C_{cn}$ has to properly adjust $i_{cn}$, respectively. Thus, two independent current controllers have to be designed.

If a simplified model is applied which is neglecting parasitic effects and components, the basic equations result in

$$\begin{aligned}L_{cp}\frac{di_{cp}}{dt}&=\delta_{cp}v_{cp}+v_{h3}-v_{pos}\\ L_{cn}\frac{di_{cn}}{dt}&=\left(1-\delta_{cn}\right)v_{cn}-v_{h3}+v_{neg}.\end{aligned} \tag{11}$$

If it is now assumed that the two DC voltages ($v_{cp}$ and $v_{cn}$) of the injection cell are regulated such – by the superimposed voltage controller with reduced dynamic – to remain fixed at the same voltage level $V_{cp}=V_{cn}=V_c$, the equations above

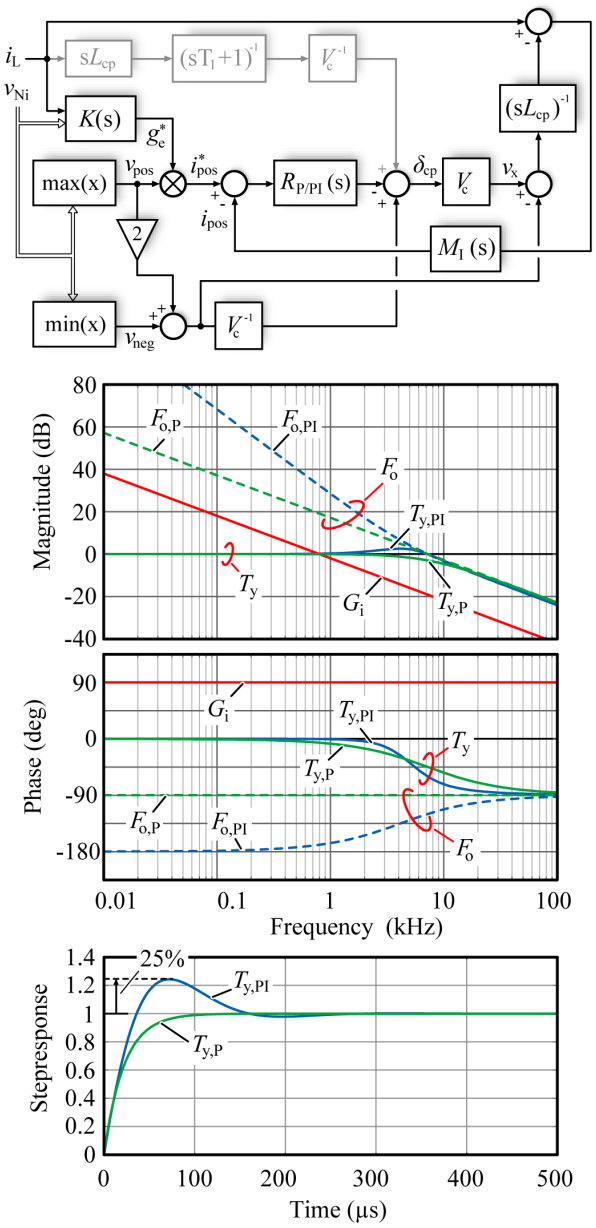



Fig. 6: Basic structure of current control circuit (top). Bode plot (middle) and step-response (bottom) of the designed current controller for a switching frequency of 72 kHz and an inductance value $L_{cp}$ of 200 µH and a gain crossover frequency of 7 kHz), for either P- or PI-type with maximum overshoot of 25 % and minimum phase margin of 60 °).

can be simplified by applying Laplace Transformation which finally results in

$$sL_{cp}i_{pos} = -\delta_{cp}V_c + v_{pos} - v_{h3} + sL_{cp}i_L. \tag{12}$$

If $v_{N1}$, $v_{N2}$, $v_{N3}$ (which are required for the generation of an equivalent conductance value, which represents the power demand of the circuit) and $i_L$ are measured, $v_{pos}$, $v_{h3}$ and $sL_{cp}i_L$ can serve as feedforward signals of the respective current control structure. The hereby resulting model can be described

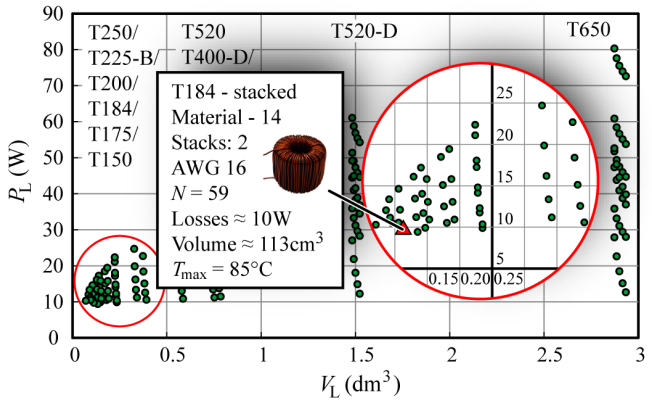



Fig. 7: Evaluation of optimized choke for different toroidal-stacked cores T20-T650, iron powder core materials 14-52 and solid conductors AWG16-AWG20 according to GeckoMAGNETICS and implemented inductor (boxed).

by

$$\delta_{cp} = -\frac{sL_{cp}}{V_c} i_{pos} + \delta_{ff} \tag{13}$$

with the feedforward signal $\delta_{ff}$

$$\delta_{ff} = \frac{1}{V_c}(v_{pos} - v_{h3}) + \frac{sL_{cp}}{(sT_1+1)V_c} i_L. \tag{14}$$

The additional damping part $1/(sT_1+1)$ is required to guarantee suppression of high frequency noise and/or disturbance. Furthermore, it has to be noticed that the feedforward part which includes $i_L$ could also be omitted for very small values of $L_c$ if it is preferred to reduce the number of current sensors. In **Fig. 6** (top) the basic structure of the proposed current controller is depicted. Furthermore, bode plot (middle) and step-response (bottom) of the designed controller is given (for a switching frequency of 72 kHz and an inductance value $L_c$ of 200 µH and a gain crossover frequency $f_c$ of 7 kHz), for either P- or PI-type (maximum overshoot of 25 %, minimum phase margin 60°) implementation. $F_o$ denotes the open loop characteristic and $T_y$ the closed loop transfer function of controlled current $i_{pos}$ which is defined by

$$T_{y,P/PI}(s) = \frac{R_{P/PI}(s)\,G_i(s)}{1 + M_I(s)\,R_{P/PI}(s)\,G_i(s)}. \tag{15}$$

The reference currents are often generated by a superimposed voltage controller. This voltage controller indirectly determines the power demand by measuring the voltage of the dc-link capacitor. However, voltage control of the injection cell DC voltages is not one of the major topics in this paper and hence not further discussed.

## IV. Inductor Design

A stacked toroidal iron powder core (implementation of $L_c = L_{c\frac{p}{n}} = L_{h3}$) finally has been selected which basically allows reduced losses and rather high current saturation limits (compared to ferrite material) which may be necessary due to unbalanced grid voltages and load step behaviour of the total system (discussed in [24] and [25]). In order to minimize input current distortions a maximum inductance of 200 µH has been

TABLE I: Design Specifications of the Built Three-Phase Rectifier.

| | |
|---|---|
| Mains voltage: | $V_{\mathrm{LL}} = 400\,\mathrm{V_{rms}}$ |
| Mains frequency: | $f_{\mathrm{N}} = 50\,\mathrm{Hz}$ |
| Switching frequency: | $f_{\mathrm{s}} = 72\,\mathrm{kHz}$. |
| Cells DC-link voltage: | $V_{\mathrm{cp}} = V_{\mathrm{cn}} = 600\,\mathrm{V}$ |
| Output power: | $P_{\mathrm{o}} = 10\,\mathrm{kW}$ |

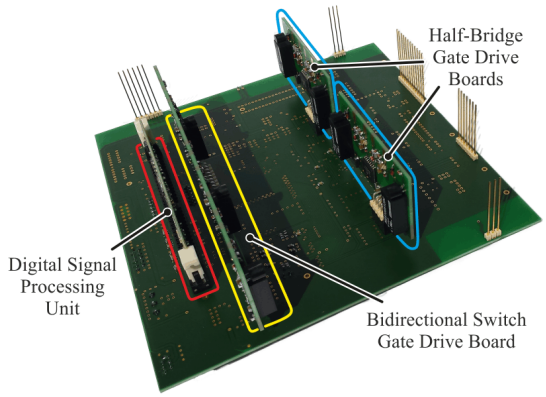



Fig. 8: Controlboard (bottom view) with plug-in DSP board (red), half-bridge gate drive boards (blue) and bidirectional switch boards (yellow).

chosen. Design guidelines for injection inductance values are listed in [23]. The number of turns $N$ for one choke can be calculated by

$$N = \sqrt{\frac{V_{\mathrm{c}} M}{3\sqrt{3} f_{\mathrm{s}} k_{\mathrm{i}} \Delta i_{\mathrm{N,max}} A_{\mathrm{L,2xT184}}}} \tag{16}$$

where $V_{\mathrm{c}}$ denotes the DC voltage of the cell (600 V), $M$ the modulation index (0.8125) and $A_{\mathrm{L,2xT184}}$ the core nominal inductance ($2 \cdot 28\,\mathrm{nH}$). It has to be noted that the basic equation to evaluate the required number of turns is given according to

$$L_{\mathrm{c}} = N^2 \cdot A_{\mathrm{L}}. \tag{17}$$

**Fig. 7** illustrates an inductor optimization which was performed with GeckoMAGNETICS for different toroidal-stacked cores T20-T650, iron powder core materials 14-52 and solid conductors AWG16-AWG20. The red triangle marks the implemented choke which is depicted in **Fig. 7**.

## V. Experimental Results

A 10 kW/72 kHz laboratory prototype was implemented in order to verify proper operation of the proposed circuit. Design specifications of the built three-phase rectifier are given in TABLE I and TABLE II. The system should be constructed for $400\,\mathrm{V_{LL}}/50\,\mathrm{Hz}$ mains voltages, which results in 600 V DC voltage levels (if the modulation index $M = 0.8125$) for the injection cell capacitors $C_{\mathrm{cp}}$ and $C_{\mathrm{cn}}$.

ROHMs SCT2080KE SiC-MOSFETs are used for implementing the active switches of the half-bridges connected to $C_{\mathrm{cp}}$ and $C_{\mathrm{cn}}$. The bidirectional switches $S_{\mathrm{i,ab}}$ are operating in back-to-back arrangement using IKW40T120 IGBTs. It has to be noted that also 1200 V or 900 V SiC-MOSFETs would be applicable and could further reduce losses of the injection

TABLE II: Power Devices Selected for Implementation of the passive rectifier and Third Harmonic Injection Cell.

| | |
|---|---|
| $S_{\mathrm{ia,b}}$ | 1200 V/40 A IGBT, IKW40T120, Infineon |
| $S_{\mathrm{c}\,\frac{\mathrm{p}}{\mathrm{n}}\,\pm}$ | 600 V/20 A SiC-MOSFET, SCT2080, ROHM |
| $C_{\mathrm{c}\,\frac{\mathrm{p}}{\mathrm{n}}}$ | 220 $\mu$F/400 V, EPCOS B43508-type |
| $L_{\mathrm{cp}}$=$L_{\mathrm{cn}}$=$L_{\mathrm{h3}}$ | Iron Powder Core 2 x T184-14, N = 59 turns 200 µH |
| $C_{\mathrm{F}}$, $C_{\mathrm{S}}$ | 1 $\mu$F/275 $\mathrm{V_{AC}}$, MKP X2, Arcotronics |
| $C_{\mathrm{o}}$ | 2.2 mF/400 V, Felsic CO 39 A728848 |
| $L_{\mathrm{DC}}$ | 2.25 mH, Iron core 2 x UI60a |
| $D_1 - D_6$ | 35 A/1600 V, 36MT160, Vishay |

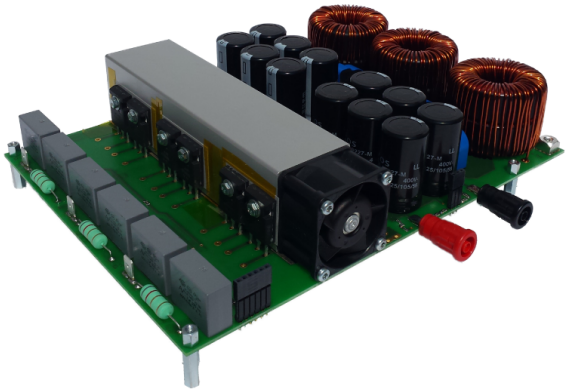


Fig. 9: Powerboard consisting of current sensors, inductors, half-bridge stage, bidirectional switches and input filter.

device by $\approx$ 30 %, which is however only $2 - 3\,\%$ of the total system losses, which does not outweigh the unfavorable additional expense of increasing cost per active component.

The passive three-phase rectifier has to be configured such to allow a maximum total harmonic distortion of input currents of approximately 45 % at nominal load (10 kW) (B6-$\mathrm{THD_i}$ - standalone operation). The required DC-side smoothing inductance ($L_{\mathrm{DC}}$) therefore results in 2.25 mH. As no high-frequency common mode at the output of the system is expected a relatively large output capacitor of 2x2.2 mF in series is chosen.

The current injection laboratory prototype mainly consists of two different boards – controller- and power board. The controller board (cf., **Fig. 8**) contains measurement circuits, auxiliary power supply, DSP control unit (TI 320F2808), additional hardware as e.g. zero crossing detection of mains line-to-line voltages and bidirectional switch controller (Lattice CPLD - MachXO 2280). Except for the digital signal processor (which is located at the bottom of the control board) all remaining parts are mainly placed top-side of the board. Gate drives of SiC-MOSFETs and IGBTs are spotted on separate plug-in boards (one board for each half-bridge stage and one additional board for bidirectional switches $S_{\mathrm{i,ab}}$). The circuits are located in between control and power board in order to minimize the total volume of the cell and reduce parasitic inductance between gate drive circuit, appropriate switches and DC-link electrolytic capacitor bank ($C_{\mathrm{cp}}$ and $C_{\mathrm{cn}}$). The power board, which is depicted in **Fig. 9**, includes main power components as forced

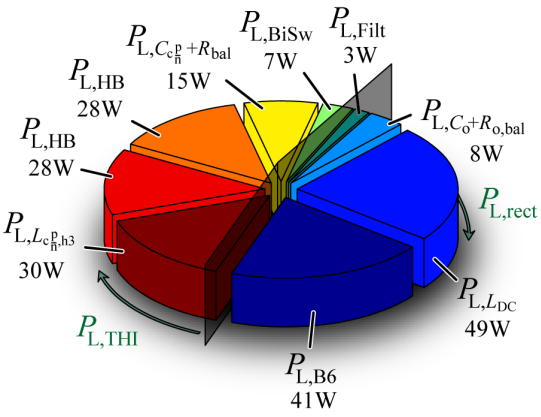



Fig. 10: Losses of the three-phase rectifier system for $230\,\mathrm{V_{rms}}/50\,\mathrm{Hz}$ a switching frequency of 72 kHz and 10 kW output power. (a) Apportioned losses by stage and/or passive components. (b) Pie chart which illustrates loss-distribution of passive system and active upgrade.

convection cooling system, IGBTs, SiC-MOSFETs, input filter, current sensors, inductors, electrolytic capacitors and additional hardware which is required for start-up operation of the system. Calculated system losses at nominal load ($P_{\mathrm{N}} = 10\,\mathrm{kW}$) are depicted in **Fig. 10**. As can be seen, the highest losses of all included parts are drawn by the DC-side choke ($\approx 50\,\mathrm{W}$) and the passive three-phase rectifier ($\approx 40\,\mathrm{W}$), which have to transfer the main part of the active power. The injection cell only has to process $\approx 6\,\%P_{\mathrm{o}}$ which obviously results in very low losses of the optional configuration related to the nominal power $P_{\mathrm{N}}$. As can be seen in **Fig. 10**, losses are evenly distributed over both circuits (passive circuit/active circuit - $\approx 50\,\%/50\,\%$, respectively). The total system losses are therefore, calculated to 209 W which results in an expected system efficiency $\eta_{\mathrm{calc}}$ of 97.95 %.

The performed loss calculation, allows the design of the forced convection (air) cooling system. The chosen air cooled heatsink should serve as loss dissipating surface for SiC-MOSFETs (half-bridges) and IGBTs (bidirectional switches). According to [26] a cooling system performance index (CSPI)

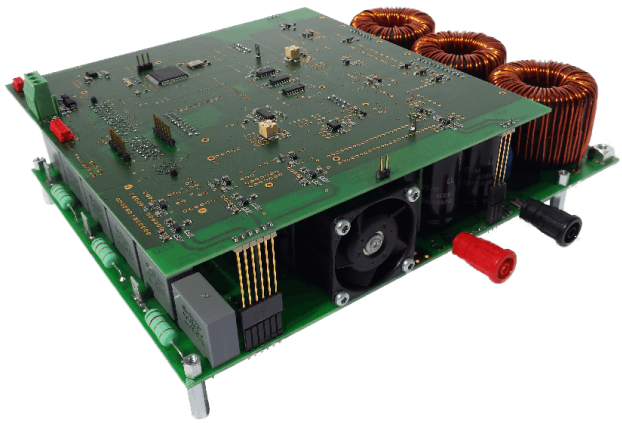
$$\mathrm{CSPI} = \frac{1}{R_{\mathrm{th,hs}} V_{\mathrm{hs}}} \tag{18}$$

has been introduced in order to generally allow a comparison of different cooling system technologies. A forced convection air cooled heatsink typically results in a CSPI between $5 - 12\,\frac{\mathrm{W}}{\mathrm{K\cdot dm^3}}$. The CSPI of the chosen LAM4K (150 mm) air cooled system, as depicted in **Fig. 9**, has been evaluated to $9\,\frac{\mathrm{W}}{\mathrm{K\cdot dm^3}}$. Considering active switch component losses as illustrated in **Fig. 10**, the maximum heatsink temperature $T_{\mathrm{hs}}$ results in

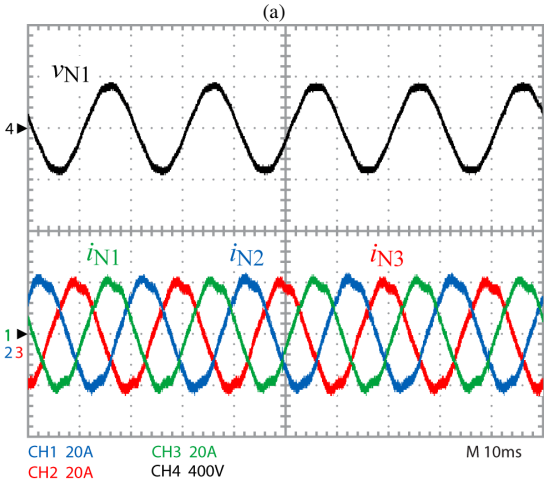
$$T_{\mathrm{hs}} = T_{\mathrm{amb}} + \frac{P_{\mathrm{sys}}\left(\eta_{\mathrm{HB+BiSw}}^{-1} - 1\right)}{V_{\mathrm{hs}} \cdot \mathrm{CSPI}} \approx 54^{\circ}\mathrm{C}. \tag{19}$$

Therefore, the cooling system would still allow an additional decrease of volume for the given active rectifier topology.

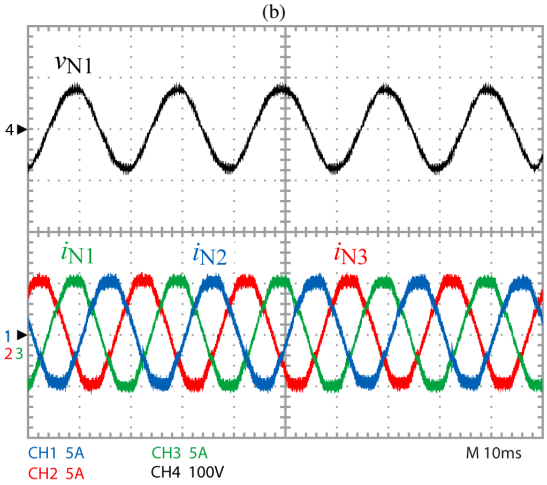
The fully assembled prototype (controller board, power board and gate drive boards) is shown in **Fig. 11(a)**. Measurement



(a)




(b)




(c)

Fig. 11: (a) Assembled 10 kW laboratory prototype. (b) Mains currents $i_{\mathrm{N1}}$ - $i_{\mathrm{N3}}$ and mains voltage $v_{\mathrm{N1}}$ for $400\,\mathrm{V_{LL,rms}}$ input voltage with implemented P-type controller without feedforward currents results in $\mathrm{THD_i} = 3.6\,\%$ and $\lambda = 0.999$. (b) Mains currents $i_{\mathrm{N1}}$ - $i_{\mathrm{N3}}$ and mains voltage $v_{\mathrm{N1}}$ for $95\,\mathrm{V_{LL,rms}}$ input voltage with implemented PI-type controller without feedforward currents results in $\mathrm{THD_i} = 1.8\,\%$, $\lambda = 0.999$.

results of the $10\,\mathrm{kW}/72\,\mathrm{kHz}$ laboratory prototype are depicted in **Fig. 11(b)** and **Fig. 11(c)**. **Fig. 11(b)** shows input currents $i_{\mathrm{N1}}$ - $i_{\mathrm{N3}}$ and mains voltage $v_{\mathrm{N1}}$ for $230\,\mathrm{V_{LL,rms}}$ input voltage

with an implemented P-type controller without feedforward currents $i_{\mathrm{L}}$ and $i_{\mathrm{h3}}$. Nevertheless, input current distortions of $\mathrm{THD_i} = 3.9\,\%$ could be observed. The power factor $\lambda$ was measured by 0.999 . Furthermore, a system efficiency $\eta_{\mathrm{meas}}$ of $97.7\,\%$ has been measured. Heatsink temperature after 20 min of operation at $10\,\mathrm{kW}$ has resulted in $56\,^{\circ}\mathrm{C}$ and injection choke inductance temperature of $87\,^{\circ}\mathrm{C}$ has been measured.
In order to, verify if input current waveforms could be further improved (by utilizing a PI-type controller) a PI-type controller has been implemented for test purpose for $55\,\mathrm{V_{LL,rms}}$ mains voltages (cf., **Fig. 11(c)**) and resulted in a $\mathrm{THD_i} = 1.8\,\%$. Therefore, a PI controller should also be considered and implemented for $230\,\mathrm{V_{LL,rms}}$ mains to improve $\mathrm{THD_i}$ of mains currents.

## VI. Conclusion

Upgrading a simple three-phase passive rectifier by an optional cell (employing two half-bridge stages) based on the third harmonic injection principle has been basically discussed and analyzed in this work. Drawbacks (sensitive to unbalanced mains voltages, minimum switching frequency required etc.) and advantages (optional upgrade, no high-frequency CM voltage, low harmonic input currents, high power factor, improved efficiency, etc.) are mentioned, illustrated and demonstrated by an implemented 10 kW/72 kHz laboratory prototype. It is shown, that due to the implementation of a simple P-type controller and neglecting feedforward currents $i_{\mathrm{L}}$ and $i_{\mathrm{h3}}$, a $\mathrm{THD_i}$ of $< 4\,\%$ can be achieved (values $< 2\,\%$ can be expected if a PI-type controller is implemented). A power factor $\lambda$ of 0.999 could be observed, and despite an applied switching frequency of 72 kHz, an efficiency of the total system (B6 + injection cell) close to $98\,\%$ ($\eta_{\mathrm{meas}} = 97.7\,\%$) could be measured, which is very well fitting with performed loss calculations.

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