Reducing dv/dt of Motor Inverters by Staggered-Edge Switching of Multiple Parallel SiC Half-Bridge Cells

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Abstract

A novel concept for reducing the output voltage dv/dt of PWM inverters (especially for traction motor applications) is proposed which however keeps high semiconductor switching speed resulting in low switching losses. Each phase of the intended converter is formed by a parallel arrangement of half-bridge legs which are PWM operated such that a small time-delay is given between the legs (time staggered switching). The output voltages of the legs subsequently are combined by an interphase transformer/inductor network/device to a total output voltage of staircase-type switching edge behavior which finally leads to a much lower dv/dt at the motor terminals despite high-speed semiconductor switching. The paper describes the basic principle and application variants, the dimensioning and the required current balancing. Finally, measurements taken from a laboratory testing setup are presented.

1. Introduction

SiC-MOSFETs frequently are proposed today as future standard switching device at higher voltage levels, especially also for drive converters due to their in comparison to today's IGBTs much lower switching losses. Furthermore, the ohmic on-state characteristic of these wide-bandgap semiconductors additionally may reduce on-state losses at partial load operation [1]. SiC-MOSFETs therefore seem to be very attractive for high-efficiency drives, in a long-term run even for railway traction main power converters.

It has to be kept in mind, however, that the low switching losses are achieved by very high switching speed resulting in dv/dt rates and overvoltages at the motor terminals which may reduce the lifetime or even damage the machine's isolation system [2], [3].

A second problem region of SiC-MOSFETs is the fact that the possibility for implementing large power modules (for high-power drives commonly many of parallel connected IGBT chips are used) by simply replacing the IGBT chips of the module by SiC devices seems to be difficult. The high di/dt-rates of SiC in any case would require a new module design with improved wiring system to minimize the switching overvoltages by reducing the commutation loop A_Z (Fig.1), [4], [5]. The wiring inductance L_{σ} of today's standard module packages would require a lowering of the SiC switching speed via the gate driver, which would be possible in principle but contradicts the attractiveness of the SiC-MOSFET.



Fig.1: Structure of a switching leg. The area A_Z causes the parasitic inductance in the commutation loop.



Fig.2: Basic concept of the proposed implementation (shown: Split-up of a switching-leg into four half-bridge cells connected in parallel with three interphase transformers combining the individual output voltages).



Fig.3: Output voltages of the half-bridge cells and the combined voltage at the output of the converter for one possible switching sequence.

To overcome the mentioned problems this paper proposes a concept where (i) a single highcurrent switching leg is split-up into several individual half-bridge cells with small "local" DClink capacitors for minimizing the cell's A_Z and (ii) operating the cells in "staggered-edge" PWM, i.e., gating the cells with a standard PWM but implementing small time shifts T_d between the individual cells (Fig.2, showing a system of n = 4cells with driver signals $s_a \dots s_d$). The cells now show slightly time-different output voltages u_a ... u_d which are summed-up by a "combiner tree" of small interphase transformers to $u_A = \sum u_i / n$ (cf. Fig.3). This finally leads to a staircase-shaped converter output voltage u_A characterized by a dv/dt reduction of the SiC switch (in the idealized case, i.e. $T_d \approx t_r$) to a value of dv/dt/n. E.g., a SiC-dv/dt of 20kV/ μ s ($t_r = 50$ ns at a DC link voltage of $U_Z = 1 \text{ kV}$) is reduced to 5kV/µs (being typical of today's IGBT traction inverters) by a split-up into n = 4 branches. The combiner (if implemented as "tree" of n-1 interphase transformers) has to be designed only regarding rather small voltage-second products of about $T_d \cdot U_Z$.

<u>Remark</u>: The proposed time-staggered switching must not be mixed up with conventional interleaved PWM where *n* branches are gated with a delay of T_P/n ($T_P=1/f_P$...converter switching period) leading finally to a multi-level phase output voltage showing an effective pulse frequency of *n*·*f*_P. This indeed would give a better output voltage quality but would also require a for drives usually not acceptable large combining device due to the much larger time-voltage area product. On contrary, the time-staggered switching can be interpreted as a kind of "edge-filter" reducing the dv/dt at the motor terminals but still using the



Fig.4: Voltages across the interphase transformers for the switching sequence shown in Fig.3.

motor's stray inductance for current smoothing. As a disadvantage of the proposed concept it may be seen that n gate drivers and also current sensors are required which today however could be implemented at low effort using gate-driver and sensor ICs favorably directly included into the power module. The individual drivers however open the possibility for active current balancing, i.e., that the total load current i_A is distributed equally to the n branches in a controlled manner as will be addressed also in the following section.

2. Basic Operation

For clarifying the relationships and the dimensioning of the combiner network a basic arrangement of two cells shall be analyzed briefly first. The two bridge-legs a, b (Fig.5a) are gated timeshifted by T_d and their output voltages u_a , u_b combined by an interphase transformer (Fig.5b) to $u_x = (u_a + u_b)/2$ showing three-level stair-case shape. The voltage difference u_{ab} (i.e. U_Z for time interval T_d) appearing at the transformer coil leads to a magnetic excitation $\Delta B = T_d U_Z / (N \cdot A)$ and hence defines the transformer's core dimensioning. To give a numeric example: For a DC link voltage U_Z =600V and T_d =100ns a N·Aproduct 600mm² is required (e.g., N=2x6 turns at A=50 mm²) for $\Delta B = 100$ mT as being typical for pulse transformer materials (ferrite or also for standard SiFe steel cores).

In the ideal case the load current I distributes equally to both legs (assuming equal on-state characteristic of the legs) and the DC components will mutually cancel such that no residual DC induction remains (as this is the case in standard common-mode chokes). If the bridge-



Fig.5: Basic cell for time-staggered switching (a); combiner choke (interphase transformer) (b); basic switching operation (c); switching sequence for balancing mode $u_{ab} > 0$ (d); sequence for balancing mode $u_{ab} < 0$ (e).

legs are gated according to Fig.5c (u_b simply is delayed by T_d vs. u_a) the u_{ab} pulse at the rising and falling PWM edge shows opposite direction resulting in a zero average, giving only AC induction in the core. In a practical system however, due to timing errors and on-state characteristic differences i_a and i_b will not be perfectly balanced but result in an "offset" current $i_0 = i_a - i_a$ i_b . The combiner core therefore has to be equipped with an air gap d (or, alternatively using a low- μ_r -material) to avoid saturation as a consequence of the offset induction $B_0 = \mu_0 \cdot N/(2d) \cdot i_0$. The mentioned coil with N=2x6 and an airgap of d=0.1mm Bo results to ≈ 75 mT/A. Considering a $B_{sat} \approx 300 \text{mT}$ (ferrite core) and an AC amplitude of $\Delta B = 100 \mathrm{mT}$ a maximum offset current of $i_O <$ 200 mT/75 mT/A = 2.7 A (i.e. $i_a = 11.35 \text{A}$, $i_b = 8.65 \text{A}$ for I = 20A). A larger airgap d would reduce the offset induction but also the core's inductance and hence would increase the current ripple ΔI of i_a , i_b originated by the $U_Z \cdot T_d$ product (here ΔI calculates to $\Delta I = \frac{1}{2} 100 \text{ mT} / (75 \text{ mT/A}) = 0.67 \text{ A}).$

Active Current Balancing. The system in principle shows an intrinsic self-balancing behavior due to the $R_{DS,on}$ of the MOSFETs. For converters at higher power level however this feature is not effective such that current imbalances due to PWM timing errors are limited adequate. Therefore, an active leg current balancing is required, using PWM patterns of Fig.5d or Fig.5e. These patterns (although generating branch output voltages u_x being identically to Fig.5c) lead to a positive/ negative u_{ab} average altering the current distribution within the bridge legs. Most simply an active balancing can be implemented using a comparator detecting the sign of $i_a - i_b$ which is used as a decision if pattern (d) or (e) is applied for the next PWM cycle by sampling the comparator's output signal briefly prior to each PWM transition (Fig.6, top). Simulation results (Fig.6, bottom) demonstrate good balancing behavior for i_a , i_b avoiding core saturation even for this simple ("two-level", because only switching pattern (d) or (e) are used) strategy. Considering further also the basic switching pattern status (c) an improved "three-level" balancing will be possible. The simple two- or three-level comparator-based balancing



Fig.6: Control scheme (top) and simulation results (bottom) for simple active current balancing. PWM and balancing are activated at $t=25\mu s$. Initially i_a , i_b are not balanced due to different $R_{DS,on}$ (100m Ω /66m Ω) of the two legs. Within a few PWM cycles (here $T_P=10\mu s$ is used for demonstration purposes) however $i_a \approx i_b \approx I/2$ is attained. For testing the control behaviour, at $t = 250\mu s$ a severe disturbance is activated by raising $R_{DS,on}$ of leg *b* from 66m Ω to 366m Ω . Nevertheless, the partial currents are still balanced by the control.



Fig.7: Combiner voltages for a full PWM cycle. All variants shown here result in zero transformer average voltage (balanced case) but are characterized by different core dimensioning (different individual time-voltage area products).



can be extended also for systems consisting of $n=4,8,16,\ldots$ bridge legs as mentioned in the next section.

3. Four-Leg Arrangement

After clarification of the basic principle the initially intended four-leg topology (Figs.2-4) is analyzed. Basically it is possible to use two 2-leg stages of Fig.5a (ab, cd), shift the 2nd 2-leg stage cd by 2 T_d and combine the two stages ab and cd by a 3rd interphase transformer to the final output voltage u_A . It is also possible to use the balancing principle discussed in the previous section again, i.e., two individual controllers which balance ab resp. cd, and a 3rd controller balancing the final interphase transformer by exchanging the gating signals for ab and cd. Such an operation mode (Fig.7a, sequence abcd) however does not utilize all degrees of freedom which are possible in a four-leg system. If, alternatively, leg a is switched



Fig.8: left: possible 16 switching states of a 4leg system and corresponding differences ab, cd, xy; middle: states, according voltage level of u_A and possible transition paths; 24 transition paths, state sequence and net voltage differentials Σab , Σcd & Σxy (see also text).

and after $T_d \log c$ and further b and finally d (i.e., Fig.7b, acbd) an identical u_A is generated, the voltages across the coils of the interphase transformers (and also their time-area products) however are different. A third possibility is shown in Fig.7c, sequence acdb. All PWM sequences depicted in Fig.7 are characterized by a zero average of u_{ab} , u_{cd} , u_{xy} within a full pulse period T_P . Consequently, they are non-balancing states (i.e., states which do not alter the current distribution) which, however result in different dimensioning of the 2+1 interphase transformers (Fig.7a, e.g., shows a twice as high voltage-time area product for the final transformer xy vs. the first transformers *ab*, *cd* whereas Fig.7b gives the opposite case) finally causing different transformer sizes.

Concerning balancing issues a more detailed analysis shows, that in principle there are 2^4 =16 possible switch positions for a 4-leg system (0000/0 to 1111/15, Fig.8). A low-to-high transition of the whole phase starts at 0 ($u_A = 0$) and ends in 15 ($u_A = U_Z$) running through the intermediate levels $u_A = \frac{1}{4}U_Z$, $\frac{1}{2}U_Z$ and $\frac{3}{4}U_Z$, which all can be generated via redundant states ($\frac{1}{4}U_Z$ by 1,2,4,8; $\frac{1}{2}U_Z$ by 3,5,9,6,10,12; $\frac{3}{4}U_Z$ by 7,11,13,14). These redundant states now show different voltage levels 0, $\pm U_Z$ for u_{ab} , u_{cd} and 0, $\pm \frac{1}{2}U_Z$, $\pm U_Z$ for u_{xy} , appearing at the interphase transformers (Fig.8, left). As indicated also in Fig.8 there are 4!=24 possible path sequences leading from 0 to 15 generating equal u_A staircase shape but resulting in different net (average) voltage sums Σu_{ab} , Σu_{cd} , Σu_{xy} across the three interphase transformers which can be used for enhanced current balancing.

In Fig.7a the basic of the multiple possibilities is depicted (generated by simply time-shifting of the individual driver signals s_a , s_b , s_c , s_d by T_d) leading to the sequence 0-1-3-7-15 for rising PWM edge and 15-14-12-8-0 for falling edge. Other sequences, however are characterized by pulses of different voltage-time area and therefore will lead to small positive or negative DC components of u_{ab} , u_{cd} , u_{xy} which can be used to compensate onstate voltage and switching delay differences of the four legs and guaranteeing that the total load current i_A is equally distributed to the legs using an adequate/optimized balancing control scheme. This can be performed in a practical system by a logic control unit considering the individual leg output currents $i_a...i_d$, e.g. by an algorithm sorting the sequence of driving signals for each PWM main cycle as indicated in Fig.9 utilizing a logic device like a fast micro processor or an FPGA.



Fig.9: Schematic of balancing current control employing employing a digital PWM sequencer.

4. Experimental Verification

Although time-staggered switching mainly seems to be attractive especially for future high-power traction converters, the principle shall be tested first using today's standard SiC-MOSFETs. The four-leg system described in section 3 is implemented as a laboratory prototype utilizing 4x2 of



Fig.10: Laboratory prototype converter (4-leg typ).

Cree's C2M0160120D devices $(1200V/160m\Omega/19A)$ using internal body diode for free-wheeling.

The gate drivers are implemented employing Si8261 isolated driver with dedicated 1W-DC/DC converters for power supply. For the three combiner chokes EFD25/13/9 N87 cores are used with 2x10 turns CuLa \emptyset 1mm for the *ab/cd* transformers and 2x6 turns, Ø1.25mm for xy transformer, both with an air gap of 0.1mm (similar as described in section 2). The four leg currents are sensed individually by Allegro ACS710 integrated Hall effect transducers. The circuit is tested as a buck converter operated at a fixed duty cycle and a DC link voltage of $U_Z = 600$ V to currents up to $i_A \approx 40$ A. The PWM signal s(t) is defined by an external function generator, a micro processor (TI TM4C1294) is used as a PWM sequencer creating a fixed time shift interval $T_d=100$ ns for the four legs including also balancing by leg current measurement as shown in Fig.9. It could however be observed that the circuit already shows good "intrinsic" current balancing behavior due to precise basic PWM timing, low and matched driver delay and the ohmic (not very pronounced and positive temperature dependent) on-state characteristic of the SiC-MOSFETs.

On the other hand with active current balancing still minor current imbalances have to be observed resulting from the offset of the used low-cost current sensors. For higher power systems it seems to be of advantage to use differential current sensors of higher sensitivity to determine i_{a-b} , i_{c-d} , $i_{x\cdoty}$, measure the total current i_A and perform a subsequent back-calculation of $i_a...i_d$.



Fig.11: Output voltage transients of two SiC-MOSFET bridge legs (red: leg a, blue: leg b) at U_Z =600V, $dv/dt \approx 20 kV/\mu s$ and at the load (green, $\approx 1.5 kV/\mu s$).

Measurement Results. Whereas the SiC-legs show a dv/dt rate of ≈20kV/µs for the used configuration ($U_Z = 600$ V, $R_G = 10/5\Omega$, cf. Fig.11, red and blue trace), the dv/dt of the voltage at the RLload (Fig.11, green trace) is much lower and only about 1.5kV/µs and does not show a stair-case shape as expected from $u_A = \frac{1}{4}(u_a + u_b + u_c + u_d)$. The reason for this additional feature is that the stray inductances of the interphase transformer network (in total L_{σ}) in connection with the capacitance C of the cable to the load acts as a kind of LC filter. This lowpass filter characteristic smoothes the idealized u_A but results also in some ringing and voltage overshoot (being however of lower amplitude compared to the SiC-switch itself, see Fig.11 top, $\Delta u_A \approx 50$ Vs. $\Delta u_{SiC} \approx 100$ V).

Filter considerations. In general it has to be noted that the basic idea of the concept is that *n* switching legs of rise-time t_r are individually timeshifted by $T_d \approx t_r$ and summed up by a combiner network to a total output voltage u_A showing a dv/dt rate of 1/n in comparison to the bridge leg. With a system of n=8 legs a dv/dt reduction to a level of today's traction IGBTs (typ <5kV/µs) can be achieved for SiC-MOSFETs running at 30... 40kV/µs. The combiner network in the ideal case shows zero output impedance ($L_{\sigma} \rightarrow 0$). In real



Fig.12: Equivalent circuit (left) and u_C/i_C -state space diagram of an idealized four-leg system.

systems, however, frequently lower numbers of legs are desired (to limit the driver effort) and the non-zero output impedance of the combiner has to be considered or even used intentionally. For a system of n=4, $T_d >> t_r$ is common, i.e. the combiner output voltage u_A is of staircase-type but shaped by it's L_{σ} in connection with the load/ cable capacitance C (Fig.12). By proper dimensioning of L_{σ} (which can be influenced by the winding arrangement of the interphase transformers) and C (which can be increased by additionnal capacitors in parallel to the load cable) the resonance system can be tuned such, that a uc/ictrajectory results showing three 90° arcs for $T_d =$ $\pi/2\sqrt{(L_{\sigma}C)}$ (cf. Fig.12, right, e.g. $L_{\sigma}=2\mu$ H, C=2nF, $T_d=100$ ns, $i_{C,pk} = U_Z/(2\sqrt{2Z_0}) = 6.7$ A for $U_Z = 600$ V). With this the load voltage u_C will get a smooth quasi-sinusoidal S-shape showing a maximum dv/dt of $i_{C,pk}$ /C = 6.7A/2nF=3.75kV/µs here.

5. Conclusion – Outlook

The results of the first tests confirm that the proposed time-staggered switching is an attractive principle for making future high-speed semiconductor switching devices compatible to standard loads. In especial the principle is interesting for traction motors which would show severe lifetime/ reliability issues if they are fed by voltages with a dv/dt of 10...40kV/µs as being typical for SiC-MOSFETs. In addition the concept further reduces the EMI issues of the drive system compatible to a level of today's IGBT converters. A further advantage is that a controlled equalized distribution of high load currents to individual bridge-legs can be achieved. The higher effort in gate drive, current measurement and required interphase transformer devices may be seen as a drawback which however seems to be acceptable for practical systems from the point of view of the advantages, in particular if highly integrated driver and sensor circuits are used.

To conclude the paper a brief outlook to additional topologies shall be given which can be derived from the circuits discussed so far. It is,



Fig.13: Two-leg converter branch; (a) circuit diagram; (b) switching leg voltages u_a , u_b and output/load voltage u_c and (c) u_c/i_c -state space diagram.

e.g. possible to reduce the 4-leg resonance system of Fig.12 to its fundamental structure. Whereas the basic topology principle (Fig.2) is all the more advantageous, the more parallel cells nare used because the MOSFET dv/dt is reduced by the factor of n without any additional filtering, converter designers alternatively also may prefer a parallel arrangement of only 2...3 legs using commercially available standard high-current power modules (like, e.g., Cree CAS300M17BM2, 1700V/225A). Such a system (Fig.13, n=2) ideally shows a three-level characteristic for u_A (Fig.13b) and similar to Fig.12 again a LC output filter is required to shape the motor/load voltage. On contrary to the 4-leg system where the uc/ictrajectory shows three 90° arcs and three centre points ($\frac{1}{4}U_Z$, $\frac{1}{2}U_Z$, $\frac{3}{4}U_Z$, Fig.12, right), the 0-to- U_Z transition now is performed in a single 180° arc around $\frac{1}{2}U_Z$ (Fig.13c), i.e. a smooth cosineshape of load/motor voltage u_{C} . The maximum motor dv/dt calculates to $U_Z/(2\sqrt{L_{\sigma}C})$). Assuming Uz=1000V (1.7kV SiC-module), a cable/output capacitance of C = 2nF and $L_{\sigma} = 5\mu H (dv/dt)_{max}$ of u_C gets 5kV/µs, which can be tolerated for most motors. The delay between leg a and b has to be adjusted to $T_d = \pi \sqrt{(L_{\sigma}C)} = \pi/2 \cdot U_Z/(dv/dt) =$ 314ns resulting in a higher core area product of the (single) interphase transformer as compared to the 4-leg system.

Remarks: (1): The stray inductance L_{σ} of the interphase transformers to a certain extent can be influenced by the winding design, e.g., bifilar



Fig.14: 3-leg converter branch utilizing a single 3-leg magnetic combiner device (cf. also Fig.13c for n=3).

windings for $L_{\sigma} \rightarrow 0$ or on contrary sectional windings if a higher L_{σ} is desired by dimensioning. (2): the LC filter as drawn in Fig.13a basically does not show any damping, hence an additional damping element is required, e.g., a damping resistor $R_D \approx \sqrt{(L_{\sigma}/C)}$ in combination with clamping diodes connected to U_Z and GND to prevent ringing of u_C in case of load current transients. It shall be noted that for the basic cosine edge shaping R_D is non-dissipative. For specific load cases it may however be of advantage to replace the passive diodes by active semiconductor switches (i.e. low-current MOSFETs.

As further topology variants systems are feasible with $n \neq 2^k$ (k = 1,2,3,...) or yet uneven n like n=3 if, e.g., a converter branch is constructed by using three parallel SiC high current power modules (Fig.14). For all these cases the combiner network-tree as discussed so far could not be used. But also for $n=2^k$ the standard combiner tree will be uneconomic for higher values of nbecause n-1 interphase transformers will be required in total (for a 16-leg system e.g. 15 transformers). As an alternative it is possible or of advantage to implement the output voltage combiner by a single *n*-leg magnetic transformer device (Fig.14). For a 3-leg system u_A shows the voltage levels 0, $\frac{1}{3}U_Z$, $\frac{2}{3}U_Z$, U_Z resulting in an u_C/i_C -trajectory consisting of two 120° arcs around the centers $\frac{1}{3}U_Z$, $\frac{2}{3}U_Z$ (see also Fig.13c, n=3) and a tuning rule $T_d = 2\pi/3\sqrt{(L_{\sigma}C)}$ is valid.

The 3-leg combiner is implemented as depicted in Fig.15. Similar to the interphase transformer of Fig.5 it also has to have small air gaps *d* to avoid core saturation in case of minor imbalances of *i*_a, *i*_b, *i*_c. The stray inductance of this combiner can be modeled (or actually influenced if required) by a magnetic bypass/shunt A_0, d_0 and calculated to $L_{\sigma} = \frac{1}{3}\mu_0 N^2 A/(d+3d_0)$ (valid for $A_0=A$, a detailed analysis of the topologies according to Figs.13,14 will be topic of a planned future publication).

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Fig.15: Combiner for converter according to Fig.14 formed by a 3-leg transformer core.

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