Control Loop Design for Closed-Loop Class-D Amplifiers with 4th Order Output Filter

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Abstract

The paper presents a control scheme for a high bandwidth class-D power amplifier with two-stage LC output filter. The amplifier's output voltage is controlled using a simple PI-type controller with added single or double capacitor filter current feedback. With the proposed design principle a well-damped dynamic response of the total system (e.g., Butterworth or Bessel) can be achieved without any additional passive damping, whereas the large-signal frequency response is still defined by the intrinsic cut-off frequencies of the LC filter. The paper reports the control loop design analytically analyzing also the design space of the LC filter, the PI-control and the current feedback parameters. System verification is performed by digital simulation including also load variations. Finally, the principle is tested by implementation of a $1\,\mathrm{kW}/\pm 200\,\mathrm{V}$ laboratory amplifier prototype based on a GaN-MOSFET half-bridge operated at a rather high switching frequency of $200\,\mathrm{kHz}$.

1. Introduction

Class-D power amplifiers today are used in many applications like, e.g. audio power systems, AC power sources for testing power electronic equipment or for experimental research [1]. In general, such amplifiers are implemented using a pulse width modulator (PWM), a switch-mode power stage and a reactance filter to suppress the switching frequency noise. In the simplest case the system is operated in open-loop mode resulting in the fact that the amplifier's frequency response is defined dominantly by the LC output filter characteristic ("intrinsic" frequency response), as a "natural" PWM in the idealized case does not show any phase lag [2]. Open-loop class-D amplifiers (as illustrated in Fig. 1), however, show the drawback that (i) DC link supply voltage fluctuations and ripple, (ii) switching stage timing errors, interlock delay and on-state voltage drops as well as (iii) filter non-idealities result in output voltage distortion. Furthermore, the damping/pole placement of the LC output filter has to be performed by additional dissipative damping paths (e.g. RC- or RL- snubbers) or, alternatively, by an ohmic load (which, however, often is not given in real systems). All disadvantages mentioned can be efficiently reduced, if closed-loop control is applied.

Several control schemes have been proposed for switching amplifiers with a single-stage [3], or a two-stage LC output filter [4]. In this paper, a control concept is proposed based on a simple PI-type controller supported by filter capacitor current feedbacks for a two-stage LC filter. The two-stage LC output filter is used to obtain a high output voltage bandwidth but also achieve sufficient attenuation of the switching frequency harmonics [4].

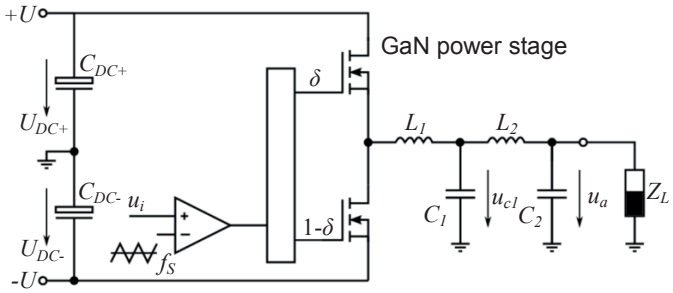

Fig. 1 Basic open-loop class-D amplifier with a two-stage LC output filter.

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Here, a bandwidth of $10\,\mathrm{kHz}$ and a noise level according to EN55011 class-A is aspired. In Section 2, it is illustrated that a specific design procedure finally results in a closed-loop frequency response showing cut-off frequencies being identically to those physically defined by the LC filter, but achieving a well-damped transient behavior like Butterworth or Bessel response actively avoiding any dissipative damping elements. Analyzing the design space of the system, it is further demonstrated that observing some constraints also the feedback of a single filter capacitor current (i_{c1}) is sufficient to achieve the aspired behavior. In Section 3, the proposed dimensioning scheme is verified by simulations and also by a $1\,\mathrm{kW}/\pm 200\,\mathrm{V}$ amplifier prototype based on GaN half-bridge topology operated at a switching frequency of $f_S = 200\ \mathrm{kHz}$.

2. Control Scheme

In this paper, an amplifier with a two-stage LC output filter is considered. In contrast to a single-stage filter, the inclusion of a second filter-stage leads to an increase of the attenuation of high frequency harmonics, without reducing the filter dynamics significantly. The resulting filter resonances are actively damped by filter capacitor current feedbacks (i_{c1} and i_{c2}) as depicted in Fig. 2. Here, the converter power stage block (including "natural PWM") has an assumed transfer function of gain $v = 1$. The feedback gains k_1 and k_2 can be adjusted to obtain a desired behavior of the filter. Without active damping, a single voltage control loop does not achieve sufficient damping of the two filter stages under no load conditions and the filter resonances would have to be damped by additional passive elements.

The transfer function in terms of the output voltage u_a to the converter input voltage u_i can be written as a general system of 4th-order, like

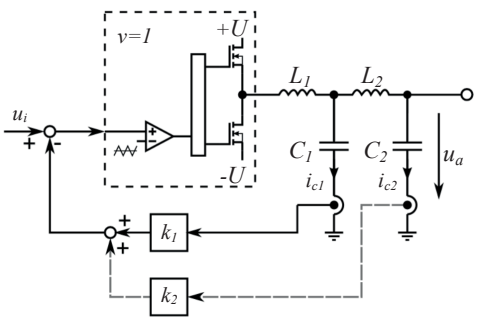

Fig. 2: Active damping concept of the amplifier by feedback of the capacitor currents i_{c1} and i_{c2}.

$$G(s) = \frac{U_a(s)}{U_i(s)} = \frac{1}{as^4 + bs^3 + cs^2 + ds + 1}. \qquad (1)$$

The coefficients a, b, c and d for double capacitor current feedbacks (i_{c1} and i_{c2}) are listed in second column of Table 1.

Despite active damping the system of Fig. 2 still suffers from the distortions mentioned in Section 1. To avoid these disadvantages the system according to Fig. 3 is extended to closed-loop operation by a PI- controller $R(s) = V_I\,(1+sT_I)/s$, resulting in a closed-loop transfer function of

$$T_{ry} = \frac{U_a(s)}{U_a^*(s)} = \frac{R(s)G(s)}{1 + R(s)G(s)} = \frac{1 + sT_I}{a\frac{s^5}{V_I} + b\frac{s^4}{V_I} + c\frac{s^3}{V_I} + d\frac{s^2}{V_I} + (T_I + \frac{1}{V_I})s + 1}, \qquad (2)$$

where V_I and T_I are the controller parameters. Equation (2) now can be rewritten to

$$T_{ry} = \frac{(1 + sT_I)}{\left(A(sT)^4 + B(sT)^3 + C(sT)^2 + D(sT) + 1\right)(1 + sT_I)}. \qquad (3)$$

Allowing the reduction of the term $(1+sT_I)$ we finally receive again a 4th-order roll-of (as defined by the LC filter) also for closed-loop operation. (Remark: Actually the system has five storage elements.) In (3), the time constant T reflects the desired system dynamic and A, B, C and D are the coefficients for Butterworth and Bessel behavior listed in column 3 & 4 of Table 1. A comparison of the denominator coefficients of (2) and (3) by s, yields to

$$a = V_I A T_I T^4, \quad b = V_I (A T^4 + B T^3 T_I),$$
$$c = V_I (B T^3 + C T^2 T_I), \quad d = V_I (C T^2 + D T_I T),$$
$$V_I = 1/(DT). \qquad (4)$$

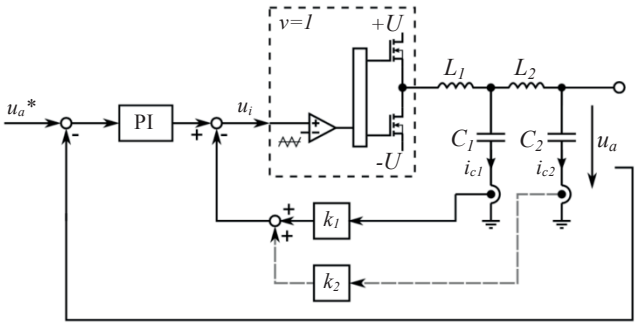

Fig. 3: Proposed closed-loop control concept using a PI-type controller for output voltage control employing additional feedback of the capacitor currents i_{c1} and i_{c2}.

Hence, the proposed control scheme results in an amplifier frequency response showing cut-off frequencies being identically to those physically defined by the LC filter, however, achieving a well damped transient behavior in closed-loop operation. In particular, Butterworth or Bessel response can be achieved for the closed-loop amplifier, avoiding any resistive damping elements. As a consequence, no additional losses of passive damping occur and a limitation of a maximum overshoot of $12\,\%$ for the system at no-load operation is obtained (as will be shown in Fig. 8).

2.1. Design Criterions

The obtained system of equations (4) is now the starting point for further considerations about the design space of a two-stage LC output filter with a double active damping, where the controller and filter parameters have to fulfill the following constraints:

For the amplifier, given specifications of a high bandwidth of the output voltage but also a sufficient attenuation of the switching frequency harmonics should be met. Therefore, the standard for conducted emission levels according to IEC/EN 55011 class-A is considered here, which implicates that in the frequency domain of $150\,\mathrm{kHz}$ to $500\,\mathrm{kHz}$ the output voltage noise has to be lower than $79\,\mathrm{dB\mu V}$.

The suppression of the switching noise is defined by the LC-products of the filter-stages. A second dimensioning issue is given by the characteristic impedances

$$Z_0 = \sqrt{L/C}$$

of the filter stages. The impedance of the first LC stage should be rather high, because L_1 determines the switching current ripple. On the other hand a low Z_0 (i.e. L_2) of the second stage is required to guarantee low voltage drop in case of load current transients. Hence, L_1 has to be selected as a trade-off between current ripple, inductor losses and inductor volume [5]. A low value of L_1 would result in a more compact inductor but also in a high current ripple. Here, it is assumed that the maximum peak-to-peak current ripple is not higher than the effective maximum load current of $I_{N,max} = 5\,\mathrm{A}$. This value was selected as a compromise between inductor size and additional AC losses (coil winding and core as well as MOSFET on-state losses). For a switching frequency of $f_S = 200\,\mathrm{kHz}$ and a DC supply of $U_{DC+} = 200\,\mathrm{V}$ a minimum value of

$$L_{1,\min} = \frac{U_{DC+}\,\delta}{\Delta i_{\max} f_S} = \frac{1}{2}\frac{U_{DC+}}{I_{N,\max} f_S} = 100\mu H\,, \tag{5}$$

is given considering the worst-case duty cycle of $\delta = 1/2$. Selecting $C_1 = 1\,\mu\mathrm{F}$, a first stage cut-off frequency of $16\,\mathrm{kHz}$ results and hence a sufficient bandwidth of at least $10\,\mathrm{kHz}$ for the total system amplifier is feasible.

As a design specification, the second filter-stage inductor is limited to $L_{2,max} \leq L_{1,min}/2$. This value was selected to ensure a small volume of the total amplifier, as well as the desired small output impedance. In a similar way, considering the output voltage dynamics and output impedance of the amplifier, the filter capacitor of the second filter-stage has to be at least in the range of C_1. On the other hand, for limiting the reactive filter capacitor currents at high output frequencies the maximum value of C_2 is defined as $C_{2,max} = 5\,\mu\mathrm{F}$. This specification guarantees a theoretical output voltage with full amplitude at an operating frequency of $3\,\mathrm{kHz}$ without exceeding the maximum allowable transistor currents of the used GaN-MOSFETs (Transphorm TPH3206P/N).

It has to be noted, that the inductance of L_1 also defines the di/dt-rates. Due to the capacitor current feedback damping principle also the switching ripple is fed back to the modulator input (cf. Fig. 3, PWM input voltage u_i) amplified by the feedback gain k_1. This may result in unwanted sli-

Table 1: Parameter values of the closed loop function for single and double active damping scheme without load, as well as the coefficients for Butterworth and Bessel behavior.

Single active damping	Double active damping	Butterworth (4th)	Bessel (4thorder)
$a = C_1C_2L_1L_2$	$a = C_1C_2L_1L_2$	$A = 1$	$A = 0.0095$
$b = C_1C_2L_2k_1$	$b = C_1C_2L_2k_1$	$B = 2.6132$	$B = 0.0952$
$c = C_1L_1+C_2L_1+C_2L_2$	$c = C_1L_1+C_2L_1+C_2L_2$	$C = 3.4143$	$C = 0.4286$
$d = C_1k_1$	$d = C_1k_1+C_2k_2$	$D = 2.6132$	$D = 1$

ding-mode effects of the modulator, i.e., multiple switching instants within one basic PWM cycle $1/f_S$ if the du/dt rate at the P-input of the PWM comparator exceeds the slope of the triangle carrier [6],[7]. The maximum du/dt at the comparator's P-input calculates to

$$\frac{du_i}{dt}\Big|_{\max} = k_1 \frac{di_{c1}}{dt}\Big|_{\max} = k_1 \frac{+U_{DC} - (-U_{DC})}{L_1} = k_1 \frac{2U_{DC}}{L_1},$$

whereas the fixed slew rate of the triangle generator is given by

$$\frac{du_\Delta}{dt} = \frac{2U_{DC}}{T_S/2} = 4U_{DC} f_s .$$

Therefore, to avoid any sliding-mode conditions, $du_\Delta/dt > (k_1\, di_{c1}/dt)|_{max}$ must be valid leading to an upper limit of the feedback gain of

$$k_1 \le 2L_1 f_s = 40\,\mathrm{V/A}. \qquad (6)$$

The output filter design in addition should be implemented regarding minimal volume and losses. In the following, therefore, a design space consideration concerning filter components for an amplifier using a double actively damped LC filter is performed.

2.2. Double Active Damped Amplifier

Here, the control concept of the amplifier is based on the PI-controller and two capacitor current feedback paths k_1, k_2 as illustrated in Fig. 3.

Assuming that C_1 and L_1 are specified in respective to the constraints mentioned above ($100\,\mu H/1\,\mu F$), the system of equations (4) can be solved explicitly for a desired time constant T and a filter inductance L_2. After inserting the parameters according to Table 1, the five unknown parameters of (4), i.e. C_2, k_1, k_2, T_I and V_I can be determined to

$$V_I = \frac{1}{DT}, \qquad T_I = \frac{(BT^2 - C_1 D L_1) C_1 L_1 L_2}{T(AL_1T^2 + AL_2T^2 - C_1 C L_1 L_2)},$$

$$k_1 = \frac{(AT + BT_I)L1}{T_I AT}, \qquad C_2 = \frac{AT^3 T_I}{C_1 D L_1 L_2}, \qquad (7)$$

$$k_2 = \frac{(ACT^2 T_I + ADTT_I^{\,2} - BC_1 D L_1 T_I - AC_1 D L_1 T) C_1 L_1 L_2}{A^2 T_I^{\,2} T^4}.$$

As illustrated in Figs. 4, 5 depending on the parameters (T, L_1, C_1, L_2), a design space for C_2 can be obtained, which indicates the realizable ranges of the second filter-stage capacitor. The plotted curves describe the physical and the specified limits for a given combination of T and L_2. The arrowheads point in the region where the

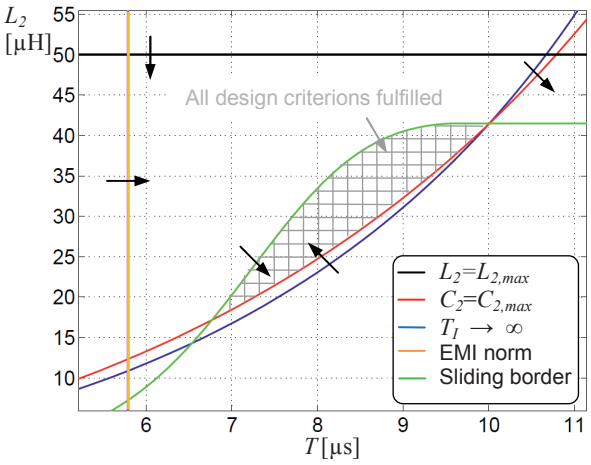

Fig. 4 Design space of the double active damped filter for Butterworth characteristic. The first filter-stage is configured to L_1= 100µH, C_1 = 1µF. The arrowheads indicate the area where the requirements can be met.

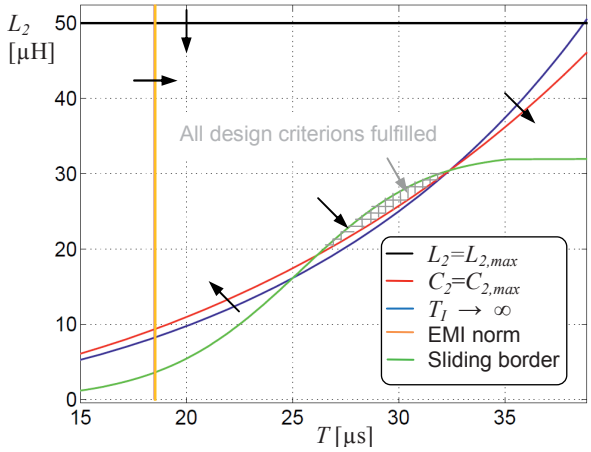

Fig. 5 Design space of double active damped filter for Bessel characteristic. The first filter-stage is configured to L_1= 100µH, C_1 = 1µF. The arrowheads indicate the area where the requirements can be met.

respective criterion is satisfied. As can be observed from (7), for certain parameter sets T and L_2, the control parameter T_I gets infinite or negative (which implicates that C_2 would be negative). Therefore, the values of C_2 in the design spaces are set to zero. The EMI norm defines the minimum value of T at which the EN55011 class-A standard is satisfied. By inserting T_I of equation (7) in k_1, maximum values of $L_2(T)$ can be calculated which implicates that (6) is fulfilled. This is represented by the sliding border in Figs. 4, 5. The hatched areas represent the design spaces where all design criterions listed above are fulfilled. The intersection of the hatched areas leads now to a small but existent value range for the output filter parameters

Table 2: Two-stage LC output filter and controller values used for the simulations.

Double active damped		Single active damped	
Butterworth	Bessel	Butterworth	Bessel
$C_1 = 1\,\mu F$	$C_1 = 1\,\mu F$	$C_1 = 1\,\mu F$	$C_1 = 1\,\mu F$
$L_1 = 100\,\mu H$	$L_1 = 100\,\mu H$	$L_1 = 100\,\mu H$	$L_1 = 100\,\mu H$
$C_2 = 1.47\,\mu F$	$C_2 = 1.47\,\mu F$	$C_2 = 1.88\,\mu F$	$C_2 = 2.41\,\mu F$
$L_2 = 25\,\mu H$	$L_2 = 25\,\mu H$	$L_2 = 25\,\mu H$	$L_2 = 25\,\mu H$
$V_1 = 5.17e4$	$V_1 = 3.55e4$	$V_1 = 4.98e4$	$V_1 = 3.42e4$
$T_1 = 23.7\,\mu s$	$T_1 = 17.2\,\mu s$	$T_1 = 27.6\,\mu s$	$T_1 = 25.6\,\mu s$
$k_1 = 39.5\,V/A$	$k_1 = 39.9\,V/A$	$k_1 = 37.6\,V/A$	$k_1 = 38.1\,V/A$
$k_2 = -4.16\,V/A$	$k_2 = -8.1\,V/A$		

($L_1 - C_2$), where both characteristics (Butterworth and Bessel) can be obtained, only by adjusting the controller as well as the active damping parameters of the system (see Table 2).

2.3. Single Active Damped Amplifier

For specific parameter sets (L_1 - C_2) also a single path active damping is sufficient to achieve Butterworth or Bessel response (see Fig. 6). The advantage is that (i) only a single capacitor current sensor is required and (ii) that an amplifier output current which possibly showing switching frequency components of the fed load (e.g., a tested switch-mode power supply or converter) does not directly affect the amplifier's PWM stage potentially leading to effects similar to the mentioned sliding-mode operation.

The coefficients a, b, c and d of equation (1) for single capacitor current feedback (i_{c1}) are listed in Table 1. Assuming that L_1, C_1 are specified initially, the system of equations (4) again can be solved explicitly for a desired time constant T. After insertion of the parameters according to Table 1, the five unknown parameters L_2, C_2, k_1, T_1 and V_1 can be determined for the single-path

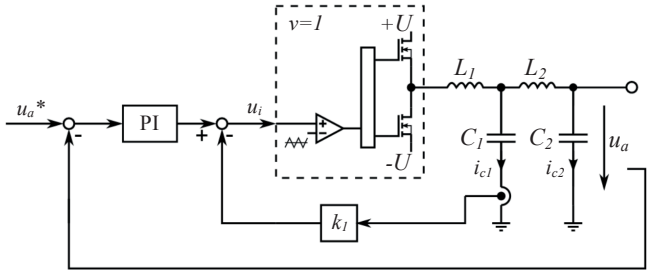

Fig. 6: Proposed closed-loop control concept using a PI-type controller for output voltage control employing additional feedback of the capacitor current i_{c1}.

damped system to

$$V_1 = 1/(DT),$$

$$T_1 = \frac{(BC_1DL_1) - ACT^2}{T_1AT} + \frac{\sqrt{4A^2C_1D^2L_1T^2 + A^2C^2T^4 + B^2C_1^2D^2 - 2ABC_1CDL_1T^2}}{T_1AT},$$

$$L_2 = \frac{AT^3T_1L_1}{BC_1L_1T^2 + C_1CL_1TT_1 - AT^3T_1 - C_1^2DL_1^2},$$

$$k_1 = \frac{(AT + BT_1)L1}{T_1AT}, \qquad C_2 = \frac{AT^3T_1}{C_1DL_1L_2}. \tag{8}$$

For the specified design range of (L_1, C_1, T) only positive values for the control parameter T_1 and the filter inductor L_2 are obtained. In contrast to the double-path actively damped amplifier and as a consequence of a now missing degree of freedom k_2, inductance L_2 depends on the desired time constant T and on the values (L_1, C_1) of the first filter-stage.

Nevertheless, for each characteristic a design space fulfilling all the criterions listed above can be found. Corresponding parameter values for implementing the single active damped amplifier are given in Table 2.

3. Simulation - Experimental Results

The proposed class-D amplifier with double-path active filter damping has to be verified by simulations using GeckoCIRCUITS [8] according the parameters specified in Table 2. The simulation model includes also the pulse width modulation based on a bridge-leg with an interlock-delay of $100\,ns$ ($f_S = 200\,kHz$). A comparison of the analytical (as specified by (2)) to

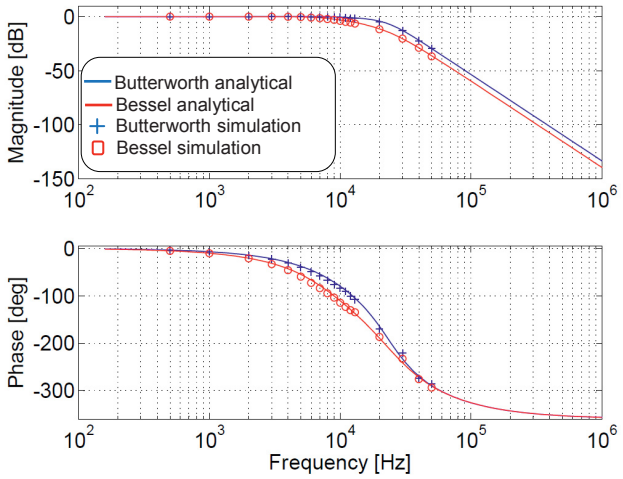

Fig. 7 Simulated transfer function of reference voltage u_a* to output voltage u_a for the double active damped amplifier for a purely resistive nominal load of $40\,\Omega$. The parameter values are taken from Table 2.

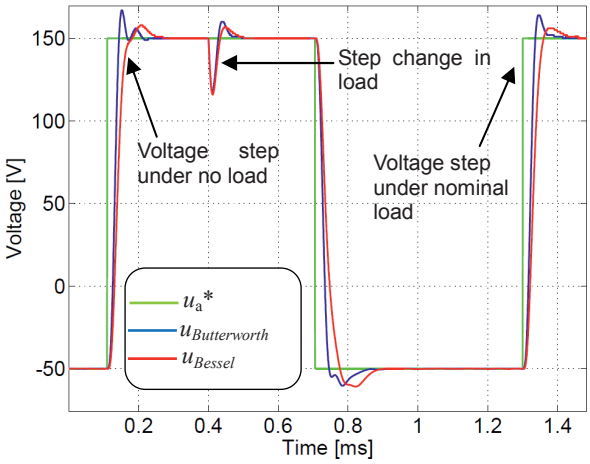

Fig. 8 Output voltage step responses for the double active damped amplifier (digital simulation using GeckoCIRCUITS). $t = 0.1$ ms: no-load reference step response; $t = 0.4$ ms: load step response; $t = 1.3$ ms step response under nominal load of $40\,\Omega$.

the simulated closed-loop transfer functions is depicted in in Fig. 7. It can be observed that for Butterworth-dimensioning the aspired -3 dB-bandwidth of $10\,\text{kHz}$ is achieved and that the standard IEC/EN 55011 class-A noise level is fulfilled (also for no-load operation). The step responses under different load conditions are given in Fig. 8 demonstrating the good reference tracking capabilities of both filter characteristics. Small deviations in comparison to the ideal behavior identified mainly originating from the interlock-delay distortions. A gate-driver optimization striving for interlock-delay as small as possible, therefore, it is highly recommended. Remark: Basically these distortions (as well as on-state voltage drops of the MOSFETs) in principle are already attenuated due to the closed-loop operation where the control-loop "surrounds" the imperfect switching device. It has to be con-sidered, however, that the extra loop-gain added by the PI-controller is not very high, limiting the distortion reduction.

For verifying the simulation results a laboratory prototype class-D amplifier according to the specifications listed above has been designed as a double-path active damping system, where Butterworth as well as Bessel behavior can be implemented (see Fig. 9). Inductors L_1 and L_2 are manufactured using toroidal iron powder cores (Sendust, L_1: Ø35.81 mm, 43 turns, L_2: Ø20.3 mm, 20 turns) leading to rather low AC and core losses as well as a high saturation current limit (in comparison to ferrite materials) resulting in a peak overcurrent capability of about 1:3.

The coils are formed as single layer windings for minimizing proximity effect using standard copper wire. For the filter MLCC ceramic capacitors (Arcshield X7R, 500V) are used which can easily handle the switching frequency ripple. Such capacitors are further used for supporting the DC link electrolytic capacitors. Due to the basic characteristic of all class-D amplifiers, that the switching frequency in practical systems has to be typically 10 to 20 times as high as the aspired amplifier bandwidth, right from the start GaN-MOSFETs are planned to be used. Due to their standard TO220 case with rather good cooling possibility TPH3206P/N by Transphorm has been chosen to achieve a prospective switching frequency of $f_S = 200\,\text{kHz}$ with not to high switching losses and good efficiency [9],[10]. Due to their "quasi-active" freewheeling diode behavior, GaN transistors can be ideally used in bridge-leg structures where conventional MOSFETs suffer from poor diode recovery. Remark: During the implementation and testing process the fear, however that the TO220 case is not perfectly suited for ultrahigh switching-speed semiconductors has proved true. To minimize voltage ringing the commutation loop inductance has to be at least minimized by bypass MLCC capacitors routed as close as possible to the MOSFETs. The advantage of this GaN type is that as result of its cascade structure (normally-on GaN chip in series to a low-voltage Si-MOSFET) the gate drive is comparatively simple, except very high du/dt rates of the high-side driver.

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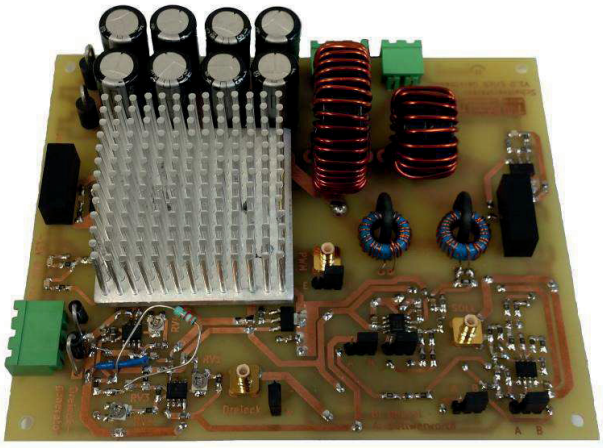

Fig. 9 Laboratory prototype of the double active damped amplifier.

Consequently, a Si82394 isolator/driver is used for the bridge leg which features fully isolation and includes also a programmable interlock-delay, adjusted here to 100 ns. The power supply of the high-side stage is performed by bootstrap/charge pump. The entire control is implemented in analog circuitry using fast OP-amps and comparators giving the mentioned advantage of almost zero PWM phase delay (natural triangle-carrier based PWM). The capacitor current sensing is performed by proper designed passive current transformers inherently giving isolation of power and control stage.

Measurement results of the prototype for sinusoidal 700 Hz-reference voltage under load (40 Ω and 5 mH in series) are given in Fig. 10. Output voltage and current show the expected sinusoidal shape. For current amplitudes however being higher than the ripple amplitude in L_1, small distortions can be observed (red circle) originating from PWM distortions caused by the interlock-delay at points where i_{L1} gets zero within the interlock interval. Consequently, the interlock-delay should be minimized as low as possible. A further improvement may be a future improved gate drive stage using adaptive delay, or a cross-conduction detection today already implemented in some low-voltage DC/DC converter chips.

Figures 11,12 illustrate the prototypes voltage step responses for Butterworth/Bessel dimensioning. Neglecting all parasitic effects like comparator- and interlock-delay the analytical calculations predict a transient voltage overshoot of 11 %/1 % and a rise time of 32 µs/60 µs. For the implemented class-D amplifier 13.5 %/32 µs has been measured for Butterworth response and 5 %/65 µs for Bessel response. Both characteristics show excellent responses and a good coincidence to the idealized values.

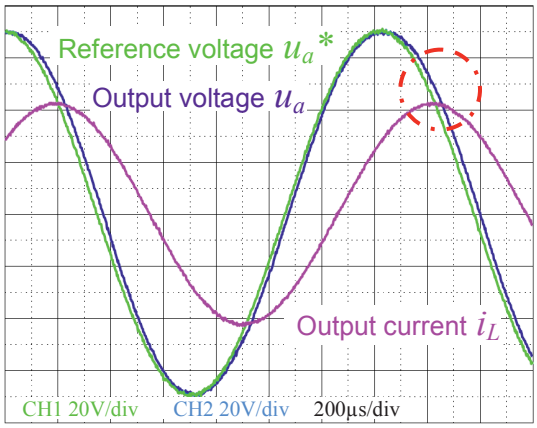

Fig. 10 Measurement result of the output voltage under load of 40 Ω and 5 mH, tested by an operating frequency of 700 Hz and switching frequency of 200 kHz.

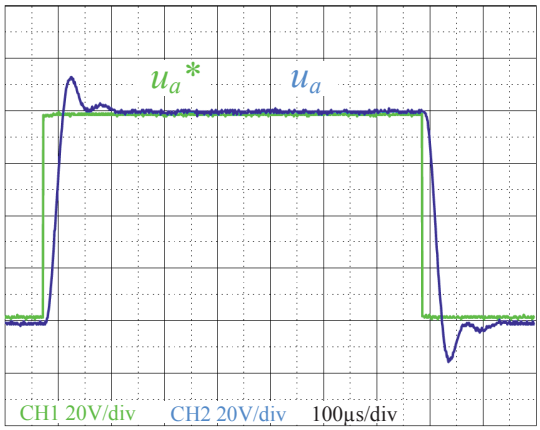

Fig. 11 Measured output voltage step response for the double active damped amplifier in Butterworth mode under no load (-40 V to 40 V).

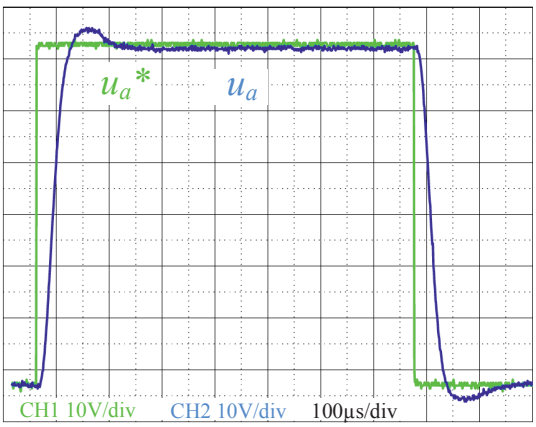

Fig. 12 Measured output voltage step response for the double active damped amplifier in Bessel mode under no load (-30 V to 30 V).

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4. Conclusion

In this work a control loop design for a class-D power amplifier with a two-stage LC output filter is analyzed. The basic idea of the proposed scheme is that the damping of the LC filter is not achieved by dissipative elements or by an ohmic load but implemented actively by filter capacitor current feedback. Furthermore, closed-loop control of the amplifier output voltage is obtained by an additional PI-controller for compensating parasitic effects like DC link variations, switching time errors, switch and filter non-idealities. By a specific parameter dimensioning the controlled system shows a transient/frequency response being identical to the physical limits (i.e., roll-off frequencies) of the LC filter but with a good dynamic behavior like, e.g., Butterworth or Bessel characteristic but in closed-loop operation featuring increased distortion reduction and DC link ripple rejection. Additionally, design space considerations are included for dimensioning of the LC filter elements fulfilling EMI, sliding-mode and realization boundaries. With this, as demonstrated, proper output voltage dynamic characteristic could be guaranteed also for single-path capacitor current feedback leading to a practical implementation of lower effort. Based on the proposed concept a $1\,\mathrm{kW}/\pm 200\,\mathrm{V}$ amplifier based on a half-bridge topology operating at a switching frequency of $200\,\mathrm{kHz}$ is designed. Simulation results identify an amplifier bandwidth of $10\,\mathrm{kHz}$, where a switching noise rejection according to EN55011 class-A is maintained. The analyzed switch-mode amplifier is implemented as a laboratory hardware prototype system using $600\,\mathrm{V}$ GaN-MOSFETs and purely analog control. This actual system shows good output voltage performance, however, some minor voltage distortions resulting from MOSFET interlock-delay (as predicted by digital simulation) appear, which in fact are improved by the used closed-loop structure but not fully suppressed. In course of future research, diverse analog measures for improving the dead-time distortions like PWM feed-forward correction etc. are planned as well as research concerning observer-based implementation of active filter damping without current sensors.

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