Predictive Pulse Pattern Control for a Synchronous Multiphase Buck Converter

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***Abstract*—Finite control set model predictive control (FCS-MPC) has been proven to be a powerful control strategy in power electronics with very high dynamic performance compared to carrier-based pulse width modulation (PWM) approaches while avoiding unnecessarily high switching frequencies that would increase switching losses. However, the limited time resolution often leads to poor steady-state performance and can only be overcome by increasing the sampling rate, which would involve an infeasibly high computational demand. This paper presents a predictive pulse pattern control (PPPC) strategy for a synchronous multiphase buck converter (SMPB) that achieves both objectives yielding in high performance for transient and steady-state operating conditions with a feasible computational demand. At every time step, a pulse pattern with minimal switching effort is selected whose switching instants are obtained by minimizing an objective function yielding in high tracking accuracy. Simulation results demonstrate the potential of the proposed control strategy to outperform state-of-the art control approaches.**

***Index Terms*—Predictive pulse pattern control. Finite control set model predictive control, Optimal switching control. DC-DC conversion.**

I. Introduction

In power electronics, finite control set model predictive control (FCS-MPC) has become a very attractive alternative to carrier-based pulse width modulation approaches [1] based on state-space averaging [2]. The computational burden, however, grows exponentially with the number of input switches and length of prediction horizon. The authors of [3] suggest an improved sphere decoding algorithm firstly introduced for a three-level voltage source inverter (VSI) in [4] to reduce the computational cost of the underlying integer optimization problem. A different approach to achieve longer prediction horizons is to approximate the tail cost using approximate dynamic programming as proposed in [5]. While FCS-MPC achieves excellent dynamic control, steady-state performance is limited by the sampling rate, which in turn also increases computational cost making it infeasible for applications where high tracking accuracy is required [6]. Continuous control strategies on the other hand yield in good steady-state performance whereas the switching frequency limits transient performance. In order to combine both advantages, model predictive pulse pattern control for a three-level VSI is proposed in [7] and validated experimentally for a five-level VSI in [8]. A similar predictive optimal switching strategy for an AC-DC converter suggested in [9] and [10] is restricted to unconstrained problems. A variable switching point torque control method for an induction motor that achieves low current and torque ripples by allowing switching between sampling instants is introduced in [11]. This paper presents a predictive pulse pattern control (PPPC) strategy for an SMPB that achieves a fast transient response and low current and voltage ripples in steady-state. The strategy also meets the requirements of highly dynamic DC-DC converters suitable for nonlinear power source emulators such as battery emulators [12] or solar array simulators [13].

II. System model

The topology of the SMPB is depicted in fig. 1. The rectifier dynamics are neglected, hence, DC-link capacitance C_0 is considered to be high enough to assume constant DC-link voltage V_0. The insulated-gate bipolar transistor (IGBT) semiconductor switches $T_1 - T_8$ are driven by the control unit with binary, complementary signals $S_a - S_d \in \mathcal{U} = \{0, 1\}$. The resistances of phase inductors $L_{1_a} - L_{1_d}$ are modeled with $R_{1_a} - R_{1_d}$ respectively. C_1 denotes the filter capacitance and the cable is modeled with L_2 and R_2. The generic load model consists of C_2 and R_L. The state vector is defined as $\boldsymbol{x} = \begin{bmatrix} i_{L_{1_a}} & i_{L_{1_b}} & i_{L_{1_c}} & i_{L_{1_d}} & v_1 & i_2 & v_2 \end{bmatrix}^\mathrm{T}$, the input vector as $\boldsymbol{u} = \begin{bmatrix} S_a & S_b & S_c & S_d \end{bmatrix}^\mathrm{T}$ and the ohmic share of the load current as the disturbance input $d = i_\mathrm{L}$. The system dynamics is derived using Kirchhoff's laws and can be written as

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{b}\boldsymbol{u} + \boldsymbol{e}d, \tag{1}$$

with

$$\boldsymbol{A} = \begin{bmatrix} -\frac{R_{1_a}}{L_{1_a}} & 0 & 0 & 0 & -\frac{1}{L_{1_a}} & 0 & 0 \\ 0 & -\frac{R_{1_b}}{L_{1_b}} & 0 & 0 & -\frac{1}{L_{1_b}} & 0 & 0 \\ 0 & & -\frac{R_{1_c}}{L_{1_c}} & 0 & -\frac{1}{L_{1_c}} & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_{1_d}}{L_{1_d}} & -\frac{1}{L_{1_d}} & 0 & 0 \\ \frac{1}{C_1} & \frac{1}{C_1} & \frac{1}{C_1} & \frac{1}{C_1} & 0 & -\frac{1}{C_1} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_2} & -\frac{R_2}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_2} & 0 \end{bmatrix}, \tag{2}$$

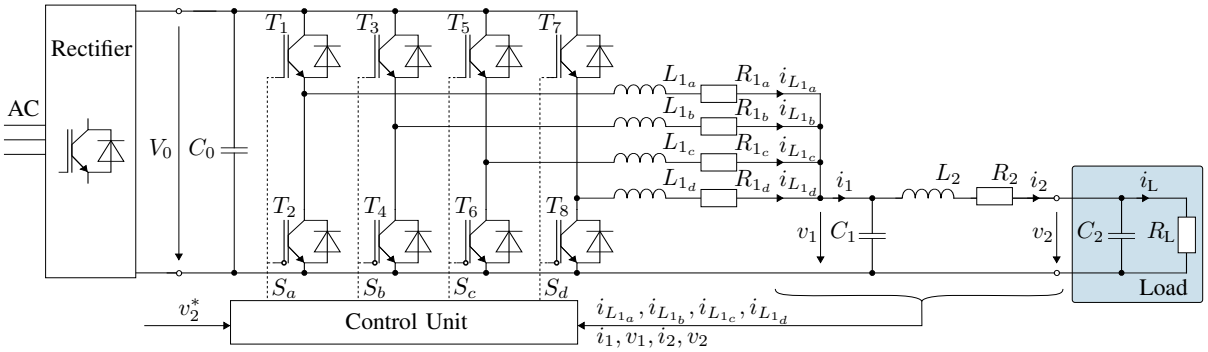


Fig. 1: Synchronous buck converter with four phases including cable and load model.

$$\boldsymbol{b} = \begin{bmatrix} \frac{V_0}{L_{1_a}} & 0 & 0 & 0 \\ 0 & \frac{V_0}{L_{1_b}} & 0 & 0 \\ 0 & & \frac{V_0}{L_{1_c}} & 0 \\ 0 & 0 & 0 & \frac{V_0}{L_{1_d}} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}, \qquad \boldsymbol{e} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -\frac{1}{C_2} \end{bmatrix} \tag{3}$$

and $i_1 = i_{L_{1_a}} + i_{L_{1_b}} + i_{L_{1_c}} + i_{L_{1_d}}$.

III. Control Strategy

The objective is to achieve fast tracking of the output voltage v_2 with high accuracy while respecting constraints on phase currents and achieving robustness against unknown loads. To this end, a two loop structure, as depicted in fig. 2, that decouples disturbance rejection and handling of the switching dynamics is proposed. An outer voltage control loop provides a continuous reference current i_1^* that is tracked by an inner current loop using the PPPC scheme. The inner loop first selects a pulse pattern and then determines optimal switching instants $\boldsymbol{t}^*$ that minimize the current tracking error over the prediction interval T_P. This problem is also known as timing optimization problem [14] and is by far easier to solve than the scheduling optimization problem [15] where additionally the switching sequence is subject to optimization. The pulse generator manipulates the SMPB with discrete inputs $\boldsymbol{u}$ at switching instants in accordance with the selected pulse pattern.

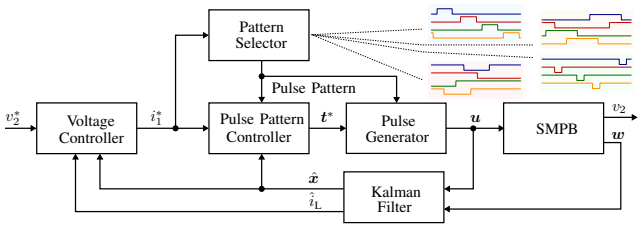


Fig. 2: Cascade control structure with outer voltage control loop and inner current loop using PPPC.

A. Outer loop - Voltage tracking

The outer loop provides a reference current for the inner loop such that the output voltage is tracked accurately and load variations are compensated. For this reason, a Kalman Filter estimates the state vector $\hat{\boldsymbol{x}}$ and unknown load $\hat{i}_\mathrm{L}$ based on the measureable state vector $\boldsymbol{w}$. Moreover, it is used to compensate the computational delay of one sampling period that occurs for computational demanding strategies based on MPC. While the outer loop is not restricted to a specific control strategy, an MPC that provides a current reference i_1^* by minimizing the voltage tracking error over the prediction horizon N_P and considering current limits on i_1 is suggested in this paper. The optimization problem can be formulated in dense form with input constraints only, which can be solved highly efficiently using the fast-gradient method [16]. The finite control set is only considered in the inner loop.

B. Inner loop - Predictive pulse pattern control

The proposed scheme allows two switching actions[1] per phase within the prediction interval T_P that is typically chosen to be equal to the sampling period. Therefore, a set of four pulse patterns which differ in simultaneously active phases is defined to cover the entire output voltage range. The pulse patterns define a switching sequence with a fixed switching frequency and only one change of switching state per switching instant $t_1 - t_7$ for minimal switching effort. As summarized in table I, pattern A allows 0 or 1 simultaneously active phases, pattern B allows 1 or 2, etc. As a result, the minimum and maximum slope of the sum phase current i_1 within one prediction interval for pattern A is given for $\sum_{j\in P} S_j = 0$ and $\sum_{j\in P} S_j = 1 \ \forall t \in [t_k, t_{k+1}]$ with the set of phases $P = \{a, b, c, d\}$. This can be done for the other pulse patterns analogously and allows to determine which pattern is most suitable to track the desired reference current, as depicted in fig. 3. These considerations can easily be extended for the case of asymmetric phases although typically the phases have an equal configuration, i.e. $L_{1_a} = L_{1_b} = L_{1_c} = L_{1_d}$ and

[1] In fact, each pulse pattern contains one phase that switches only one time as the patterns are defined such that the corresponding second switching coincides with the end of the prediction interval. This way one decision variable can be eliminated while the possible switching sequence remains unchanged.

TABLE I: Switching sequences for the set of pulse patterns.

Interval	Pattern A				Pattern B				Pattern C				Pattern D			
	S_a	S_b	S_c	S_d	S_a	S_b	S_c	S_d	S_a	S_b	S_c	S_d	S_a	S_b	S_c	S_d
$t_k \leq t < t_1$	1	0	0	0	1	0	0	0	1	1	0	0	1	1	1	0
$t_1 \leq t < t_2$	0	0	0	0	1	1	0	0	1	1	1	0	1	1	1	1
$t_2 \leq t < t_3$	0	1	0	0	0	1	0	0	0	1	1	0	0	1	1	1
$t_3 \leq t < t_4$	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	1
$t_4 \leq t < t_5$	0	0	1	0	0	0	1	0	0	0	1	1	1	0	1	1
$t_5 \leq t < t_6$	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1
$t_6 \leq t < t_7$	0	0	0	1	0	0	0	1	1	0	0	1	1	1	0	1
$t_7 \leq t < t_{k+1}$	0	0	0	0	1	0	0	1	1	1	0	1	1	1	1	1

$R_{1_a} = R_{1_b} = R_{1_c} = R_{1_d}$. After selecting a pulse pattern, the

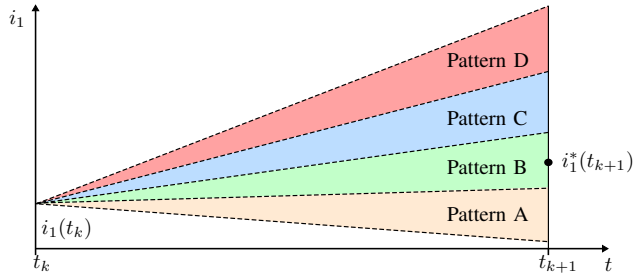


Fig. 3: Predicted current trajectories to select the pulse pattern that minimizes the tracking error at the next sampling instant.

switching instants are determined by solving an optimization problem. The objective function

$$J_1 = \sum_{i=1}^{8} \Bigg(\left(i_1^*(t_{k+1}) - i_1(t_i)\right)^2 + \sum_{j \in P} \alpha_j \left(\frac{1}{4} i_1^*(t_{k+1}) - i_{L_{1_j}}(t_i) \right)^2 \Bigg), \quad P = \{a, b, c, d\} \tag{4}$$

comprises the sum phase current tracking error as well as the phase current tracking error at each switching instant and at the end of the prediction interval t_{k+1} with weighting factors α_j. The former will result in minimal sum phase current ripple and the latter is required to establish equal current balancing. By using the small ripple approximation [2] and by approximating the voltage drop on phase resistances with the average phase current $i_{L_{1_j}}^{\text{avg}}$, the current predictions stated in (4) can be expressed for each pulse pattern (sequence of switching states S_j depends on the pulse pattern) and phase $j \in P$ recursively as

$$i_{L_{1_j}}(t_{i+1}) = i_{L_{1_j}}(t_i) + v \frac{(t_{i+1} - t_i)}{L_{1_j}}, \quad i = 0, \ldots, 7, \tag{5}$$

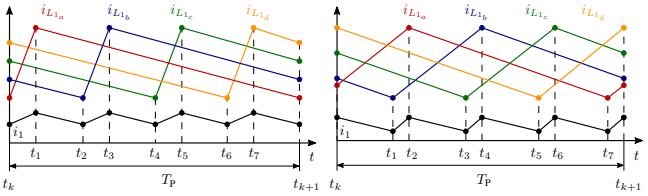
where

$$v = S_j(t_i) V_0 - v_1(t_0) - R_{1_j} i_{L_{1_j}}^{\text{avg}}. \tag{6}$$

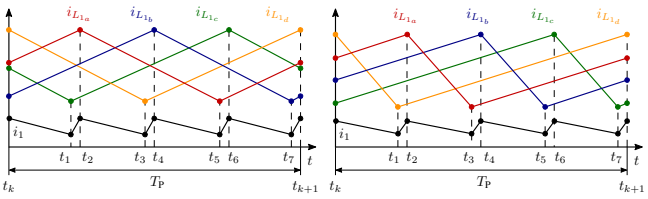
Schematic current predictions for the set of pulse patterns are shown in fig 4. The optimal vector of switching instants $\boldsymbol{t}_k^* = \begin{bmatrix} t_1 & t_2 & t_3 & t_4 & t_5 & t_6 & t_7 \end{bmatrix}^{\mathrm{T}}$ is obtained by solving the boundary control problem

$$\begin{aligned} \boldsymbol{t}_k^* = \underset{\boldsymbol{t}_k}{\text{argmin}} \quad & J_1 \\ \text{subject to} \quad & t_i \leq t_{i+1}, \quad i = 0, \ldots, 7, \end{aligned} \tag{7}$$

where $t_0 = t_k$ and $t_8 = t_{k+1}$. The number of decision variables for the PPPC method grows linearly with the number of phases instead of exponentially as in the case of FCS-MPC. Problem (7) is a standard convex quadratic program that can be solved with an active-set solver proposed in [17]. It shall be noted that the current constraint is assumed to be handled by the outer loop while the inner PPPC loop only accomplishes current tracking. Therefore, the switching ripple of the current has to be considered when defining the current limit. However, the state-space can easily be partitioned to find maximum on-times that can be added to the constraints of problem (7). In



(a) Pattern A: 0 or 1 active phases. (b) Pattern B: 1 or 2 active phases.



(c) Pattern C: 2 or 3 active phases. (d) Pattern D: 3 or 4 active phases.

Fig. 4: Current prediction at time instant k based on decision variables $t_1 - t_7$ for different pulse pattern switching sequences.

contrast to conventional FCS-MPC formulations, the current predictions are based on the continuous-time dynamics, which decouples time resoultion from sampling rate and therefore yields in superior accuracy as the predictions include inter-

sampling instants. Fig. 5 illustrates the different time scales of the inner and outer loop with different prediction lengths.

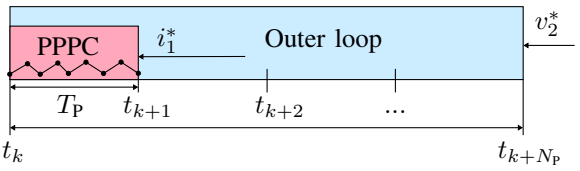


Fig. 5: Different time scales of the inner and outer control loop.

Inclusion of dead times: So far the current prediction model has considered ideal switches with complementary switching signals for each phase. In real systems, however, it is necessary to avoid shoot-throughs by inserting dead times during which none of the switches of a phase is on and the current commutates to one of the corresponding free-wheeling diodes [18]. Considering the effect of dead time on the effective switching instant is subject to future work.

C. Inner loop - FCS-MPC

To assess the performance of the PPPC method, an FCS-MPC similarly as [4] is designed with a prediction length of $N = 1$ and the switch positions $\boldsymbol{u}$ as decision variables. Therefore, an objective function with the sum phase current tracking error, phase current tracking error and switching effort with weighting factors β_j and λ_u is defined as

$$\begin{aligned} J_2 = &\|i_1^*(k+1) - i_1(k+1)\|_2^2 \\ &+ \sum_{j\in P} \beta_j \|\frac{1}{4} i_1^*(k+1) - i_{L_{1_j}}(k+1)\|_2^2 \\ &+ \lambda_u \|\boldsymbol{u}(k) - \boldsymbol{u}(k-1)\|_2^2. \end{aligned} \tag{8}$$

The predictions for $i_{L_{1_j}}(k+1)$ and $i_1(k+1)$ respectively are based on the discrete-time model associated with (1). The optimal switch positions are obtained by solving

$$\begin{aligned} \boldsymbol{u}^*(k) = \underset{\boldsymbol{u}(k)}{\operatorname{argmin}} \quad & J_2 \\ \text{subject to} \quad & \boldsymbol{u}(k) \in \mathcal{U} \times \mathcal{U} \times \mathcal{U} \times \mathcal{U}. \end{aligned} \tag{9}$$

IV. Simulation results

The PPPC strategy is compared to FCS-MPC using a sampling rate of $f_{s,\text{PPPC}} = 16\,\text{kHz}$ in the former and $f_{s,\text{FCS-MPC}} = 256\,\text{kHz}$ in the latter case to allow a fair comparison. Note that the PPPC method can have 8 different switching states for $\boldsymbol{u}$ within one prediction interval. Consequently, the sampling rate for FCS-MPC needs to be significantly higher than the sampling rate used for PPPC in order to achieve a sufficient time resolution. The pulse generator of the PPPC on the other hand needs a sufficiently high time resolution to properly manipulate the switches at the desired switching instants. The simulation does neither consider quantized pulse generator time resolution nor dead times for the switches. Both controllers use the same voltage control in the outer loop, which handles the required constraint on i_1 and are tuned for best performance. A good trade-off between the twofold control objective (sum phase current tracking and phase current balancing) of PPPC was found with weighting factors $\alpha_A - \alpha_D = 16$. The weighting factors for FCS-MPC were set to $\beta_A - \beta_D = 4$ with a switching penalty of $\lambda_u = 525$ to achieve a switching frequency in the range of the PPPC. Fig. 6a and 7a show the sum phase current and output voltage for PPPC and FCS-MPC for a setpoint step from $0\,\text{V}$ to $350\,\text{V}$ with the current limit set to $150\,\text{A}$ per phase. Both controllers accomplish a transition time of approximately $2.5\,\text{ms}$ and suffer from a computational delay of one sampling period that is compensated for by the Kalman Filter. Fig. 6b and 7b illustrate the response to a constant power load with $125\,\text{kW}$ for both controllers. Each one achieves the disturbance rejection in about $1\,\text{ms}$. While the PPPC suffers from a higher voltage drop than the FCS-MPC, it regulates the voltage slightly faster back to the setpoint. The corresponding phase currents are shown in fig. 6c and 6c respectively. The steady-state phase currents, switch states and voltage ripple on v_1 in idle are depicted in fig. 8a, 8b and 8c for the PPPC and in 9a, 9b and 9c for the FCS-MPC. Due to limited time resolution and the trade-off in the associated objective function, FCS-MPC performs worse than PPPC in steady-state. The former achieves an average phase and sum peak-to-peak current ripple of $37.84\,\text{A}$ and $14.28\,\text{A}$ and an average phase and sum switching frequency of $18.75\,\text{kHz}$ and $75\,\text{kHz}$. PPPC on the other hand accomplishes an average phase and sum peak-to-peak current ripple of $42.12\,\text{A}$ and $11.33\,\text{A}$ and a phase and sum switching frequency of $16\,\text{kHz}$ and $64\,\text{kHz}$. Although the FCS-MPC was tuned to yield in a higher switching frequency and therefore in lower phase current ripple, the resulting sum phase current has a higher ripple than for the PPPC. The peak-to-peak voltage ripple on v_1 is $176\,\text{mV}$ for the FCS-MPC versus $19\,\text{mV}$ for the PPPC.

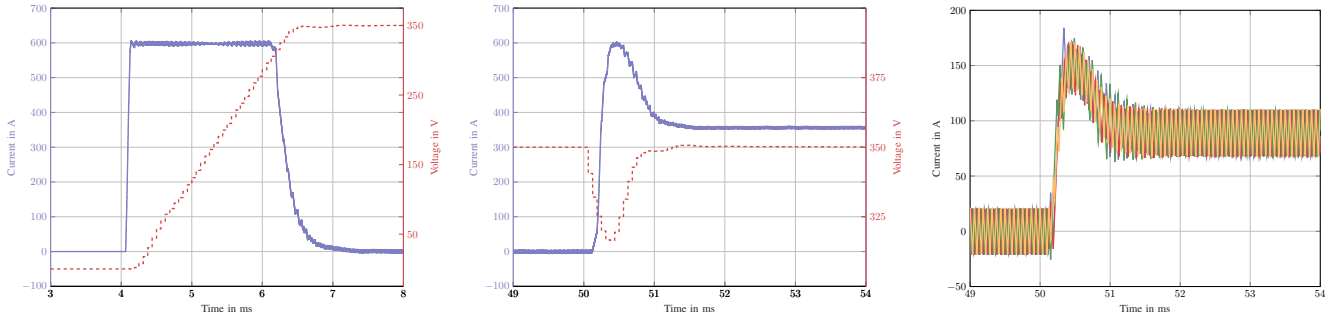
The simulations were done with system parameters listed in table II.

TABLE II: Parameters of the SMPB.

Parameter		Nominal value
DC-link capacitance	C_0	∞
DC-link voltage	V_0	$820\,\text{V}$
Filter inductance	$L_{1_a} - L_{1_d}$	$300\,\mu\text{H}$
Inductor resistance	$R_{1_a} - R_{1_d}$	$10\,\text{m}\Omega$
Filter capacitance	C_1	$1575\,\mu\text{F}$
Cable inductance	L_2	$10\,\mu\text{H}$
Cable resistance	R_2	$50\,\text{m}\Omega$
Load input capacitance	C_2	$2300\,\mu\text{F}$

V. Conclusion

This paper proposes a tailored pulse pattern control approach that allows fast tracking during transients as well as high performance in steady-state for an SMPB. While conventional PWM-based control strategies achieve good steady-state performance, their transient response is limited by the switching frequency that is proportional to switching losses.

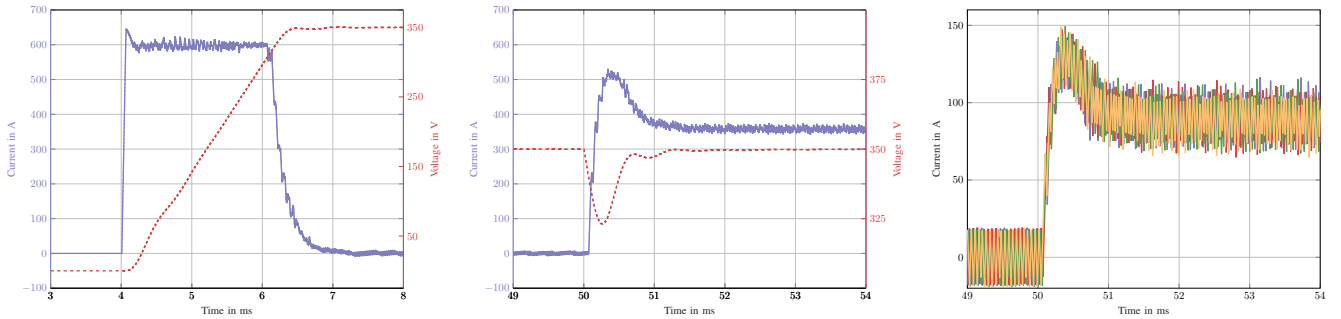


(a) Sum phase current i_1 and output voltage v_2 (dashed) for a setpoint step from 0 V to 350 V.

(b) Sum phase current i_1 and output voltage v_2 (dashed) when enabling a constant power load with 125 kW.

(c) Phase currents when enabling when enabling a constant power load with 125 kW.

Fig. 6: Dynamic performance of PPPC with a sampling rate of 16 kHz.



(a) Sum phase current i_1 and output voltage v_2 (dashed) for a setpoint step from 0 V to 350 V.

(b) Sum phase current i_1 and output voltage v_2 (dashed) when enabling a constant power load with 125 kW.

(c) Phase currents when enabling a constant power load with 125 kW.

Fig. 7: Dynamic performance of FCS-MPC with a sampling rate of 256 kHz.

FCS-MPC on the other hand provides a fast transient response, but performs poorly in steady-state due to a limited time resolution and a resulting high computational effort when increasing sampling rate. The PPPC strategy achieves both goals by solving a constrained quadratic program efficiently. The computational demand of PPPC scales linearly with the number of phases in contrast to exponential growth of FCS-MPC. The simulation results demonstrate the high performance of the proposed control strategy for transient and steady-state operating conditions.

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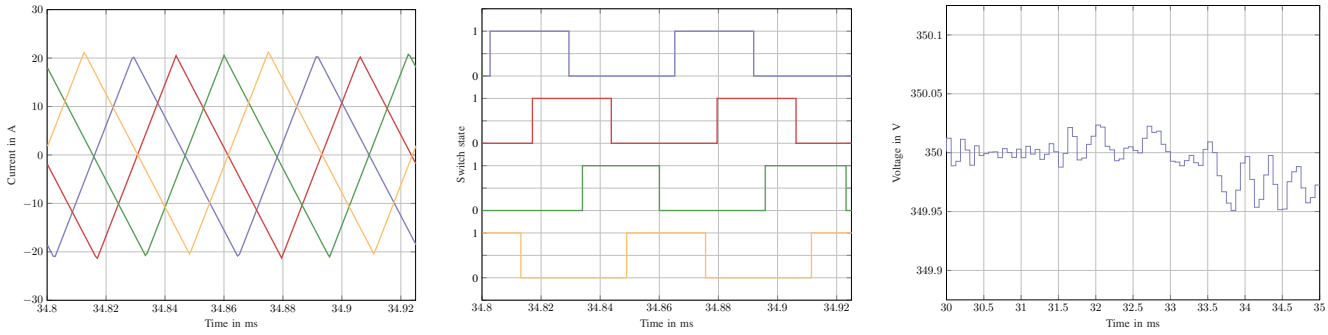
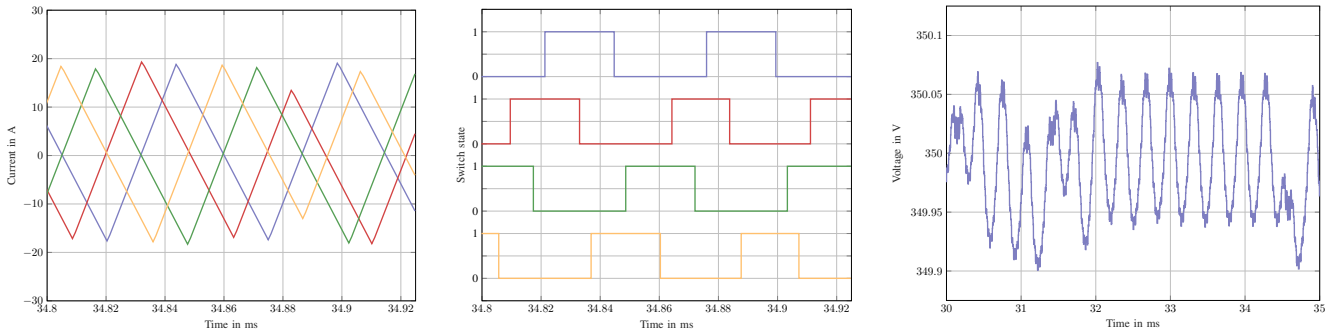


(a) Phase currents. (b) Switch states. (c) Voltage ripple.

Fig. 8: Steady-state performance of PPPC with a sampling rate of 16 kHz at 350 V.



(a) Phase currents. (b) Switch states. (c) Voltage ripple.

Fig. 9: Steady-state performance of FCS-MPC with a sampling rate of 256 kHz at 350 V.

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