All-optical address recognition based on Mach-Zehnder interferometer

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Abstract. We introduce a novel method for all-optical address recognition by using the semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI). The phase of a locally generated Continuous Wave (CW) light beam is modulated in each arm of the Interferometer. In one arm the CW light is modulated by the incoming address signal and in the second arm by the locally generated address. Destructive interference occurs at the output when the bit sequence is equal and constructive if one or more bits are different. The feasibility of our scheme is demonstrated and the simulation results are shown.

1 Introduction

For the development of packet-switched optical network, the following issues should be solved:

- buffering problems
- compression and decompression of the packets
- optical time division demultiplexing (in OTDM networks)
- optical processing of the header

In an optical packet-switched network data is transported in a form of optical packets. Such packets consist of two sections: a header section and a payload section. The header section contains address and protocol dependent control information. When the optical packet arrives at the node it must be dropped or forwarded to the following node depending on the address indicated in the header. In order to perform this, the optical packet can either be converted to the electrical domain, the address can be converted to the electrical domain, or the address can be processed in the optical domain. To switch the optical packet (e.g., by using a basic 2x2 switch shown in Fig. 1), an electrical control signal is needed. It is possible to get this signal as a result of comparing the local header address with the incoming address. This can be done in the *electrical* or in the *optical* domain. However, the electrical solution is limited in terms of the processing speed. High-speed electronics are expensive as well. Several all-optical address recognition methods have been proposed and investigated in the recent past [1,2,3,4,5]. Besides high power requirements [1,2,4] and large physical sizes [1,3], those techniques primarily suffer in limiting of the address length to only few bits. Our method is intrinsically unrestricted in terms of the address size.
Fig. 1 demonstrates a typical optical node architecture deploying an all-optical address recognition unit. A small fraction of the incoming optical packet, which typically consists of a header and payload section, is fed into the header recognizer via an optical splitter. If the packet's destinations address matches the local node address, the packet is received by this

node and the optical switch is set to "cross" state leading to a sink. In the opposite case, the switch is set to the "bar" state and the packet passes through the node. Note that an appropriately adjusted optical delay is placed on the transmission path to compensate for the switching latency.

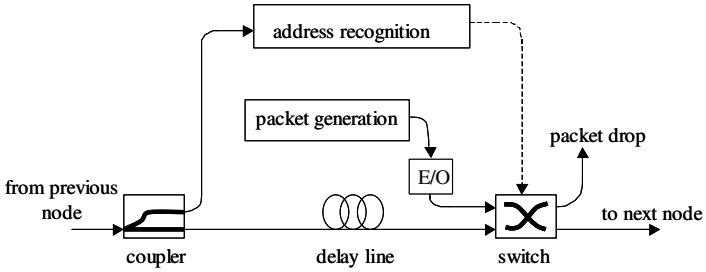

Figure 1. General optical packet switching node architecture

2 Address Recognition

The general configuration of the proposed all-optical header recognition scheme is shown in Fig. 2. It consists of a Mach-Zehnder Interferometer (MZI) equipped with one Semiconductor Optical Amplifier (SOA) at both of the interferometer arms.

It is very seldom that the local and incoming address will have the same amplitude. They are not coherent and in phase with each other. We use a source of CW light and split it to get two coherent light beams. The phase of these light beams is modulated in the SOA_1 and SOA_2, by incoming and local address signals, respectively. Cross-gain modulation (XGM) inside the SOA is performed as well. The modulation of their phases and gains still vary depending on the power difference between incoming and local address peak power and their pulse widths. Moreover, the synchronization of these two signals plays an important role as well. Additionally, if the device is not integrated, a phase shifter has to be inserted in one arm to equalize the phase asymmetries of the MZI.

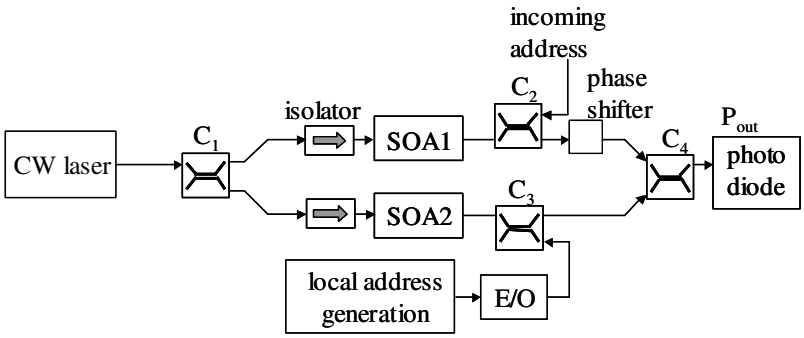

Figure 2: MZI as XOR gate

The incoming header is launched into the first arm via coupler C_2, while the local header is inserted into the second arm through coupler C_3 in a counter-propagating manner relative to the CW beam direction (thus no optical filters are needed). Counter-propagating scheme is used because the address and the CW beam can be spaced relatively near in the frequency domain, which simplifies the simulation. However, for the practical set-up co-propagating scheme is even more favorable while the carrier density inside the SOA is changed even more due to the address signal.

The main detected output power with respect to the overall phase shift $\Delta\phi=\phi_1-\phi_2$ between the arms is given by:

$$P_{out} = \frac{1}{T_a}\int_0^{T_a}\frac{1}{8}P_{CW}\left[G_{SOA1} + G_{SOA2} + 2\sqrt{G_{SOA1}G_{SOA2}}\cos(\Delta\phi)\right]dt$$

$$G_{SOA_n} = f[P_{ai_n}(t)] \quad , \qquad n = 1,2 \tag{1}$$

with T_a denoting the header duration. Consider that couplers C_1 and C_4 together cause a π phase shift between two arms, while couplers C_2 and C_3 are only introducing losses.
The phase of the signal is changed by the following formula:

$$\phi_n = \frac{2\pi nL}{\lambda} + \frac{g_0 bL}{2}\left(\frac{P_{a_n}}{P_{a_n} + P_s}\right) \quad , \qquad n = 1,2 \tag{2}$$

The first part is the nominal phase shift, where n is the material refractive index and L the length of the SOA. The second part results from the change in carrier density from the nominal value when no signal is present. g_o is unsaturated material gain coefficient in the absence of the input signal and b is linewidth broadening factor. The bias condition is set up such that an incoming or generating address signal can additionally make a π phase shift, which will cause destructive interference in the case that both addresses contain identical bits at the same time. Constructive interference occurs with non-identical bits.
XGM is performed inside the SOA_1 and SOA_2 as well. Note that the instantaneous amplification of the SOAs is provided by the following recursive formula:

$$G_{SOAn} = G_0 e^{-\frac{P_{CW} + P_{ai_n}}{2P_s}(G_{SOAn} - 1)} \quad , \qquad n = 1,2 \tag{3}$$

where G_0 denotes the unsaturated gain, P_s the average signal power in the SOA when the material gain is 50% of its unsaturated value. P_{ai1} and P_{ai2} represent the instantaneous optical power of the incoming and local header, respectively. P_{cw} is the output power of the CW laser. In the case of non-identical bits in the incoming and local address, the CW light beams in both arms experience the same additional phase shift and the same amplitude changes, if the peak powers of the incoming and local address are the same $P_{a1} = P_{a2}$. However, $\Delta\phi = \pi$ due to the couplers C_1 and C_4. This leads to destructive interference and the power at the output is 0. In the case of non-identical bits, additional phase shift causes constructive interference, so that the output power is greater than zero.

3 Simulation results

Extensive simulations have been carried out in order to evaluate the feasibility of the proposed address recognition technique. Particularly, the dependence of the optical output power on different parameters such as pulse width, power deviation and synchronization mismatch (detuning) between the incoming and the local address signals is analyzed for different bitrates.
The address signal is RZ (Return to Zero) modulated and the length of the SOAs is chosen to be L = 400 µm and the facet reflectivity is 0. CW laser has 10 MHz linewidth and the output power P_{cw} = 1mW. Fig. 3 demonstrates the dependence of the detected optical power (in logarithmic scale) on the power ratio P_{a1}/P_{a2} and the address length for 2,5 Gbit/s and 80 Gbit/s. Pulse width is the same and P_{a1} and P_{a2} are the peak powers of the incoming and the local pulses, respectively. P_{a2} remains at 10mW level, while P_{a1} is changed. The power curves for differently sized addresses, in which only one bit prevents a complete address match, are compared to the case, where the local address is solely made up of "1" bits (111…1) representing the worst case scenario for address power deviations. The one mismatched bit is located in the incoming address bit stream.

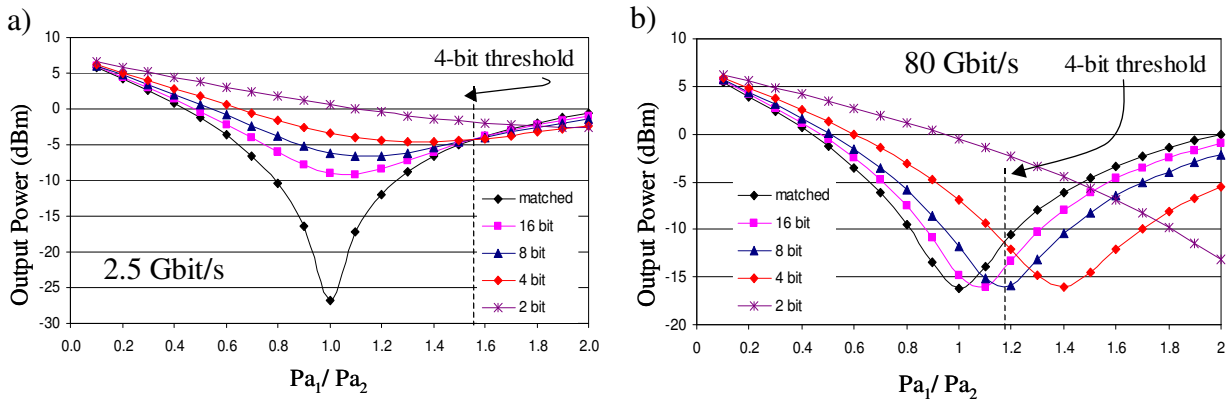

Figure 3: Output power versus address power ratio for matched and one bit mismatched address

Generally, a sufficient margin (see Fig. 4) for the correct address detection may be observed. The higher the deviation relative to the matched address case, the better the operation. However, after a certain deviation, the address cannot be recognized any more since the corresponding power values cross the matched address curve. Moreover, this threshold is significantly shifted towards lower deviations (approach $P_{a1} = P_{a2}$) for higher bit-rates as can be seen in the 80 Gbit/s diagram. For demonstration, the threshold for the 4-bit address case is also indicated in Fig. 4. The difference between mismatched and matched cases shows the region where the address recognition is possible (above 0mW level). This is shown in Fig. 4 for 20 and 80 Gbit/s. It can be seen that for a 16-bit address and 80 Gbit/s bit rate the P_{a2} has to be adjusted very precisely with respect to the power of the incoming address P_{a1}.

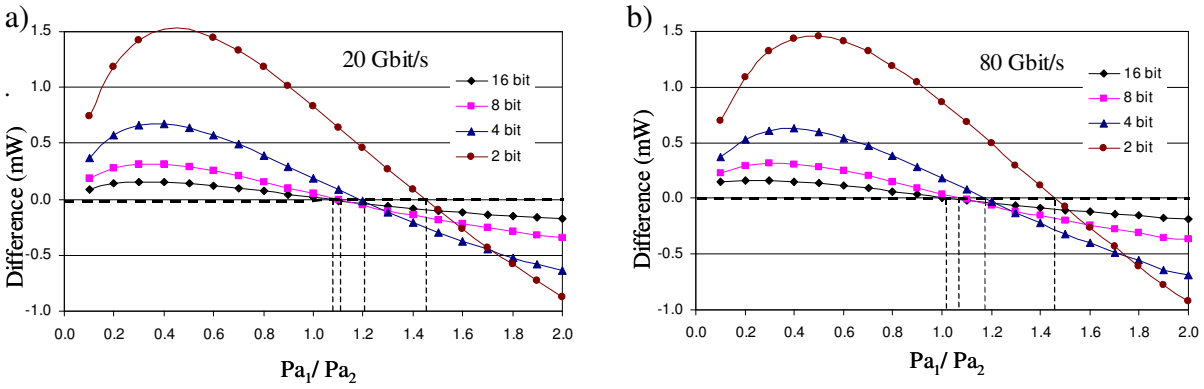

Figure 4: Difference of the power between not matched and matched case

The asymmetric shape of the power curves in Fig 4. is a result of the mismatched address bit, which is placed in the incoming address. When the one zero bit that prevents complete address matching is in the local address and not in the incoming one, the threshold lines are situated on the left side of the graph, as can be seen in the Fig. 5b. In Fig. 5a, where the dependency on the incoming address signal detuning with respect to the local address (for a 101010…10 bit sequence) is illustrated, it can be seen that the detuning has a relatively low impact on the detection capabilities of the system for the 2.5 Gbit/s bit-rate.

However, the synchronization between the incoming address and the local one is important even for the lower bit-rates when $P_{a1} \neq P_{a2}$ (see Fig. 5b and 6). As it can be seen from Fig. 5b, the power difference curve of the mismatched and the matched addresses will cross the zero point at about 0.6 ($P_{h1} = 0.6 \cdot P_{h2}$) for the case of 16-bit address. That means that the power of the incoming address can vary up to 40% and it is dependent on the synchronization of two bit streams. When the addresses are well synchronized (detuning below 20 ps), this difference is even larger. Thereby, it is possible to distinguish one different bit in the 4-bit address even if the power of the incoming address vary up to 50%.

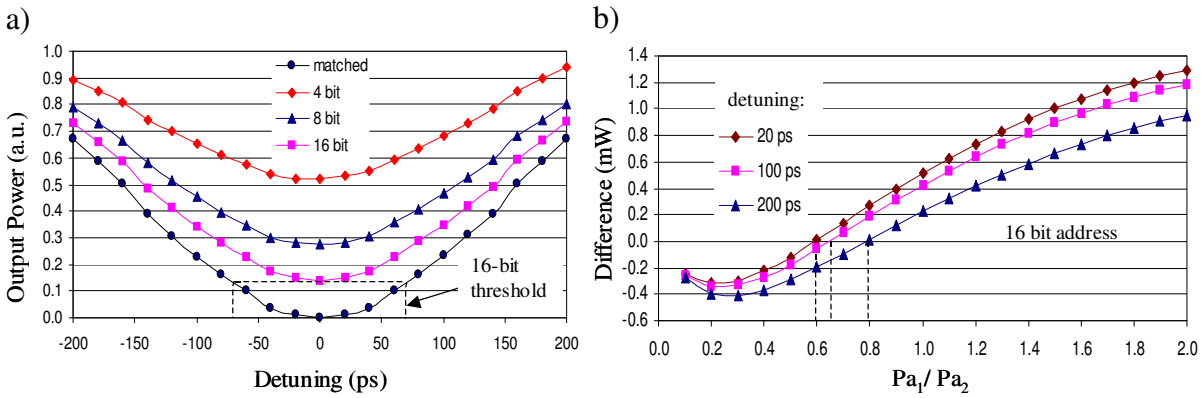

Figure 5: a) Output power in dependence on the synchronization mismatch between Pa_1 and Pa_2
b) Output power difference curve

Otherwise it will be less possible to distinguish one different bit, and for 200 ps detuning of the incoming signal, its peak power can vary just 20% of the P_{a2} value.

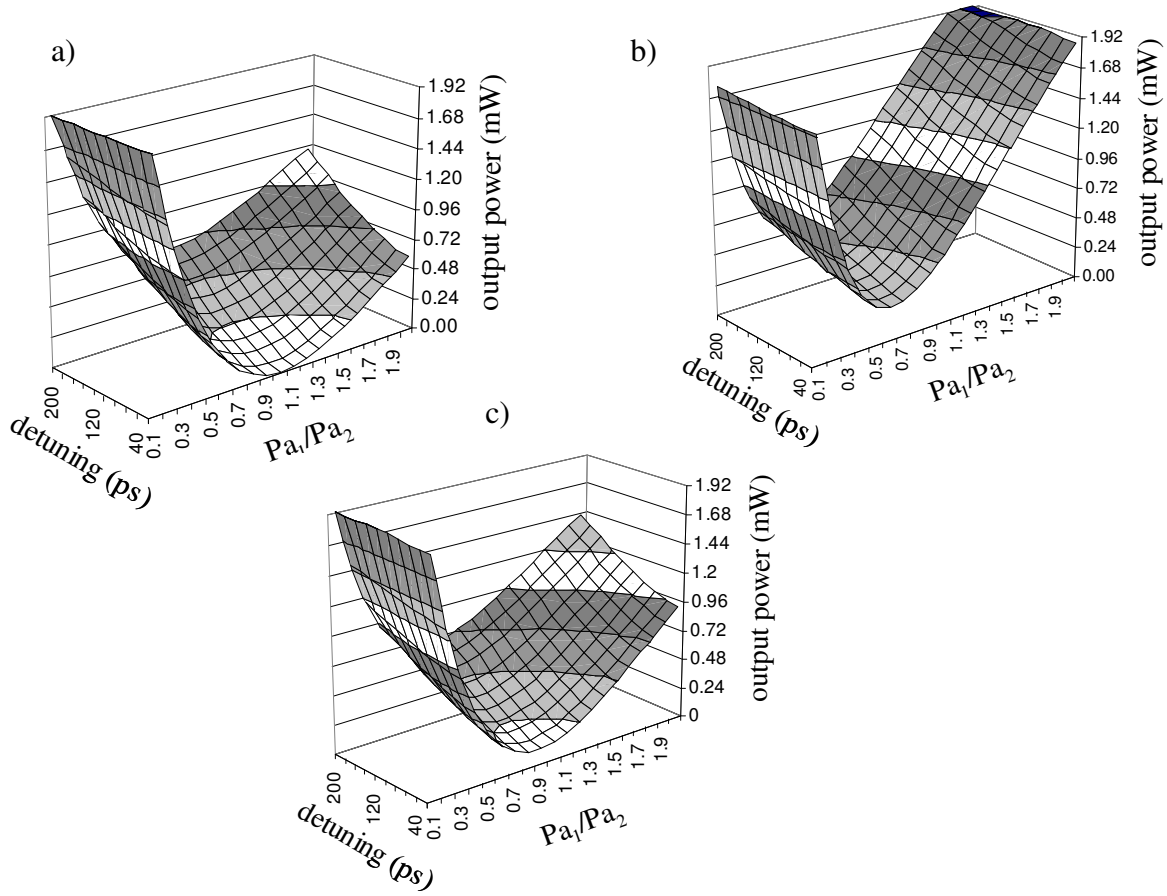

Figure 6: Output power versus address power ratio and synchronization mismatch between Pa_1 and Pa_2 for a)-equal, b) and c)-unequal incoming and local addresses

3D graphs in Fig. 6 depict the dependence of the output power on the peak power ratio of the incoming and local signal and of the detuning of the incoming address for the 2.5 Gbit/s bit-rate. Fig. 6a shows the case where the addresses are matched. The worst case where just one bit is different and address length is 4 and 16 bits is shown in Fig. 6b and 6c, respectively. It can be seen that the 16-bit address plane lies on a lower level than 4-bit address. The difference between the 16-bit address plane and the matched one is lower and therefore it is more difficult to distinguish one bit that is not matched. That is especially the case in that region of the graph, where detuning of the incoming signal increases.

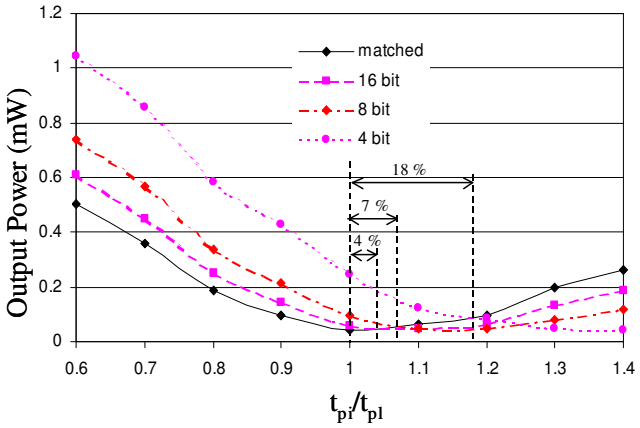

Figure 7: Output power versus pulse length ratio of the incomming and local pulses (80Gbit/s)

Fig. 7 depicts the importance of having similar pulse durations in incoming and local addresses. Locating the mismatched "0" bit in the incoming address causes the upper limit for the incoming address pulse widths. For example, for an 80 Gbit/s signal and 4-bit address, incoming address pulses can be up to 18% broader than the local pulses. For a 16-bit address this will be only 4%. Otherwise, if the mismatched "0" bit is located in the local address, the pulse widths would be limited inversely.

4 Summary and Conclusions

In conclusion, we proposed a novel and relatively simple optical address recognition scheme. Our proposed method is intrinsically unrestricted in terms of the address size. However, for higher bit-rates and a longer address size, power equalization of the local and incoming signal, their synchronization and detection capabilities of the deployed photo detector play a very important role. To achive a better symmetry between two MZI arms, an integrated version of MZI can be implemented.

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