AN OVERVIEW ON NEW TECHNOLOGIES IN ACCESS NODE DESIGN FOR ULTRA FAST PHOTONIC NETWORKS EMPLOYING OTDM

Slaviša Aleksić, Vjeko Krajinović, Kemal Bengi, Harmen R. van As
Vienna University of Technology,
Institute of Communication Networks
Favoritenstrasse 9/388,
A-1040 Vienna, Austria

Abstract: In this paper, photonic technologies for the realization of high-capacity optical time-division multiplexed (OTDM) local and metropolitan area networks (LANs and MANs) are addressed including all-optical techniques such as ultra short pulse generation, all-optical clock recovery, optical multiplexing/demultiplexing, and optical packet compression/decompression. Furthermore, the new trends in high-speed electronics, data processing and optical interconnects are analyzed enabling the avoidance of the electronic processing bottleneck. By the use of both, high-speed electronics for implementing functions of higher complexity with higher level of parallelism and all-optical techniques for the realization of simple ultra fast (> 40 Gbit/s) medium access functions, a hybrid medium access node capable of handling high data rates can be designed.

Keywords: OTDM, all-optical techniques, MAC-node design, high-speed electronics, high-speed optical interconnects

1. INTRODUCTION

Ultra high-speed optical technology that offers aggregate bit-rates in the upper Tbit/s range will be needed due to the fast growth of Internet traffic demand as well as for supercomputer interconnections and tele-medicine applications. Single-mode fibers operated at the 1.55 μm window provide a potential usable transmission capacity of 20 Tbit/s.

Currently, most research efforts in photonic networks concentrate on two primary techniques for multiplexing data onto a single fiber: WDM (wavelength-division multiplexing) and OTDM (optical time-division multiplexing). The major part of that research is devoted to WDM systems. An important reason is that the basic technologies used in WDM networks are to a large extent commercially available (e.g. optical filters, WDM-demultiplexers, sources with narrow linewidth, etc.). On the other hand, technologies for ultra high-speed single-wavelength transmission are still in the experimental phase. A number of research institutes are currently investigating on ultra high-speed OTDM technology including Princeton University [1], Heinrich-Hertz-Institut [2], BT Laboratories [3], Nippon Telephone & Telegraph (NTT) [4], University of Michigan [5], M.I.T. Lincoln Laboratory [6] as well as many others. OTDM systems overcome some of the difficulties associated with WDM transmission, e.g. four wave mixing (FWM) and lacking gain-uniformity of fiber amplifiers with respect to wavelength. Recently, very high bit-rate point-to-point transmission up to 640 Gbit/s of RZ (Return to Zero) optical signal over a 60 km dispersion-managed fiber using 250 fs optical pulses has been reported [7]. This high link capacity offers great opportunities for the Next-Generation Internet (NGI). Some other applications, including localized networks such as those found in multiprocessor interconnects as well as computer local area networks (LANs) and metropolitan area networks (MANs) can benefit from optical TDM technologies as well.

A significant increase of transmission rates in recent years imposes new requirements on access node architectures and high-speed protocol implementations. By the use of both new technologies and the efficient design of the medium access node (as well as the interface to the next layer in the protocol stack), the communication bottleneck can be transferred to the higher layers or directly to the workstation in the near future. Thus, the medium access node design is a very important issue by the realization of ultra fast photonic LANs and MANs [8].

All-optical networks allow signals to remain in an optical format until they arrive at their destination. By avoiding the bottleneck due to the electro-optic and opto-electronic conversions, all-optical networks provide high bandwidth, bit-rate/format transparency, and fault-tolerant communications. In principle, there are two kinds of all-optical networks: circuit-switched and packet-switched. The circuit-switched all-optical networks are less efficient than packet-switched networks. In the packet-switched all-optical networks, an optical packet consists of a fixed-length header and a payload section. Usually, the header contains the source address, the destination address, as well as the information about type,

format, and bit-rate of the payload. All transit nodes must be able to receive and process the packet header on the fly and to perform routing decision within the shortest time. At ultra high bit-rates this can be achieved only by the use of all-optical processing techniques. An optical packet can be either dropped by the node or forwarded to the other nodes in the network by an optical switch. The destination node must be able to receive the payload at a very high medium bit-rate. Through the use of new technologies a high-speed medium access node capable of handling high data rates up to 100 Gbit/s is feasible.

In this paper, we address an appropriate medium access node design for high-speed OTDM local and metropolitan area networks. In this context, an overview of new technologies and approaches towards all-optical techniques is given. Also, the latest research efforts and results in high-speed electronics and opto-electronic processing systems are briefly reviewed.

2. MEDIUM ACCESS NODE DESIGN STRATEGY

With the increase of transmission bandwidth provided by the optical fiber communication technology, the communication bottleneck has been transferred from the transmission medium to the protocol processing unit. Consequently, a new design strategy has to be developed to eliminate the protocol processing bottleneck. Various methods can be employed to solve this throughput preservation problem and to improve MAC-protocol performance, for example:

- Use of ultra high-speed optical components, and high-speed electronics for the realization of ultra fast MAC-protocol functions.
- High level of parallelism, both multiple data parallelism and multiple processing parallelism.
- Optimal trade-off between optics, electronics, and software, concerning implementation of various protocol functions.
- Design of a simple and efficient medium access control protocol.
- Enable optimal interprocess communication.

OTDM technology can be used to maximise the utilisation of the optical fibre by circumventing the electronic bottleneck, thereby providing high-speed access to the optical fibre. Attachment of the medium access node to the high-speed optical TDM network can be realized by using one of the two main multiplexing techniques: *bit-interleaved OTDM* and *packet-interleaved OTDM.*

In *bit-interleaved OTDM-systems* the specific time slots identify each low bit-rate channel in a bit-interleaved manner. OTDM-systems in bit-interleaved manner can be described as follows:

At the transmitter, an optical pulse source produces short pulses at the low bit-rate B_b (basic bit-rate that can be processed electrically) as shown in Fig. 1. This train of picosecond duration optical pulses is spitted into N ways by an 1 x N optical splitter. Each pulse-train is individually modulated by a tributary electrical data signal at the basic bit-rate B_b. The resulting N modulated RZ-signals are then multiplexed using passive optical delay lines and N x 1 optical coupler to produce a high-speed OTDM RZ-signal at the aggregate bit-rate B ($B = N \cdot B_b$).

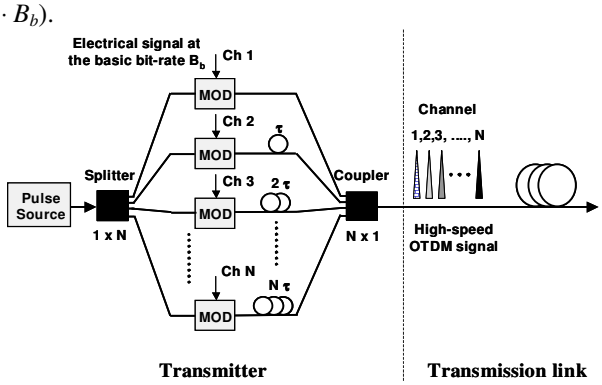

Fig.1: Bit-interleaved OTDM transmitter.

Basically, at the receiver, a demultiplexer splits the incoming high-speed OTDM signal into individual low-speed channels, which can be detected and further processed electronically. A clock recovery circuit recovers the clock from the incoming signal. The recovered clock is used to synchronize optical demultiplexing (Fig.2).

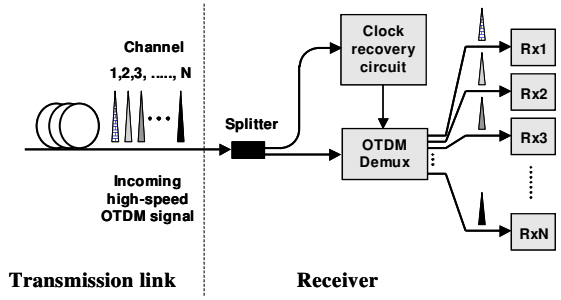

Fig.2: Bit-interleaved OTDM receiver.

Optical add/drop multiplexers are required to extend the OTDM point-to-point transmission to an optical network domain. The add/drop functionality consists of dropping a single low-speed channel from the incoming high-speed OTDM signal and inserting a new low-speed channel into the vacant time slot as indicated in Fig. 3.

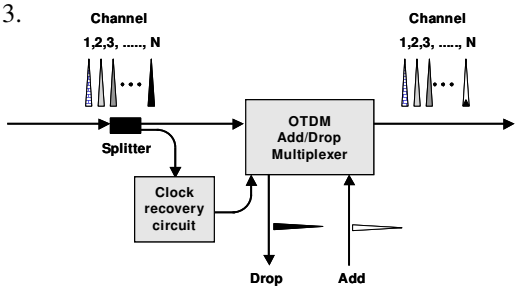

Fig.3: Bit-interleaved OTDM add/drop multiplexer.

Naturally, synchronization in OTDM networks is a very important issue. Especially, in bit-interleaved OTDM networks the synchronisation at the bit-level is

required and the bit-rate/format transparency cannot be provided. Furthermore, intra- and inter-channel interferometric cross-talk and walk-off caused by mismatched wavelengths of the pulse sources at the remote add/drop multiplexers can seriously impair the optical signal and severely limit the cascadability.

Packet–interleaved OTDM networks provide high-speed access to the optical medium employing the optical packet compression/decompression method. We call this kind of networks Optical Packet Compression Time Division Multiplexing (OPC-TDM) networks. In those OPC-TDM networks, walk-off and inter-channel interference are no more the critical issues. Moreover, the OPC-TDM networks can provide the bit-rate/format transparency.

As shown in Fig. 4, an optical TDM channel corresponds to a slot of fixed length consisting of a header and a payload section. Depending on the packet destination address, incoming high-speed packets can be either dropped or forwarded by an optical switch located at the node. An optical delay line is employed in the optical path to compensate the header processing latency of the nodes. The high bit-rate payload must be down-converted to the low bit-rate suitable for electronical processing, saving and interpreting by the use of the Optical Packet Decompression Unit. On the other hand, the low bit-rate packet acquired from the transmitting queue must be at first up-converted to the high medium data rate and after that inserted in the network by replacing of a dropped or an empty packet.

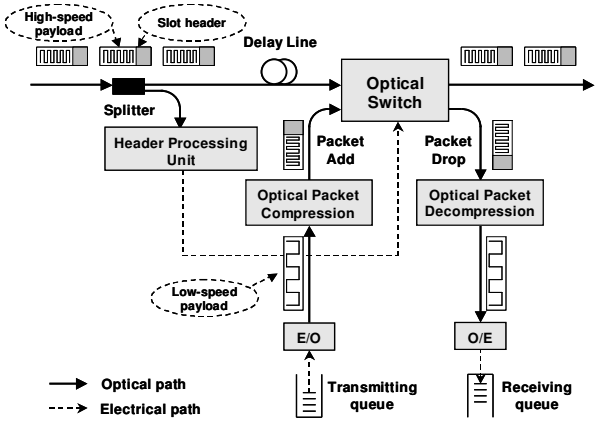

Fig.4: Node architecture for OPC-TDM networks.

Regardless of whether bit-interleaved or packet-interleaved multiplexing technique is used, it is possible to define a common protocol implementation strategy for high-speed OTDM nodes. The design strategy for ultra high-speed OTDM network nodes is indicated in Fig. 5, and is discussed in the following:

- **Medium Attachment Unit (MAU)**

The *Medium Attachment Unit (MAU)* interfaces the OTDM network node to the high-speed optical TDM LAN/MAN. Since high-speed data-rate and bit-rate/transparency are required, the MAU-functions must be implemented in optics. The functions implemented in the MAU are e.g. high-speed optical switching, optical signal pre-amplification and boosting, optical signal splitting and coupling as well as OTDM add/drop multiplexing. Losses and cross-talk in switches, ASE (Amplified Spontaneous Emission) noise accumulation, and interferometric cross-talk in OTDM add/drop multiplexers influence optical signal resulting in the limited node cascadability. Therefore, the MAU block is partly embedded into the high-speed network as depicted in the Fig. 5.

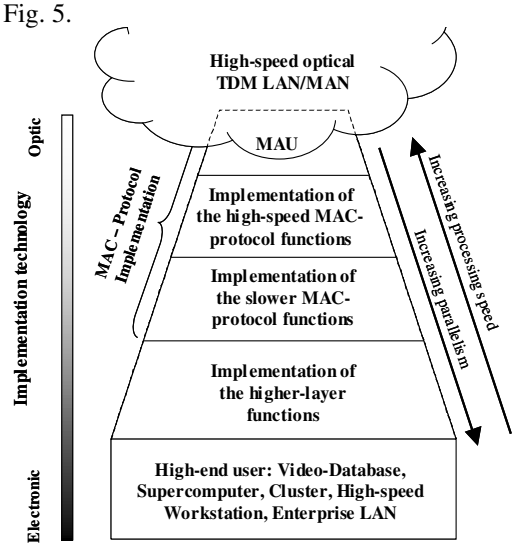

Fig.5: Protocol implementation strategy (MAU – Medium Attachment Unit, MAC – Medium Access Control).

- **Implementation of the high-speed MAC-protocol functions**

High-speed MAC-protocol functions can be implemented in optics, in high-speed electronics or in opto-electronics. If ultra high processing speed is required, the protocol functions must be implemented in optics. Examples for such functions are OTDM multiplexing/demultiplexing, optical packet compression /decompression, and all-optical header recognition.

At ultra high bit-rates (more than 40 Gbit/s), all-optical time division multiplexer and demultiplexer are feasible. The principle of an optical TDM multiplexer is shortly explained above and depicted in Fig. 1. It is relatively easy to build an OTDM multiplexer even at very high bit-rates. However, the realization of the high-speed OTDM demultiplexer is more complicated. Recently, an OTDM demultiplexer realized as a hybrid-integrated symmetric MZ (Mach-Zehnder) interferometer with SOAs (Semiconductor Optical Amplifier) in its arms have been used to demultiplex 10.5 Gbit/s data channels from 168 Gbit/s data streams [9]. Another principle is to use the SOAs in loop configurations to switch out data bits temporally separated by 4ps (corresponding to 250 Gbit/s) at a 100 MHz clock rate [10]. This type of devices is often referred to as a TOAD (Terahertz Optical Asymmetric Demultiplexer) or SLALOM (Semiconductor Laser Amplifier Loop Optical Mirror). In

Section 4, all-optical demultiplexing techniques are addressed.

Generally, Optical packet compression and decompression techniques allow the design of high-speed packet switched OTDM networks. Packets arriving at a lower bit-rate at the transmitting node have to be compressed in time (when necessary also in pulse width) and decompressed at the other end (at the receiving node). A sampling module can be used for changing the width of signals, while different methods addressed in Section 5 can be used for compression in time, i.e. bit-rate up and down conversion.

A header recognition unit can also be realized in optics. All-optical header recognition allows ultrafast header processing on the fly without need for O/E conversion. Thereby, the header-processing latency can be reduced to a few nanoseconds or even below 1ns. However, there are some restrictions concerning header length and processing complexity.

- **Implementation of the slower MAC-protocol functions**

As shown in Fig. 5 decrease of processing speed is achieved by increase of parallelism. High-speed medium data-rate can be down-converted to the lower data rate by the use of high-speed MAC-protocol functions such as optical packet compression/ decompression or OTDM multiplexing/demultiplexing. *Slower MAC-protocol functions* that need not to be processed on the fly can be realized in electronics and partly in software. Such functions are counters, timers, reading and updating of state vectors, rate control, memory management, creating and updating of traffic matrix, computation of minimum/maximum values etc. An optimal trade-off between hardware- and software-implementation must be obtained. For dedicated hardware entities, the PLDs (Programmable Logic Devices) can be used. If large aggregate bandwidths and higher processing speeds associated with high interconnection requirements are needed, an optoelectronic FPGA (Field-Programmable Gate Array) can be used [11]. Of course, implementation in hardware is favorable when costs and complexity are not the limitation factors.

- **Implementation of the higher-layer functions and high-end users**

Higher protocol layers usually have to be implemented in a dedicated protocol processor. Protocol units that execute functions of higher layers can be programmed in microcode. By designing the appropriate microprogram, enabling functions and event actions, it is possible to implement layer bypassing. Thereby, a separate processing path that involves only a small subset of the complete protocol can be identified and optimised resulting in a so-called *fast path*. PDUs (protocol data units) transmitted or received on the fast path are treated differently by pieces of code/hardware designed especially for this purpose resulting in an additional performance gain.

High-end users such as supercomputers, video-databases, cluster computing, etc. require a large communication bandwidth for supporting high performance applications. Multiprocessor architectures are the logical way to reach a performance level not accessible with a monoprocessor machine. Today, processors run at 1 GHz [12] and issue as many as 4 instructions/cycle. The performance of microprocessors has increased much more rapidly than that of memory systems. Therefore, the most critical and prevailing issue in stored program computer architectures is the memory-access latency (MAL). Moreover, in high-connected multiprocessor architectures with a distributed shared memory concept, the interconnection (network) latency can also be a severe limitation factor. Top-of-the range supercomputers use more than 1000 processors. In such systems, interprocessor connections must provide in minimum Gbit/s range bandwidth per link and average access times to shared data in the nanosecond range. Optical interconnects can be justified for this purpose offering a multitude of advantages over their electrical equivalent (e.g. larger bandwidth, lower losses, larger interconnection distances, no electromagnetic interference, galvanic isolation, etc.).

3. SHORT PULSE SOURCES AND ALL-OPTICAL CLOCK RECOVERY

The requirements on the optical clock sources for OTDM systems is to generate pulses in the ps range close to the transform limit with at least a few gigahertz repetition rate. It can be achieved with an *External Cavity Mode-Locked Laser*, *Fiber Mode-Locked Laser* and *Gain- Switched Distributed Feedback (DFB) Laser.*

The main principle of *Mode-Locked Laser* (MLL) is multi-mode lasing with definite phase relation between all modes. This can be achieved actively, by modulating the gain, or passively, by modulating the loss of the laser cavity. All equidistantly spaced modes with locked phase relations between them by using simple Fourier analysis will give a periodic pulse train whose repetition frequency equals the frequency spacing of the existing modes in the laser cavity:

$$\Delta f = \frac{c}{2Ln_g}$$

where c is the light velocity, L the cavity length, and n_g the group index of the waveguide. Mode spacing of a conventional laser is a few hundred GHz and an external cavity is added to reduce this frequency. It has to be reduced since the frequency of the electrical signal used to modulate the gain of the active region is limited. Gain-modulation of the active region causes the side bands on each mode in the frequency domain. The next requirement is that those side bands coincide with the neighboring longitudinal modes and there will be energy

exchange between each adjacent pair of longitudinal modes, which will force them all to lock in phase.

Passive mode locking can be achieved adding a saturable absorber in the laser cavity. Absorption of a saturable absorber is given as:

$$\alpha(I) = \frac{\alpha_0}{1 + \frac{I}{I_S}}$$

where I represents the intensity in the active medium, α_0 is the absorption for I=0, and I_s denotes the saturation intensity. For I=I_s the absorption is $\alpha_0/2$. When a medium inside the cavity is excited to a sufficiently high level, the electromagnetic field intensity in the cavity increases and after a while saturates the absorber. The output power is increasing after the saturation of the absorber ($I > I_s$, $\alpha \approx 0$) and this leads to the saturation of the gain and the electromagnetic field intensity is decreasing. Before the amplifying medium goes out of the saturation the output intensity is decreased to almost zero. The whole process repeats itself and leads to a passively modulated loss inside the active medium. The difference between both mode-locking types is that there is no need for externally driving the injection current in the passive case, but the time moment where the minimum loss in the cavity occurs is determined by the system.

However, a saturable absorber is used also for shaping and shortening the pulses [13] when the laser is actively mode-locked and driven by the electrical signal, as illustrated in Fig 6.

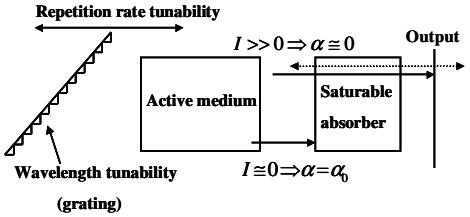

Fig.6: Repetition rate and wavelength tunable MLL with saturable absorber.

In this case, the bias current has to be under the threshold to get active mode-locking. Adding the fast saturable absorber increases significantly the threshold current. It is desirable to have wavelength tunability and this is achieved by adding a grating behind the external cavity. Moving the grating along the cavity changes the effective length of the cavity and the tunability of the repetition frequency is achieved. MLL generates picosecond transform limited pulses with low timing jitter. Wavelength and repetition rate (up to 20 GHz) tunable devices with pulse width lower than 1ps are already on the market [14], and pulses with only 180 fs width are demonstrated in the laboratory [13]. Repetition rates of 43.5 GHz using an integrated electroabsorption modulator as active mode locker [15] is demonstrated. The result is 4 ps pulses with positive chirp.

One more way to perform the gain-modulation is by injecting the pulse train from the other laser. In this case, the relaxation time of the population inversion has to be fast enough ($2Ln_g/c$), so that the gain can be appropriately modulated. This method is used for *all-optical clock recovery*. The pulses are synchronized to the original clock-phase of the data signal and can be used to control the all-optical demultiplexer. In the case of the laser with saturable absorber inside the cavity, it should be passively mode-locked and the bias current should be held above the threshold with no RF power applied [16]. These pulses can be 1000 times shorter [17] than the injected pulses.

A fiber loop can be used as a laser cavity. Erbium doped fiber can amplify the pulse and has a relatively broad bandwidth (≈ 40nm), which enables them to produce pulses narrower than 1 ps [18] in the commercially important telecommunication window around 1550 nm.

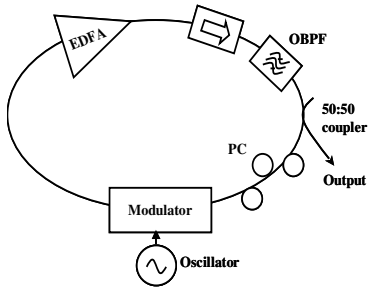

Fig.7: Fiber mode locked laser with active mode locking

Passively mode-locked lasers where just one pulse is circulating in the fiber resonator give the shortest pulse, but the repetition rate is too low here. A modulator (e.g., electroabsorption modulator) is used to synchronize more pulses in the loop and this is called harmonic mode locking (Fig. 7). If the neighboring modes are not locked together, but modes with a distance that is a harmonic of the round-trip period, these locked modes are building an intensity pattern with more than one position where constructive interference takes place. The number of the harmonics corresponds to the number of pulses in the cavity. Therefore, the RF repetition rate of the modulator is increased to a multiple of the round-trip period ($m \cdot c/2L$).

DFB lasers can be used to produce short pulses as well. The most simple and ideal way would be direct-pulsed RF modulation of the laser but it is difficult to realize it at high repetition rates. Gain-switching is used where a relatively strong sinusoidal electrical signal serves as a driving signal. Timing jitter is a major problem when RF signal is below the threshold during the modulation process, due to the stochastic nature of the spontaneous emission. If the laser is driven above the threshold the extinction ratio is low, and a trade-off between these two parameters is the operating point at the threshold current. Due to the self-phase modulation, negative chirp is prevalent. The rising pulse slope is causing decrease in carrier density due to the saturation. Carrier density decrease changes the refractive index inside the cavity and self-phase modulation occurs. The corresponding transmitter chirp can be utilized for pulse compression. The compressed pulses will cause strong dispersion effects during the transmission. By using a

chirped Bragg fiber, broadband dispersion compensation is achieved. Using passive and dispersive Q-switching, where one section of the laser serves as saturable absorber and dispersive reflector respectively, self-pulsations and clock recovery are feasible.

4. OTDM DEMULTIPLEXING

In principle, all optical demultiplexing uses nonlinearities in fiber and in a SOA to perform switching. Because of the long fiber length required, fibre devices are not practical. Nonlinearities used in SOA are FWM and Cross Phase Modulation (XPM). FWM has inherently very high operation speed because intraband dynamics is utilized, but the set up is quite complicated. Intraband dynamics is associated with carrier density modulation. SOA-based devices use XPM where high-power control pulses change the refractive index inside the SOA. Such devices are Ultrafast Nonlinear Interferometer (UNI), Terahertz Optical Asymmetric Demultiplexer (TOAD), Mach-Zehnder Interferometer (MZI).

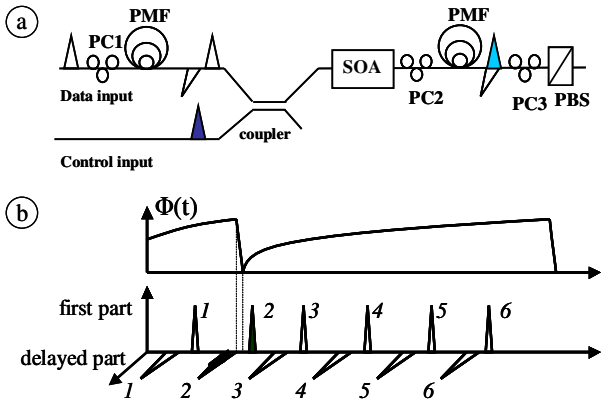

Fig. 8: a) Ultrafast nonlinear interferometer, b) phase change inside the SOA

UNI uses the birefringent characteristic of Polarization Maintaining Fiber (PMF) to split pulses into two orthogonally-polarized parts. This is achieved by using a Polarization Controller PC1 as depicted in Fig 8 a). Due to the propagation through the PMF, one pulse is delayed. The delay is proportional to the fiber birefringence and length. After that, polarization is changed with PC2 so that the slow part of the pulse propagates through the fast axes and the first arriving pulse propagates through the slow axes. At the output of the device, they will arrive at the same time as one pulse. When the first part of the pulse (that is going to be demultiplexed) passed the SOA, a control signal is launched and it changes the refractive index and induces gain-nonlinearities. Launching the control pulse at the SOA after the first and before the second part of the splitted pulse the phase of the second part of the pulse will be changed and thus also modify the polarization of the output signal. The phase is changed immediately, but the recovery time is relatively slow. All other pulses will experience the same phase shift for both parts and will have different polarization than the switched pulses at the output. Optical demultiplexing with data rates in excess of 100Gbit/s is demonstrated [19].

Besides using polarization, the pulse can be also splitted using 3 dB couplers in a loop device like TOAD (Fig. 9). Each pulse is splitted into equal clockwise and counterclockwise parts, which counterpropagate around the loop. The switching window is determined by the asymmetry of the SOA position in the loop. The SOA is not placed in the midpoint of the loop, but with a small offset which forces the splitted pulses to arrive at different times at the SOA.

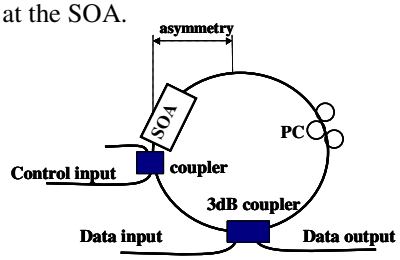

Fig. 9: TOAD

The basic concept of loop devices can be extended to other interferometers like MZI (Fig. 10). The difference is that a pulse after being splitting this time travels through two different MZI arms. This configuration is less stable to the environment (temperature) and two SOAs are needed. Advantages are that it facilitates add/drop multiplexing and has two outputs for selected and unselected pulses which makes them easy to cascade. With hybrid-integrated symmetric MZI 168 to 10.5 Gbit/s demultiplexing is achieved [9].

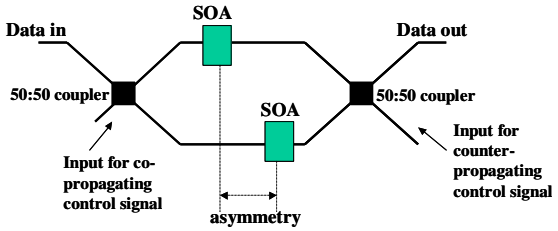

Fig. 10. Mach-Zehnder interferometer

5. OPTICAL PACKET COMPRESSION/DECOMPRESSION

In OPC-TDM networks, rate conversion of ultra high-speed optical data streams to lower rate data streams that can be detected, saved and processed electronically is essential. On the other hand, low bit-rate packet from the transmitting queue must be up-converted to the high medium data rate for inserting into the network. Those rate conversions can be achieved by using the optical packet compression/decompression method.

Recently, several methods for optical rate conversion (compression and decompression) have been

proposed [20,21,22]. Most of these optical rate conversion schemes are based on an optical buffer (optical storage loop) and a sampling technique.

The optical packet compression scheme proposed in [22] is based on the idea of so-called rational harmonic mode locking. Fig. 11 (a) depicts the packet compression unit. The low-speed packet is sampled by the sampling module using FWM in SOA and then enters the storage ring through the coupler. The relation between the fundamental frequency of the storage ring f_0, the sampling clock frequency f_1, and the target high bit-rate f_2 is as follows:

$$f_2 = mf_1 = (mh - 1)f_0$$

where m represents the required number of round-trips in the loop to obtain the desired bit rate and h denotes the number of bits entering the storage loop in each round-trip yielding the packet size mh - 1.

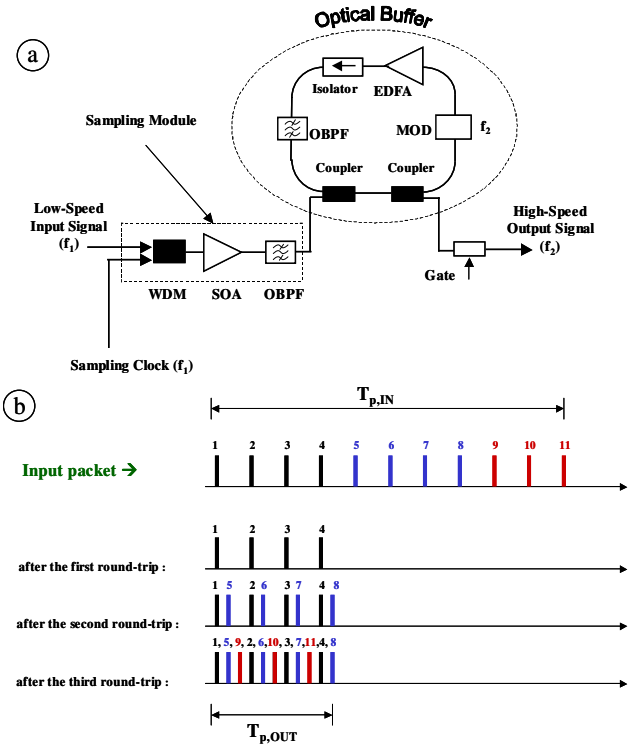

Fig.11: Packet compression unit (a) and timing chart of the compression operation of an 11-bit packet (b).

The principle of the optical packet compressor depicted in Fig. 11 (a) can be illustrated in an example shown in Fig. 11 (b). For simplicity, $m=3$, $h=4$, and the packet length in bits $mh - 1 = 11$ are chosen. In the first round trip, four bits enter the storage ring. The bits numbers 5 to 8 are written into to ring after the bits numbers 1 to 4 completes a round trip. They follow the first four bits by a bit period $1/f_2$ (the bit period of the compressed high-speed packet) because of $f_1/f_0 = h - 1/m$. After the second round trip, there are eight pulses in the ring, and the remaining three bits can be written into the ring also shifted by a bit period $1/f_2$. After the third round trip, the whole packet is compressed and can be read out through the gate. The process for the optical packet de-compression is the inverse. The compressed packet enters the storage ring through the gate, and the sampling module reads it out by sampling of four bits in each round trip at the low-speed bit rate (f_1). In the third round trip, the remaining three bits (9 to 11) are read out. At this time, the whole packet is decompressed.

However, there are some restrictions concerning bit-rate and packet size if above introduced technique is used. It is difficult to store ultrahigh-speed large optical packets for a larger period because of the optical signal impairing caused by dispersion and ASE noise accumulation during amplification. Nevertheless, J.D.Moores reports on a storage of 80 Gbit/s 9-kbit packets for over 30 seconds [23], and predicts that using optical modulation, the operating rates of these fiber loop memories may be extended to 100 Gbit/s.

A further technique for optical packet compression is a feed-forward delay-line structure consisting of $n=log_2(N)$ stages (N = packet length) [24]. The packet compression/decompression using a feed-forward delay line structure, a $LiNbO_3$ modulator and an OTDM demultiplexer for decompression is shown in Fig. 12.

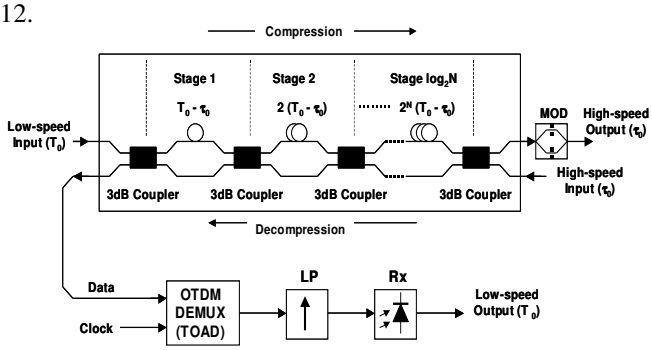

Fig.12: Packet compression/decompression using an optical delay line lattice.

The operation of the device can be explained as follows. The low-speed incoming pulse stream enters the device at the low-speed input (bit period T_0). At the output (bit period τ_0), each pulse is N times copied with an interpulse spacing of (T_0 - τ_0) seconds. For easier understanding of the principle, in Fig. 13, a two-stage optical delay line structure along with its timing diagrams for the 4-bit packet compression and decompression are shown. Timing charts in the different points of the schematics are shown in Fig. 13 (a and b). At the output (point 5, Fig. 13 (b)), each input pulse is four times copied and spaced from its neighbour by T_0 - τ_0. It is able to select the complete compressed packet by placing a modulator at the output of the delay line structure. The fully compressed packet occurs only between the third and the fourth input packet bits, so that the modulator with gating functionality can select it. Decompression occurs in the reverse direction of the same device. The high-speed optical packet enters the device at the high-speed input port. In Fig. 13 (c), decompression of the 4-bit packet is shown. As illustrated by the signal at the point 1, the delay lines create four replicas of the input

packet. Each copy is delayed with respect to the next copy of the packet by T_0 - τ_0. An ultrafast OTDM demultiplexer selects by the very narrow switching window bits spaced at the bit period T_0. The decompressed low-speed output signal has the same bit pattern sequence as the compressed packet. The data and clock signals at the input ports of the TOAD are orthogonally polarized. Consequently, a linear polarizer (LP) must be used to separate the data signal from the clock at the low-speed output port.

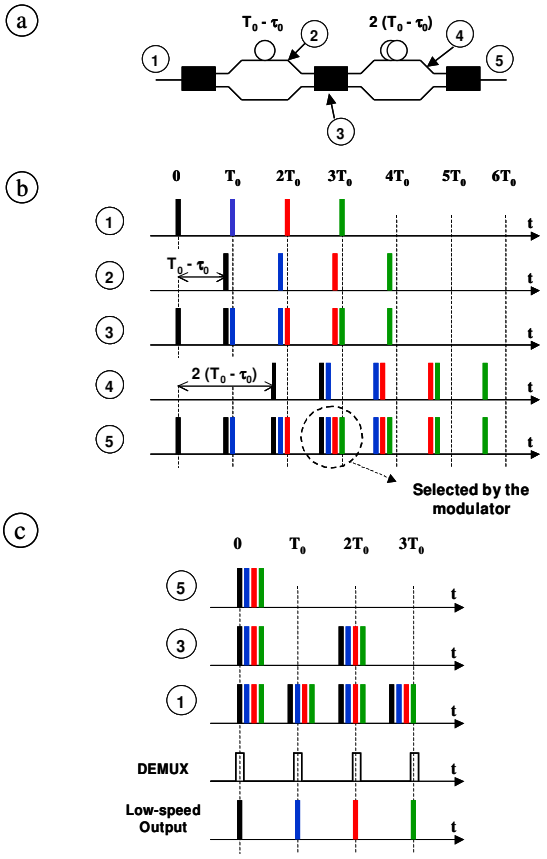

Fig.13: Schematic of a two-stage optical delay line lattice (a) using to illustrate optical packet compression (b) and decompression (c) of a 4-bit packet. T_0 is the bit period of the uncompressed packet and τ_0 is the bit period of the compressed packet.

Optical packet compression/decompression method employing optical delay line lattice is simple to build. It allows the compression of packets to be transmitted simultaneously with decompressing received packets using the same device. The number of delay stages increases logarithmically with the number of bits to be processed. For larger packet lengths the splitting losses (3dB per coupler - in Fig. 13 not depicted) must be compensated with optical amplifier stages. However, the maximal packet size ($L_{p,max}$) is limited by the rate-conversion coefficient K as follows:

$$L_{p,\max} \le K - 1 \quad ; \quad K = \frac{T_0}{\tau_0}$$

Consequently, for 1:100 compression ($K=100$) the $L_{p,max}$ is limited to 99 bits (when neglecting the pulse width). Such short packets are usually impractical in many applications. If larger packet sizes are needed, a larger rate-conversion coefficient or a parallel arrangement of delay lines can be used.

6. ULTRA HIGH-SPEED ELECTRONICS AND PROCESSING SYSTEMS

Increasing of channel data rates in WDM and OTDM systems can also be achieved electrically. Recently, electrical parallel/serial conversions (electrical TDM multiplexing/demultiplexing) up to 40 Gbit/s have been reported [25,26]. The fundamental components for high-speed digital integrated circuits (ICs) with decision, multiplexing, and demultiplexing functionalities are D-flip-flops. Last years, different high-speed electronic ICs for optical fiber communication systems have been developed using various technologies. The most used technologies are: Si-bipolar, GaAs MESFET (Metal Semiconductor Field Effect Transistor), SiGe HBT (Heterojunction Bipolar Transistor), GaAs HBT, InP HBT, and InP HEMT (High Electron Mobility Transistor). Table 1 summarizes the performances of the fabricated ICs concerning operation speed.

Table 1: High-speed electronic technologies

Technol. / IC	Bipolar	FET/HEMT		HBT		
	Si	GaAs	InP	SiGe	GaAs	InP
Decision	25 Gbit/s	40 Gbit/s	50 Gbit/s	40 Gbit/s	40 Gbit/s	---
MUX	40 Gbit/s	45 Gbit/s	70 Gbit/s	40 Gbit/s	40 Gbit/s	40 Gbit/s
DEMUX	40 Gbit/s	---	40 Gbit/s	---	30 Gbit/s	---

InP-based high electron mobility transistors (HEMTs) can potentially offer the highest speed performance. They provide a record f_{max} (maximum oscillation frequency) of 500 GHz and f_T (current-gain cut-off frequency) of 300 GHz [27]. The speed of the conventional D-flip-flops is limited to around one fifth to one fourth of the f_T for FETs. Consequently, using InP-based HEMTs a 70 Gbit/s D-flip-flop could be feasible. HEMTs consisting on the InAlAs/InGaAs structure on a InP substrate have grown to be uniform devices, which can be applied to wide variety of ICs for millimeter-wave and optical fiber communication systems.

Reduced lithography feature size, increased die size, more efficient micro architectures, and better design automation tools have generally driven the growth of the semiconductor technology. Today, commercially available processors are manufactured using 0.18-micron process technology and run at nearly 1 GHz (on-chip clock) [12]. The off-chip clock increases in frequency much slower and will require redesigned I/O drivers, assuming shorter inter-chip wiring or use of optical interconnects, to achieve the increase in frequency. At

present, commercially available DRAMs (Dynamic Random Access Memories), containing 1 Gbit per chip [28], are manufactured in 0.13-micron technology. The memory access time is still too large resulting in high MAL values.

ASICs (Application Specific Integrated Circuits) devices play an important role in user-specific designed circuits. ASIC devices allow so-called system-on-a-chip design. The design of such a system-on-a-chip is being made practical by improvements in megafunctions, programmable interconnects, and CAE simulation tools. Future improvements in ASIC technology, being researched by IBM, TI, NEC, and others, are based on sub-tenth-micron feature sizes. Fig. 14 summarizes the ASIC feature size trend.

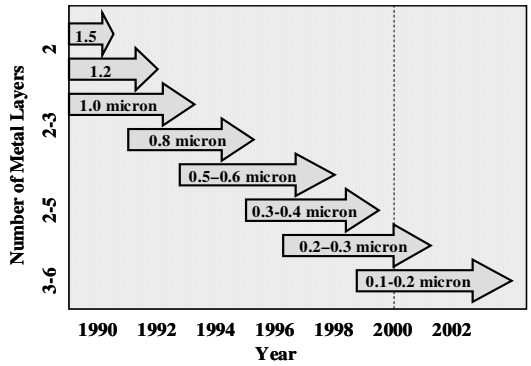

Fig.14: ASIC feature size trend.

PLDs (Programmable Logic Devices) have the advantage that they are customizable by the user in the laboratory or field. FPGAs and CPLDs (Complex Programmable Logic Device) are most common in use. The commercially available PLDs incorporate 50 million transistors and up to 500.000 system gates using a 0.25-micron CMOS process with dual-gate oxide and five metal layers [29]. Moreover, using a 0.18-micron process technology with 2.2 and 1.8 core voltages, densities up to 1.52 million gates are achieved [30].

7. OPTICAL INTERCONNECTS (OIs)

Electrically-controlled optical modulators based on effects in quantum well structure including the family of devices known as self-electrooptic-effect devices (SEEDs) [31] as well as development of vertical cavity surface emitting lasers (VCSELs) [32] offer optoelectronic output devices for fabrication in large numbers of arrays. The demonstration of the integration of thousands of quantum well modulators and photodetectors to silicon logic chips shows that optics might be feasible approach to dense interconnection to the chip [33].

The insertion of OIs into high performance computing systems results in a number of advantages that favors optical technologies. Some of these arguments are e.g. extremely high bandwidth, noise immunity and security provided by galvanic isolation between interconnected subsystems, and potentially higher interconnect density. The one area in which optics can have advantages over electronics in terms of interconnection busses in a network-based parallel computer with distributed-shared memory architecture, as found in *supercomputers*. Thereby, the OIs can minimize the latency of the network-based memory access by providing of both high bit-rates and high pin-outs. Moreover, the implementation of a ring-structured backplane in optics makes it possible to achieve a very large bandwidth (on the order of Tbit/s for highly parallel links).

OIs may have an important role in *reconfigurable architectures* and in *dedicated optoelectronic processors*. In FPGA arrays, the introduction of a new routing layer can essentially increase its processing speed. A three-dimensional (3-D) field-programmable system that uses islands of conventional electronic FPGAs arranged in planes and interconnected with optical light-emitting diodes was proposed [34]. The optical interconnections between electronic FPGAs can be established by the use of a standard optical imaging system [35], a parallel fiber-ribbon [11], guided wave or holographic optical interconnects [36]. The optical hardware needs to be further miniaturized and to be made commercially compliant, especially in terms of connections to the outside world.

8. CONCLUSIONS

In conclusion, new technologies will allow the design of ultra high-speed photonic networks that can provide a high capacity for the NGI. OTDM networks are particularly addressed in this paper. A medium access node design strategy including all-optical techniques for achieving ultra high data rates are analyzed and discussed. The new trends in high-speed electronics, processing systems and optical interconnects are briefly reviewed. Approaches towards all-optical techniques contribute to a better utilization of transmission capacity of optical fibers. This work gives an overview on new technologies in high-speed optical communications, and its effective use in a medium access node design.

Acknowledgement

This work is supported by the Austrian FWF (*Fonds zur Förderung der wissenschaftlichen Forschung*) under contract P13144-INF.

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