37 UMTS link-level demonstrations with smart antennas

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With the exploration of multiple antennas at transmitter and possibly also at receiver end, the original concept of UMTS (universal mobile telecommunications system), specified within 3GPP (3rd-generation partnership project), needs to be reconsidered. While the so-called MIMO (multiple-input multiple-output) techniques promise huge improvements in spectral efficiency, in general, once constraints by standards are specified, it can become quite cumbersome to achieve such improvements. The success of MIMO techniques in UMTS depends on the availability of technically feasible and affordable solutions. The terminal side needs special attention due to its limitations in computational and battery power. In general, MIMO algorithms are rather complex, making their implementation as FPGA or ASIC difficult. Therefore, low-complexity solutions for MIMO systems attract more and more attention.

In this chapter, steps towards integrated circuit solutions for MIMO systems are reported. The discussion starts with a review of a state-of-the-art UMTS SISO (single-input single-output) mobile terminal in Section 37.1. RF (radio frequency) as well as baseband signal processing challenges and requirements are addressed. Furthermore, principle RFIC (radio frequency integrated circuit) and baseband chip architectures, with particular regard to the RAKE receiver, are discussed. In Section 37.2 the SISO RAKE concept is extended to the SIMO (single-input multiple-output) case, which is especially of interest for the uplink. Space-time (ST) RAKE receivers for UMTS base stations (node B) are presented. General MIMO system considerations covering RF aspects as well as baseband MIMO decoding techniques, including their implementation constraints, are highlighted in Section 37.3. In addition, insight in the complexity of MIMO decoding algorithms is provided. First realizations of UMTS MIMO prototypes and even ASICs are reported on in Section 37.4.

37.1. SISO UMTS receiver review

In this section, we review the principle architecture of a UMTS standard Release 4 [1] compliant mobile terminal. For a more detailed structure of a node B UMTS

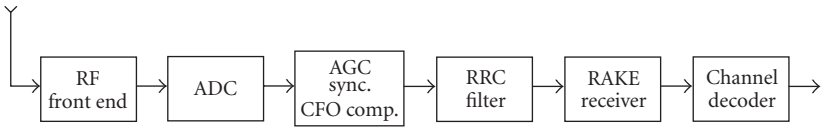

Figure 37.1. Receiver structure for mobile terminal.

receiver, we refer to [2]. The receiver structure for a UMTS mobile terminal is shown in Figure 37.1. After passing the RF front end and the ADC (analog-to-digital converter), the digital signal processing starts with a synchronization phase including AGC (automatic gain control) and CFO (carrier frequency offset) compensation. Subsequently, the signal is processed by an RRC (root raised cosine) filter, which results in an overall RC (raised cosine) pulse shape of the received symbols, since the transmit pulse shaping filter has also an RRC response. The actual data detection is performed by a RAKE receiver followed by the channel decoder. This chapter focuses on the RF front end on the one hand, and on the crucial data detection algorithms and architectures, for example, the RAKE receiver, on the other hand.

Compared to GSM (global system for mobile communications) compliant solutions, the development of UMTS RF chipsets results in some new challenges. Obviously, the higher channel bandwidth of UMTS influences the RFIC design. Beyond that, there are some other critical points that clearly distinguish UMTS from GSM in terms of RF requirements. Both, transmitter and receiver have to fulfill much tighter dynamic range demands. Moreover, the higher ACS (adjacent channel-selectivity) requirements aggravate the receiver design. The transmitter architecture is mainly influenced by the large peak-to-average power ratio (PAR) and the tighter requirements on the output power control. Current solutions use linear power amplifiers to limit RF emissions in neighbouring channels. As a consequence, the power amplifiers have to be operated with adequate backoffs, which results in low PAE (power added efficiency) values. The general tendency in RF transceiver design for wireless communications systems leads towards direct conversion architectures, which do not require costly IF filters, for example, surface acoustic wave (SAW) devices, that are not amenable to monolithic integration (see Section 37.1.2).

By comparison, UMTS is by far the most challenging wireless cellular standard in terms of baseband computational complexity. In [3] it is shown that a GSM, a GPRS, and an EDGE modem requires approximately 100, 350, and 1200 MIPS, respectively. This grows to around 5000 MIPS for a UMTS modem, but a more precise figure depends on the mobility class and the data rate. It is not possible to map the entire set of operations onto a standard, single DSP chip with today's technology. As a consequence, the most complex parts have to be implemented in hardware. These dedicated hardware accelerators are typically supported by a DSP, which handles the less costly tasks. The approximate computational complexity in MIPS for the different functional modules of a UMTS mobile terminal (Release 4)

Table 37.1. MIPS complexity of receiver blocks for 384 kbps class modem.

Digital filtering (RRC, channelization)	2000 MIPS
Searcher (slot and frame synch., code identification)	2500 MIPS
RAKE receiver	850 MIPS
Maximum ratio combining (MRC)	24 MIPS
Channel estimation	12 MIPS
AGC, AFC	10 MIPS
Deinterleaving, rate matching	14 MIPS
Turbo decoding	65 MIPS
Total	5500 MIPS

Table 37.2. RF performance characteristics and related TCs.

Reference sensitivity TC	Noise figure
Adjacent channel selectivity TC	Selectivity
Intermodulation TC	3rd-order intercept point
Maximum input TC	1-dB compression point, tolerable inchannel distortions
Blocking TC	Reciprocal mixing

is shown in Table 37.1. It has to be noted that different mobility classes and data rates result in different complexity.

Interestingly, the bulk of the computational complexity is concentrated in two blocks.

(i) *Digital filtering*. The functions for signal shaping up to the RRC filter are of high computational complexity due to the high sample rate, which is at least twice the chip rate (i.e., 7.68 MHz sample rate).

(ii) *Searcher*. The aim of the cell search module is to detect the slot/frame sequence of the base station among all received signals in order to establish a communication link. In a low SNR environment, the detection probability can be enhanced by retrying this procedure. This increases the processing load until the correct sequence is detected. Hence, this detection is of random nature and its final MIPS count is difficult to estimate.

37.1.1. Basic 3GPP requirements

RF requirements. The requirements for a UMTS-FDD (frequency division duplex) mode compliant RF transceiver can be derived from the testcases (TCs) given in [4]. Almost all receiver related TCs in this document define the required receiver performance indirectly, that is, by stating that under given signal conditions at the terminal antenna connector, a predefined BER (bit error rate) or BLER (block error rate) of a certain value must not be exceeded. The most important receiver TCs together with their related RF performance measures are summarized in Table 37.2.

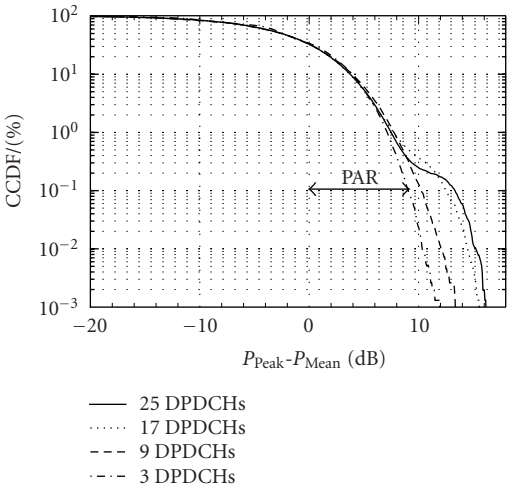

FIGURE 37.2. CCDF for several numbers of DPDCHs including CPICH (common pilot channel), CCPCH (common control physical channel), PICH (paging indicator channel), SCH (synchronization channel).

Most of the RFIC performance figures mentioned in Table 37.2 have to be derived via detailed system simulations, taking into account the RF-receiver architecture and the subsequent digital baseband receiver structure. Requirements that can be estimated by means of simple calculations are rare. One notable exception is the calculation of the receiver noise figure (NF) based on the reference sensitivity-level TC [5]. The impact of limited receiver linearity has been evaluated in [6]. The influence of channel-selection filtering is investigated in [7, 8]. A link between the RF performance measures for sinusoidal signals and for W-CDMA (wideband code division multiple access) signals can be found in [9].

Most of the RF performance figures are defined for sinusoidal signals excitation only. These measures cannot readily be applied for W-CDMA signals due to different signal statistics and bandwidths. Especially important in this context is the PAR, which can be derived from the complementary cumulative probability density function (CCDF). The peak power P_{Peak} for the calculation of the PAR is defined as

$$\text{CCDF}\left(P_{\text{Peak}}\right) = 0.1\%. \tag{37.1}$$

Thus, the instantaneous signal power is lower than the peak signal power P_{Peak} with a 99.9% probability. Figure 37.2 shows the CCDF of a downlink UMTS signal for several numbers of dedicated physical data channels (DPDCHs). Remarkably, the peak power increases substantially for higher numbers of DPDCHs.

Baseband requirements. The main parameters for the physical layer of the UMTS mobile communications system are defined in the standards document [4]. These parameters impose constraints on hardware design aspects such as the processing

speed and the temporary storage of information among others. UMTS is a CDMA system with chip rate $f_c = 3.84$ Mcps leading to a sample rate of at least 7.68 Msps for baseband signal processing. The data frames consist of 15 slots, each one with 2560 chips. The base station transmits a CPICH with a fixed spreading factor (SF) of 256 and identical spreading code to support parameter estimation at the terminal side. The SF for data ranges from 4 to 256.

A low BER can only be achieved, if as much as possible transmit power is received. In a multipath environment, several receive paths with significantly different time delays have to be combined. The UMTS standard [4] defines TCs with channel delays up to 20 microseconds. The RAKE receiver for a UMTS system combines several receive paths into a single output signal. The direction, the intensity, and the arrival time of the received signals change as the user moves. Therefore, the path search window has to be sufficiently large around the peak level. In practice, the observation window spans from -10 microseconds to $+20$ microseconds, which corresponds to the chip positions -40 to $+80$. Furthermore, in *soft handover mode*, the terminal combines the received signal of up to six base stations. In this case, the observation window is extended to ± 38.5 microseconds (equivalent to ± 148 chips).

The dynamic channel properties naturally depend on the mobile's speed. Assuming a mobile moving with 250 kmph results in a path delay change of approximately half a chip duration within 56 frames or 560 milliseconds. This exhibits that the delay estimation rate may be substantially lower than the frame rate.

37.1.2. RF front end

The first step in receiver design is the choice of the receiver architecture. Besides achieving the required RF performance, several criteria like the number of external components, cost, power dissipation, and complexity determine the selected receiver structure. However, as IC technologies evolve, the relative importance of each of these criteria changes, allowing to return to approaches that once seemed impractical as plausible solutions. UMTS compliant RF receivers are quite different from their 2nd-generation TDMA/FDMA (TDMA: time division multiple access, FDMA: frequency division multiple access)-based counterparts, due to the separation of the user signal in the code domain rather than in the time and/or frequency domain. In this section, we will only focus on the two dominant receiver architectures used for cellular terminals, which are the homodyne and the heterodyne receiver structures.

Heterodyne receiver architecture. Figure 37.3 shows the heterodyne receiver structure. This architecture first translates the signal band down to some intermediate frequency (IF), which is usually much lower than the initially received frequency band. Channel-select filtering is usually done at this IF, which requires some bandpass filter with a center frequency equal to the IF. The choice of the IF is a principle consideration in heterodyne receiver design (see Figure 37.4).

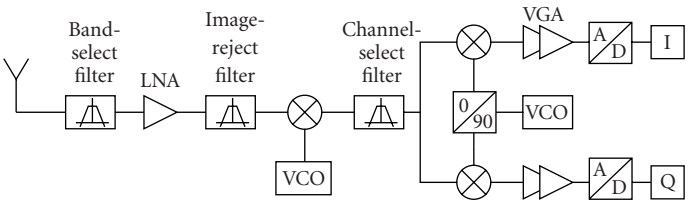

FIGURE 37.3. Heterodyne receiver structure.

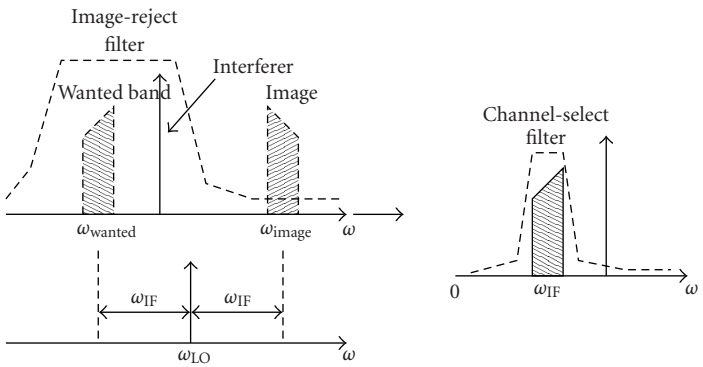

FIGURE 37.4. Image rejection and channel selection for the heterodyne receiver structure.

As the first mixer downconverts frequency bands symmetrically located above and below the local oscillator (LO) to the same center frequency, an image-reject filter in front of the mixer is needed. As depicted in the left part of Figure 37.4, the filter is designed to have a relatively small loss in the desired band and a large attenuation in the image band, two requirements that can be simultaneously met if $2 \cdot \omega_{\text{IF}}$ is sufficiently large. Thus, a large IF relaxes the requirements for the image reject filter, which is placed in front of the mixer (see Figure 37.3). On the other hand it complicates the design of the channel-selection filter (right part of Figure 37.4), because of the higher IF. In today's cellular systems, the channel-selection filtering is normally achieved with external SAW filters, because implementations amenable to monolithic integration like active-RC or $Gm - C$-filters would be too power consuming for the required performance.

An interesting situation arises if an interferer with frequency

$$\frac{\omega_{\text{wanted}} + \omega_{\text{LO}}}{2} \tag{37.2}$$

is present. If this interferer experiences second-order distortion and the LO contains a significant second harmonic, then a component at

$$\left| (\omega_{\text{wanted}} + \omega_{\text{LO}}) - 2\omega_{\text{LO}} \right| = \omega_{\text{IF}} \tag{37.3}$$

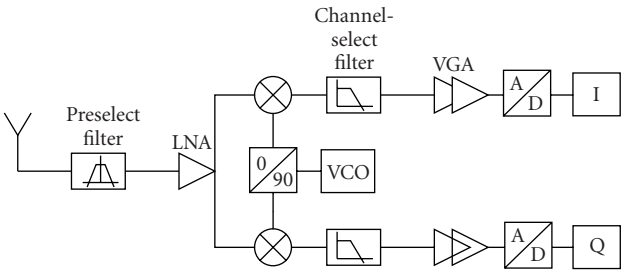

Figure 37.5. Homodyne receiver structure.

arises, which can be extremely troublesome, because this interference source directly occurs in the receive band. Thus, it cannot be removed by filtering in subsequent receiver stages. This phenomenon is called half-IF problem.

Due to the fixed receive bandwidth of the heterodyne receiver structure caused by the external IF-filter, the multimode and multiband capabilities can only be implemented by using separate IF sections for each mode. Clearly, this would result in high costs and a complex receiver structure. One example of an RFIC for UMTS based on this architecture can be found in [10].

Homodyne receiver architecture. The homodyne receiver structure (also called zero-IF or direct-conversion architecture) depicted in Figure 37.5 avoids the disadvantages of the heterodyne concept by reducing the IF to zero. This saves the first mixer, the LO, and the IF channel-selection filter. Moreover, also the image problem vanishes if a quadrature converter is used. Thus, the simplicity of this structure offers two important advantages over its heterodyne counterpart. First, the problem of image is circumvented because ω_{IF} is 0. As a result no image filter is required. This may also simplify the LNA (low noise amplifier) design because there is no need for the LNA to drive a 50Ω load, which is often necessary when dealing with image-rejection filters [11]. Second, the IF SAW filter and IF amplifiers can be replaced by lowpass filters and baseband amplifiers that are amenable to monolithic integration.

The zero-IF or homodyne receiver topology entails a number of issues that do not exist or are not as serious in a heterodyne receiver. Since in a homodyne topology the downconverted band extends to zero frequency, offset voltages can corrupt the signal and, more importantly, saturate the following stages. There are three main possibilities of how DC offsets are generated. First, the isolation between the LO port and the inputs of the mixer and the LNA is not infinite. Therefore, a finite amount of feedthrough from the LO port to the mixer or the LNA input always exists. This "LO leakage" arises from capacitive and substrate coupling and, if the LO signal is provided externally, bond wire couplings. This leakage signal is now mixed with the LO signal, thus producing a DC component at the mixer output. This phenomenon is called "self-mixing." A similar effect occurs if a large interferer leaks from the LNA or mixer input to the LO port and is multiplied by itself.

A time-variant DC offset is generated if the LO leaks to the antenna and is radiated and subsequently reflected from moving objects back to the receiver.

Large amplitude modulated signals that are converted to the baseband section via second-order distortion of the IQ mixers may also lead to time-variant DC offsets. The spectral shape of this signal contains a significant component at DC accounting for approximately 50% of the energy. The rest of the spurious signal extends to twice the signal bandwidth before being downconverted by the second-order nonlinearity of the mixers. The reason for the large signal content at DC is due to the fact that every spectral component of the incident interferer is coherently downconverted with itself to DC. In order to prevent this kind of DC offset, a large second-order intercept point (IP2) of the IQ mixer is necessary.

3GPP compliant receivers approximately need 80 dB gain. Most of this gain is contributed by the baseband amplifiers. That means that even small DC offsets (in the range of several mV) at the mixer outputs may lead to DC levels sufficient to saturate the ADCs.

In TDMA systems, idle time intervals can be used to carry out offset cancellation. This would be a practical solution for the 3GPP-TDD (time division duplex) mode. It cannot be used for offset cancellation in the FDD mode because of the continuous signal reception. Here, the natural solution for DC offset cancellation is highpass filtering. Since the signal band extends from DC to approximately 2 MHz, a high-pass filter with a cutoff frequency of several kHz results in an acceptable degradation of the system performance [12]. This approach is only possible because of the wideband nature of the signal. An interesting solution to overcome the switching transients due to highpass filtering is presented in [13]. A system level DC offset compensation approach can be found in [14].

IQ mismatches are another critical issue for the zero-IF receiver topology. Fortunately, pilot-symbol-assisted channel estimation is performed in W-CDMA systems. Irrespective of the pilot symbols used (either the time-multiplexed pilot symbols or the common pilot signal), this estimation additionally leads to a correction of the IQ phase and amplitude mismatch.

Most of the published work on receiver design is based on the direct conversion topology [15, 16, 17, 18, 19]. This comes at no surprise due to the importance of the highest possible integration, which is clearly advantageous for the zero-IF receiver structure. All these receivers are designed using standard BiCMOS processes. An interesting option is the use of SiGe bipolar technology for the receiver front end [20, 21]. Recent advances in UMTS compliant RFIC receiver design are often focused on the use of RF-CMOS as the semiconductor technology of choice [22, 23].

37.1.3. Baseband receiver architectures—the RAKE receiver

The RAKE receiver as shown in Figure 37.6 combines signal energy arriving from different paths requiring a correlator assigned to each (relevant) propagation path. In the RAKE literature, these correlators are called RAKE fingers. They are parameterized by the positions of the propagation paths in time, such that the code

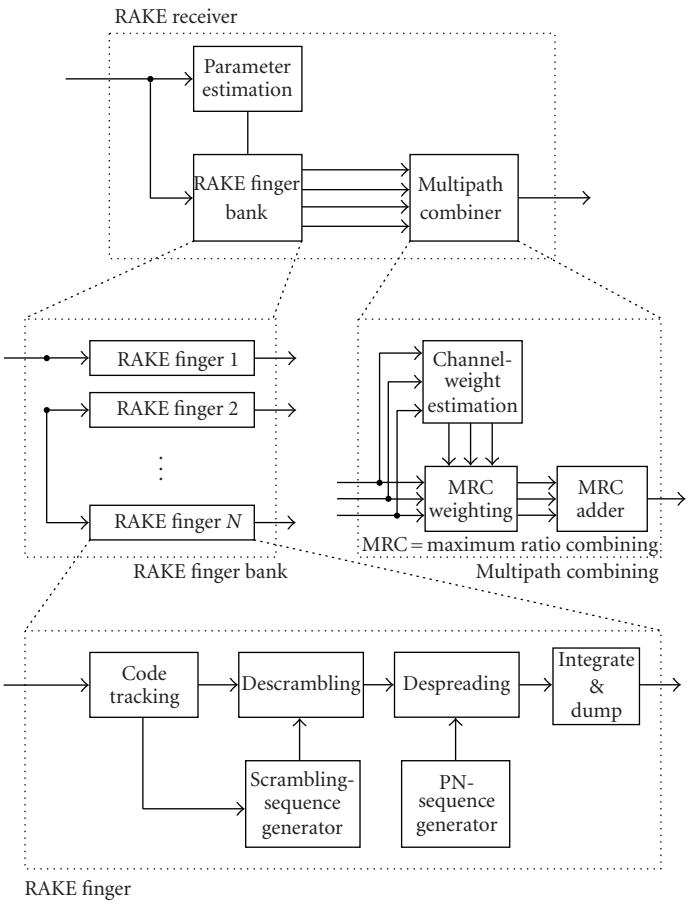

Figure 37.6. Principle structure of a RAKE receiver.

generator for descrambling/despreading runs synchronously to the slot start. The finger outputs are combined to one signal in a maximum ratio combiner.

Typically, the RAKE fingers process samples at twice the chip rate. However, the actual path delay is, in general, not a multiple of half a chip duration. Hence, the analog signal is not sampled at the optimum time. Therefore, a code-tracking unit is used at each finger to reconstruct the input signal for optimum sampling (see Figure 37.7). Each RAKE finger contains a timing error correction (code-tracking unit), a descrambler to distinguish different base stations, a despreader, and an integrate-and-dump operation. The descrambling and despreading codes are generated in respective code generators. The code numbers are available prior to the start of the data demodulation.

The multipath combiner comprises a channel estimation block to estimate the channel weights for each individual path, and an MRC weighting and MRC

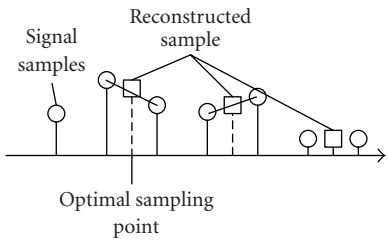

FIGURE 37.7. Reconstruction of the optimal sampling point.

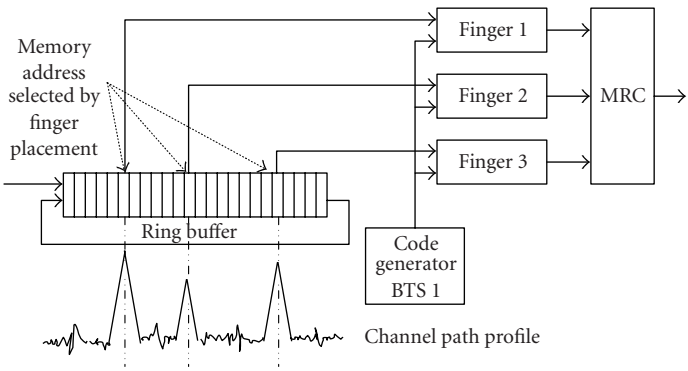

FIGURE 37.8. Input buffer for delay compensation at chip level.

adder block, which combine the received signals according to the maximum ratio criterion.

The RAKE receiver processes the sampled and quantized output signal of the RRC filter. To achieve adequate system performance, a path resolution of $\pm(1/16)T_c$ (with chip duration $T_c = 1/f_c$) is required. This accuracy may either be achieved by using a high oversampling rate (OSR), or by using a low OSR (e.g., the minimum OSR of two) in combination with interpolation methods. The latter case implicates a lower ADC clock rate. The interpolator reconstructs the signal from the received samples, for example, by linear or quadratic interpolation (see Figure 37.7). The code-tracking unit selects the sample closest to the optimal sampling point.

Due to multipath propagation, the signals of different paths arrive with a time difference. In order to combine them coherently, the arrival delays have to be compensated. This can either be performed at chip level, that is, at the input of the RAKE fingers (see Figure 37.8) or at symbol level, that is, at the output of the RAKE fingers (see Figure 37.9). The preferred method depends on the number of fingers, the OSR, as well as the spreading factor.

In the first case, an input buffer is required and the RAKE fingers point at different locations in this buffer. Since data is stored consecutively, there is a unique

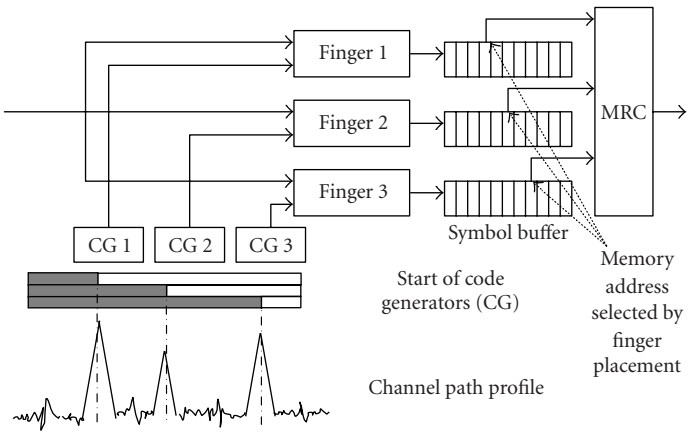

FIGURE 37.9. Output buffer for delay compensation at symbol level.

relation between path delay and memory address. The buffer size is determined by the OSR and the maximum path difference to be covered (see Section 37.1.1). All the RAKE fingers run synchronously, their corresponding code generators start at the same point in time, which simplifies a synchronous design.

In the second case, the path delay is compensated at the output of the RAKE fingers, where the symbols have to be buffered. The multipath combiner selects symbols from these buffers according to their path delays. In this approach, the fingers run asynchronously, therefore the code generators have to be adjusted according to the path delays.

The buffer size for data and control overhead is different for both approaches. The choice depends on the number of fingers and the spreading factor. For comparison, the buffer size is calculated for both cases. The signal is assumed to be complex-valued (IQ = 2), the OSR is set to two, and soft handover mode is assumed. SHO chips are stored and maximum channel delay spread (corresponding to DS chips) has also been taken into account. Considering the requirements discussed in Section 37.1.1, the size of the input buffer (IB, see Figure 37.8) follows to be

$$\begin{aligned} \mathrm{IB} &= \mathrm{IQ} \cdot \mathrm{OSR} \cdot (2 \cdot \mathrm{SHO} + \mathrm{DS}) \\ &= 2 \cdot 2 \cdot (2 \cdot 148 + 120) \text{ samples} \\ &= 1664 \text{ samples}. \end{aligned} \tag{37.4}$$

This amounts to a memory size of around 13 kb for an 8-bit data input.

The second option is to process the input data without prior delay compensation. In this case, a separate code generator is used for each path synchronized to the corresponding path delay. The symbol rate at the output of the fingers is f_c/ SF

with SF ranging from 4 to 256. The size of the output buffer (OB) is given by

$$\begin{aligned} \mathrm{OB} &= \mathrm{IQ} \cdot F \cdot \frac{2 \cdot \mathrm{SHO} + \mathrm{DS}}{\mathrm{SF}} \\ &= 2 \cdot 10 \cdot \frac{2 \cdot 148 + 120}{4} \text{ samples} \\ &= 2080 \text{ samples.} \end{aligned} \tag{37.5}$$

In this estimation, $F = 10$ was assumed. For the chosen parameter set, a 16 kb data memory would be required. The first solution is preferable for a large number of RAKE fingers and a small OSR. An additional problem that arises with the architecture shown in Figure 37.9 occurs when a terminal is moving towards the base station. In this case, the path delay decreases, and the phase of the code generator has to be adjusted accordingly. A solution to this problem applying a one-bit delay line at the output of the code generator is proposed in [24].

37.2. Extensions of SISO RAKE receiver

The RAKE receiver for SISO UMTS discussed in Section 37.1.3 is very effective in optimum combining of multipath components, and thus represents a receiver structure utilizing time diversity (multipath diversity). The use of multiple antennas at the receiver additionally enables to exploit the spatial dimension, that is, it allows for spatial diversity. This section focuses on ST RAKE receivers which are especially interesting for the UMTS uplink because of the obvious facility to apply multiple antennas at the base stations. This system approach illustrates a SIMO extension of the scheme addressed in Section 37.1.2.

In this section, we will present two different approaches of how to exploit the spatial dimension, namely, the MRC-ST RAKE receiver in Section 37.2.1 and the beamforming-ST RAKE receiver in Section 37.2.2.

37.2.1. MRC-space-time RAKE receiver

This straight forward approach combines the outputs of individual temporal RAKE receivers (one for each antenna) in an MRC sense. This scheme [25] (see Figure 37.10), called MRC-ST RAKE, accomplishes diversity by means of temporal and subsequently spatial combining. Note that the order of temporal and spatial combining can also be exchanged without performance degradation.

As it is shown in Figure 37.10, the entire SISO RAKE receiver chain (Figure 37.6) has to be implemented for each antenna. If n_R is the number of receive antennas, the computational complexity of the MRC-ST RAKE is approximately n_R-fold that of a SISO RAKE (see Table 37.1):

$$C_{\text{MRC-ST-RAKE}} \approx n_R \cdot C_{\text{SISO-RAKE}}. \tag{37.6}$$

Due to the close spacing of the receiver antennas, the delays of the dominant temporal taps (RAKE fingers) of the individual channel profiles are strongly correlated.

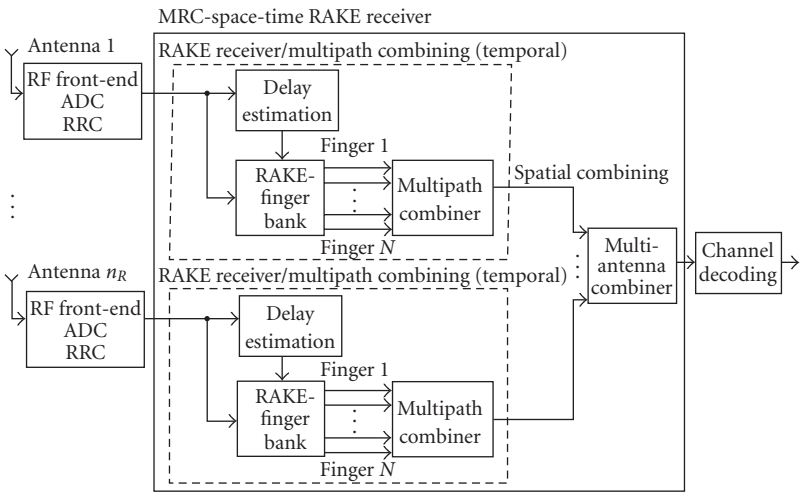

Figure 37.10. MRC-space-time RAKE receiver.

Complexity can therefore essentially be reduced by centralizing the delay estimation block, which does not need to be implemented for each branch individually. Since the delay estimation is the most complex part in the RAKE receiver (see Table 37.1), this may reduce the overall complexity of the MRC-ST RAKE significantly.

37.2.2. Beamforming-space-time RAKE receiver

The use of multiple antennas enables to exploit the spatial diversity of the channel and, in addition, to reduce the effects of multiuser interference (MUI) by the use of beamforming. Figure 37.11 shows the block diagram of a beamforming-ST RAKE receiver. Here, spatial beamforming is implemented for each path (i.e., for each RAKE finger), followed by a temporal RAKE combiner. Each spatial beamforming operation (one beamforming for each temporal path) is implemented by applying a spatial weight vector to the n_R antenna signals. The position of each RAKE finger in turn is determined by the delay estimation block.

Applying the spatial weight vectors can be regarded as a beamforming procedure, one for each temporal RAKE finger, which rejects interfering signals of other users. This rejection is achieved by pointing one or more narrow beams at the incoming desired signals. Any one of several beamforming criteria such as minimum mean square error (MMSE) or minimum variance distortionless response (MVDR) may be used to calculate the spatial weight vector. Both MMSE and MVDR require the antenna array covariance matrix and its inverse [2]. A less complex alternative to these beamforming criteria called approximate MVDR is described in [26].

Note that the multipath combiner block in Figure 37.11 not only consists of the MRC weighting and adder parts, but also comprises an estimation block for

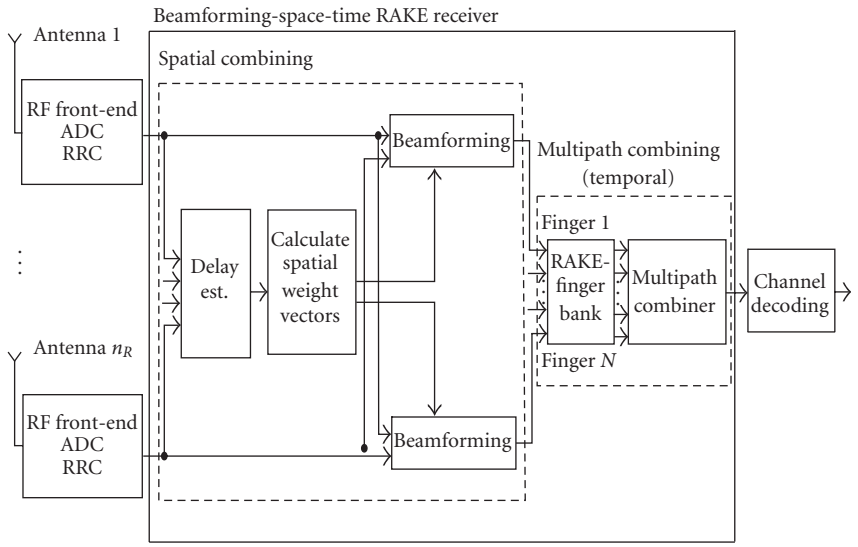

Figure 37.11. Beamforming-space-time RAKE receiver.

determining the weights of the temporal RAKE fingers (see Figure 37.6). These temporal weight vectors should be updated every time slot to track the fast fading, while the spatial weight vectors can be averaged over several slots since the spatial characteristics change much slower than the fast fading.

In rural environments (i.e., high spatial correlations), the beamforming-ST RAKE typically outperforms the MRC-ST RAKE, because it directs its beams towards the strongest incoming signal (dominant eigenvector). On the other hand, in the so-called pico-environments (low spatial correlation), the MRC-ST RAKE typically outperforms the beamforming-ST RAKE, since in that case the beamforming-ST RAKE is hardly able to exploit spatial diversity (only the strongest eigenvector which represents only a small part of the corresponding path is exploited) [25, 27].

In [25] the idea of ST RAKE receivers is furthermore extended to closed loop diversity schemes, on the W-CDMA downlink. In such schemes parts of the complexity and multiple antenna processing are shifted to the base station where the transmit signals are predistorted. Note that the predistortion requires channel state information, therefore a feedback channel is needed. For further improvements on ST RAKE receiver concepts (eigen-RAKE, joint-ST RAKE) and performance comparison demonstrations, we refer to [25, 27].

37.3. MIMO system architectures

Most of the published work in the MIMO field focuses on the algorithmic parts and on their respective implementations in the digital domain. There is only little work available that specifically takes MIMO compliant RF front ends into account.

In Section 37.3.1, the principle conceivable MIMO RF receiver architectures are discussed. In Section 37.3.2, MIMO baseband algorithms are considered and their complexity is evaluated.

37.3.1. RF front end

Basic work on MIMO RF receiver architectures is reported in [28, 29]. One of the obvious challenges in MIMO optimized RF front-end design is the separation of the antennas. Obviously, small-sized mobile terminals fit poorly for multiantenna implementations. To properly implement multiple antennas into a small terminal, a minimum distance of half the wavelength λ could be taken as a rule of thumb to sufficiently decouple the antennas. Further decoupling can be realized by using cross-polarized antennas. At 2 GHz carrier frequency, $\lambda/2$ corresponds to 7.5 cm. Therefore, the size limitations of cellular terminals set a natural limit on the respective number of implemented antennas.

The straight forward approach of a MIMO capable RF front-end implementation is the use of one dedicated receiver per antenna to preserve the spatial and temporal integrity of the antennas signals. This structure is called a full-parallel MIMO RF receiver. In principle, it is also possible to separate the received signals from different antennas in the analog front end in the time, frequency, or code domain. All of the mentioned techniques have their distinct advantages and shortcomings. At least the separation in frequency and time does not seem to be an option for a highly integrated RFIC due to inherent technical problems.

Frequency-domain-multiplexed MIMO RF receiver. In this approach, the received signals from different antennas would typically be mixed onto different frequency bands. Obviously, each receive path requires separate LOs and mixers, but the analog IF or baseband section and the subsequent ADCs could be shared. The resulting frequency bands should be as close as possible, that is, one channel spacing of the standard under consideration. There are however some severe disadvantages inherent to this concept. All the problems common to the design of heterodyne receivers would aggrevate for such frequency-domain-multiplexed MIMO receiver. Trying to implement this receiver structure on a single RFIC could prove to be impractical due to frequency planning issues taking into account the number of different frequency sources needed. Furthermore, filtering requirements would be hard to realize.

Time-domain-multiplexed MIMO RF receiver. In the time-multiplexed approach, the outputs from the different antennas are multiplexed together using an RF switch. The combined signals are subsequently downconverted to baseband by a single radio receiver. Since the sample interval of the received signals at each antenna has to be preserved, the RF switch must operate at $N \cdot S$ (N-number of antennas, S-nominal sampling frequency). One disadvantage of this approach is the fact that only a fraction of the received power that is available at each antenna is actually being used for further processing. From an implementation point of view, this concept seems even more challenging than the frequency-domain-multiplexed RF

receiver described above. Finding suitable RF switches and realizing the demultiplexing operation correctly are just two issues that make this architecture only a theoretical option.

Code-domain-multiplexed MIMO RF receiver. This method uses a code-division approach for the signal separation similar to techniques employed in CDMA systems. A unique identity is assigned to each received antenna signal by application of an orthogonal code (i.e., a Walsh code). Due to the orthogonality of the used codes the combined signals can be separated in the digital domain after they passed through a single RF chain with subsequent ADCs. Biphase modulators can be used to apply the code domain multiplexing in the analog domain.

Full parallel MIMO RF receiver. This approach necessitates one full receiver front end (see Figures 37.3 or 37.5) per antenna. However, it should be noted that important blocks can be shared among the different receivers. The sharable blocks include the frequency generation (VCO, PLL), the IQ divider, the biasing circuitry, and the clock generation functionality. Furthermore, the digital calibration circuits, for example, for the analog channel-selection filters, can be commonly used by all the receiver chains. Consequently, the integration of, for example, two parallel receivers onto one RFIC would not simply result in a doubling of the required die area compared to the single receiver implementation. Thus, the area and power saving potential of an optimized RFIC implementation of a full-parallel MIMO RF receiver might be significant.

From all the mentioned architectures only the full-parallel MIMO RF receiver offers the full benefits of a MIMO system. Due to the severe technical challenges of the frequency- and time-domain multiplexing approaches, only the code-domain multiplexing RF receiver is left as a second potential solution.

37.3.2. Baseband receiver architectures

General MIMO decoder considerations. The actual decoding stage takes place after AGC, RRC filtering, synchronization, and frequency offset compensation have been performed. The decoder comprises from the RAKE receiver correlators for channel estimation (CE), the correlator bank (CB) of selected fingers, the MIMO decoder (M-Dec), and the finger position search and management (FPM) unit as shown in Figure 37.12. The channel estimator is supported by a pilot code generator (PCG), while the correlator bank is supported by separate code generators depending on the user codes. In MIMO transmissions, the linear RAKE combiner is typically replaced by a specific decoder unit that performs ML (maximum likelihood) decoding or matrix inversion techniques, like ZF (zero forcing), MMSE, or V-BLAST (vertical Bell Laboratories Layered Space-Time) [30]. Finally, the control unit (Cntr) converts the timing synchronization into appropriate signals for each block. The channel decoding is done by a turbo decoder (turbo).

The complexity of all these units depends strongly on the channel requirements. For a channel impulse response of 10 microsecond duration, roughly 40 channel taps are required when running a T-spaced receiver. For higher sampling

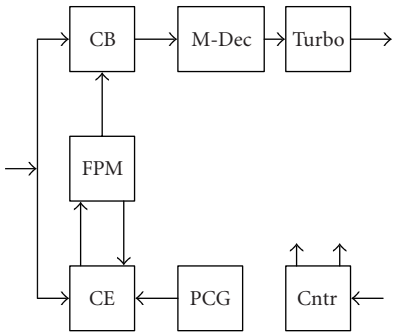

Figure 37.12. Decoder and RAKE structure.

rates, the number increases accordingly. Note that for a MIMO system with n_T transmit and n_R receive antennas, a total number of $n_T n_R$ subchannels need to be estimated. The channel example (10 microsecond impulse response duration) above with four transmit and four receive antennas and an oversampling rate of four, easily ends up in 2560 channel taps to estimate. While this estimation requires 2560 correlator operations, it does not require 2560 correlators working independently. The relative long time duration of 260 nanoseconds between two chips allows to reuse the correlators, that is, to fold the required HW. Also, the several pilot sequences for the antennas do not need to be independent sequences. In [31] a real-time system with four transmit antennas was reported using the secondary pilot channel (SPICH) to transmit four pilot sequences stemming from the same branch of the OVSF (orthogonal variable spreading factor) code tree. This allowed to substantially decrease complexity. In the 3GPP standard document TR 25.869 [32], a four-antenna transmit and receive system is proposed for UMTS Release 6. There, the four transmit antennas are supported by one CPICH signal only, but this signal is split into two patterns (AA) and (−AA) and further split into four different antenna signals by using two different OVSF codes. A low-complex solution for the receiver can also be found in this 3GPP document.

In particular, there will be more than one OVSF code assigned to each user in HSDPA (high-speed downlink packet access) mode (see also proposed 3GPP standard document TR 25.848 [33]). Many complexity reductions are possible [34, 35, 36] since the codes can be grouped into stems from the same branch of the code tree. Higher modulation schemes (16-QAM and 64-QAM) have also been proposed for increased data rates, but at the price of increased complexity for the decoding algorithm.

Further advantages that can be elaborated on are the dynamic channel properties. Due to the Doppler speed, a finger appearing on a certain position will not change its position abruptly. Since radio waves propagate with the speed of light, they travel about 75 m in 260 nanoseconds. Assume a slow mobile moving with 3.6 kmph, or, equivalently, 1 mps. At this speed, it takes 75 seconds or 7500 frames until the finger position moves to the next chip. For a fast mobile moving with

180 kmph, this duration decreases to 1.5 seconds or 150 frames, still a very long time that can be used either for averaging and thus improving estimation quality or can be traded against complexity by assigning only fractions of this period per channel tap estimation. Thus, it is possible to substantially reduce the estimation rate of the channels and at the same time to reduce the HW complexity.

Due to noisy estimation and fast Doppler, the finger energy may vary substantially over time while its position remains constant for a much longer period. In this case, it may be a better strategy to keep the location of the finger fixed even if its observed energy drops below a certain level. While for a short period other locations may appear as better choices, they can easily be mistaken and are of random nature. An intelligent FPM unit is thus required to decide whether a finger position remains unchanged even if the corresponding observed finger energy drops or a new finger location is selected. Measuring the finger energy at a certain finger position requires the computation of a norm of the correlator output signals. This can be performed by a complex-valued multiplication, computing the squared l_2-norm:

$$\|r\|_2^2 = \Re^2\{r\} + \Im^2\{r\}. \tag{37.7}$$

Thus, two multiplications per finger are required. If this is to be reduced in complexity, a good approximation of the nonsquared l_2-norm is given by

$$\|r\|_2 \approx \frac{3}{8}\max\left(|\Re\{r\}|, |\Im\{r\}|\right) + \frac{5}{8}\left(|\Re\{r\}| + |\Im\{r\}|\right), \tag{37.8}$$

which gave excellent results in [31, 34].

Furthermore, the optimal number of fingers is a challenging question. In some wireless channels, many strong reflections appear, while in others such reflections may be so close to each other that their received superposition cannot be resolved as independent paths.

The number of detection fingers allocated to a specific code has to be kept low, since it determines the complexity of the receiver. Thus, an intelligent finger management unit allocates the fingers separately for each code based on the channel estimation and the available resources.

While the classical RAKE receiver linearly combines the signals on the various finger outputs, better methods for MIMO transmissions are available (see Section 37.2 for SIMO extensions and Section 37.3.2 for MIMO extensions of the SISO UMTS system).

Complexity considerations for MIMO decoding algorithms. Decoding algorithm for MIMO transmissions can be divided into two groups: (i) matrix inversion methods and (ii) ML decoding. Since ML decoding is considered the most complex algorithm, it is typically not considered in transmission techniques and only the lower complexity version utilizing suboptimal ML sequence estimation techniques are used instead. However, for QPSK and transmission systems of order 4×4, it has

been shown [34] that an ML implementation can be much cheaper than a BLAST technique, achieving much higher decoding quality. In ML decoding, the complexity of the algorithm is typically of the order (n_R number of receive antennas, n_T number of transmit antennas)

$$C_{\mathrm{ML}} = \mathcal{O}\left(n_R (n_T K)^P\right), \tag{37.9}$$

for K transmitted antenna symbols with P being the alphabet size. For flat Rayleigh fading channels, the symbols sent in different time periods arrive independently in time, reducing the ML complexity to

$$C_{\mathrm{ML}} = \mathcal{O}\left(n_R n_T^P\right), \tag{37.10}$$

for each transmitted antenna symbol. In particular, for higher-order constellations, this seems to be a very high complexity. However, in [37, 38, 39], techniques for low-complexity implementations especially for 16-QAM and 64-QAM have been proposed reducing the complexity considerably. Also smart, suboptimal techniques like sphere decoding [40], geometrical approaches [41], and other techniques [42] have been proposed.

Suboptimal ML sequence estimation techniques, originally invented by Viterbi [43], are usually favoured since their complexity is given by

$$C_{\mathrm{ML}} = \mathcal{O}\left(n_R (n_T n_C)^P\right), \tag{37.11}$$

with n_C denoting the channel length. Since such techniques also work in non-flat channels and, in particular, when the encoding part forces a certain memory, this technique can be found in 3GPP in form of turbo coding [44] (see also Figure 37.12). While many turbo coding implementations for UMTS in ASICs [45, 46] and standard DSPs [47] have been reported, there is only little information available on implementations for MIMO systems.

Matrix inversion methods are ZF, MMSE, and V-BLAST techniques, the simplest one being ZF, forcing the symbols $\mathbf{s}$ to be correct no matter what happens to the noise symbol $\mathbf{v}$. Let $\mathbf{r} = \mathbf{H}s + \mathbf{v}$ be the received symbol, with $\mathbf{H}$ denoting the channel matrix. Then, $\hat{\mathbf{s}} = (\mathbf{H}^H\mathbf{H})^{-1}\mathbf{H}^H\mathbf{r}$ is the ZF estimate. Such operation will force the noise to be filtered: $\hat{\mathbf{s}} = \mathbf{s} + \tilde{\mathbf{v}}$ with $\tilde{\mathbf{v}} = (\mathbf{H}^H\mathbf{H})^{-1}\mathbf{H}^H\mathbf{v}$. The complexity is next to the required channel estimation defined by the inverse operation of a matrix, thus, in general,

$$C_{\mathrm{ZF}} = \mathcal{O}\left(n_T^3\right), \tag{37.12}$$

and does only need to be performed once the channel changes. The decoding part is then simply a matrix multiplication of $\mathbf{r}$ by the term $(\mathbf{H}^H\mathbf{H})^{-1}\mathbf{H}^H$, thus of order $n_T n_R$ for each transmitted symbol. A hard decision is usually required afterwards to decide which symbol from the symbol alphabet has been received. While the order $n_T n_R$ per symbol seems to be much smaller than in the case of ML, the matrix

inversion operation requires high-precision techniques. Standard 16-bit DSPs have problems performing such operations with sufficient precision. Alternatives are either expensive floating-point processors or dedicated logic with QR algorithms [48, 49] or similar techniques using *energy preserving* CORDIC operations [50].

While ZF usually gives the poorest performance, only slightly better than linear combination techniques, MMSE promises better quality with approximately the same complexity. Different to ZF, the noise impact is taken into consideration when forming the matrix inverse: $\hat{\mathbf{s}} = (\mathbf{H}^H\mathbf{H} + \sigma_v^2 I)^{-1}\mathbf{H}^H\mathbf{r}$ is the MMSE estimate. While the computation of the matrix inverse is not more complex, the additive noise term improves the condition number and thus the requirement on floating point precision. However, such matrix inverse still requires, in general, more than 16-bit precision and thus nonstandard HW. Also the additive noise part of the channel needs to be estimated now, a task not simple in a time-variant channel environment. In case the noise estimation is more than 3 dB off, the quality improvement compared to ZF is typically lost again [51].

A better method utilizing matrix inversion is given by the so-called V-BLAST algorithm. It exists in ZF and MMSE form. Rather than performing the matrix inverse for all symbols, it is only performed for the symbol with the strongest energy, estimated on the matrix inverse. After the first symbol has been detected, the channel matrix is reduced in rank and the entire procedure is repeated until the last symbol is detected. The V-BLAST complexity is thus of n_T times the ZF complexity. Performance quality is substantially improved compared to ZF and MMSE. However, like in the ZF and MMSE case, a standard, low-cost 16-bit DSP has problems in computing accurate matrix inverses.

37.4. Implementation examples

In this section, we only focus on MIMO baseband prototype and chip solutions, since little work is available on MIMO complient RFICs. MIMO systems are currently in the process of 3GPP standardization. It turns out that MIMO will only be established for the HSDPA extension of UMTS [52]. Naturally no low-cost mass products are available yet. However, two trends can be observed. At universities and research centers, demonstrations are performed with off-the-shelf equipment (see, e.g., [53, 54, 55], a more complete listing will be provided in the chapter *Demonstrators and Testbeds* in this book). A second trend in MIMO realization, mainly driven by the semiconductor industry, concerns first steps towards integrated solutions.

Demonstrator and prototype developments are often evolutionary starting with rather simple and easy manageable approaches, which are enhanced step by step, finally resulting in real-time systems. The air interface is usually realized by standard RF and mixed signal components (see Figure 37.13) covering the WLAN and/or the UMTS band. Typically, a PC generates data, which is transmitted over real or artificial channels. After down conversion, the received signals are stored and processed, again in a PC, online or offline. The transmission is typically performed in burst mode. Such a configuration is ideally suited for algorithm

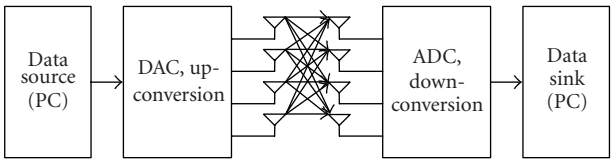

Figure 37.13. MIMO demonstrator system.

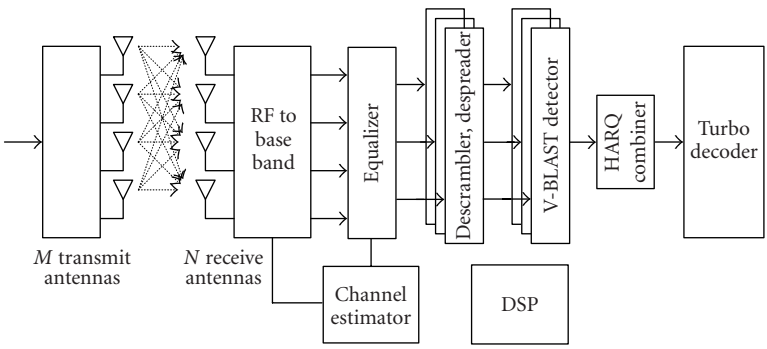

Figure 37.14. HSDPA MIMO receiver as reported in [2].

development under real physical channel conditions. A modular and flexible design allows to enhance the system towards real-time processing by replacing PC software by DSP and FPGA modules step by step. A complete four-antenna receiver design following this approach was presented in [31, 34] for the UMTS downlink. In [31] the authors report on the prototype experience of a UMTS MIMO system with four transmit (TX) and receive (RX) antennas considering ZF-V-BLAST and ML algorithms. The different MIMO detectors including appropriate channel estimation procedures are evaluated by comparing their performance and complexity.

A number of experimental and commercial smart antenna systems are published in [56]. The purpose of these systems was the demonstration of the performance increase through the use of smart antennas.

Several chip solutions have already been presented by Lucent Technologies and Agere Systems. A baseband chip for the base station was presented in [2]. The detection is performed using the V-BLAST algorithm, a 0.16 μm CMOS technology is used for chip implementation. Figure 37.14 shows a simplified block diagram of the receiver.

In this implementation, the channel estimation and matrix inversion are performed by a DSP. An ML detector for a flat-fading channel is introduced in [57]. The block diagram of this receiver is shown in Figure 37.15.

The detection is performed either for four RX antennas in combination with QPSK, or for two RX antennas and 8PSK/16QAM. A maximum number of 10

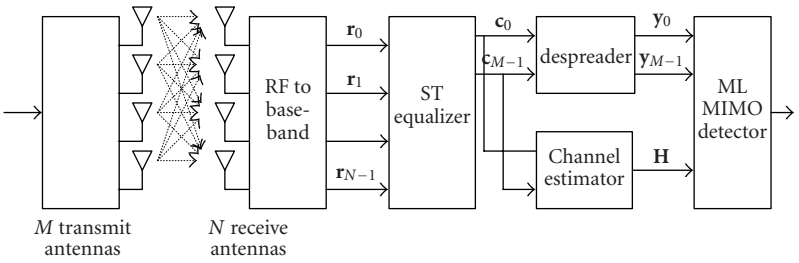

FIGURE 37.15. HSDPA MIMO receiver as reported in [57].

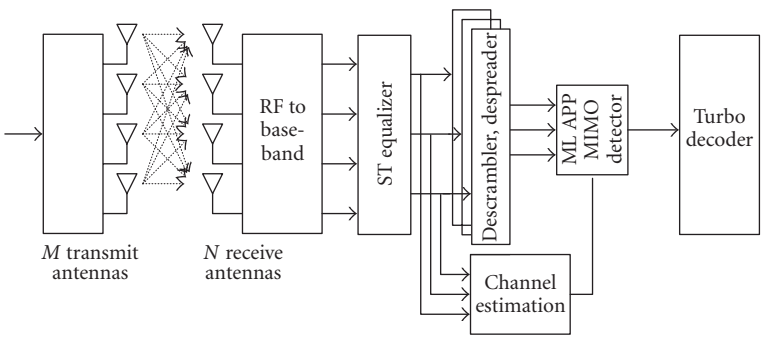

FIGURE 37.16. HSDPA MIMO receiver for frequency-selective fading channel as reported in [60].

spreading codes of length 16 allows a data rate of 19.2 Mbps. The detector outputs are derived by approximating the log-likelihood ratios of the a posteriori probability (APP). Hence, this algorithm is called ML-APP detector.

Different MIMO 3GPP-HSDPA detectors have been reported in [57, 58, 59, 60] by the same group of authors. As an example, Figure 37.16 shows the block diagram of a 28.8 Mbps 4×4 MIMO 3GPP-HSDPA receiver [60]. This approach is capable of handling frequency-selective channels by applying an ST equalizer at chip level. A normalized least mean square (LMS) algorithm is used for the estimation of the equalizer coefficients. A peak data rate of 28.8 Mbps can be achieved by using 15 spreading codes and a 4×4 system.

Implementation examples of square root MIMO detection algorithms are reported in [48, 61, 62].

All these chip implementations and prototypes depict important steps towards cost efficient integrated MIMO HSDPA solutions. They play a crucial role in the standardization process, which is currently in progress. Note that final MIMO HSDPA solutions have to be downwards compatible to current 3GPP standard releases.

37.5. Summary

The development of MIMO techniques for UMTS is a major field of ongoing research at university and industry level. MIMO algorithms typically exhibit

extremely high complexity. Therefore, the exploration of low-complexity solutions is highly desirable with respect to today's semiconductor technology implementations. A number of prototype systems and chip solutions have already been reported. Most of these solutions act on simplified assumptions, for example, flat-fading channels. Nevertheless, these first prototypes are extremely helpful in identifying problems inherent to MIMO signal processing. Thus, they are driving the standardization process of UMTS MIMO systems.

There is only little work available that specifically deals with MIMO compliant RF front ends. The straight forward approach of a MIMO RF front-end implementation is the use of a dedicated receiver per antenna. This approach shows significant area and power saving potential, and therefore tends to be the most favored technology.

Acknowledgment

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Abbreviations

3GGP	3rd-Generation Partnership Project
MIMO	Multiple-input multiple-output
SISO	Single-input single-output
RFIC	Radio frequency integrated circuit
ST	Space-time
ADC	Analog-to-digital converter
AGC	Automatic gain control
RRC	Root raised cosine
GSM	Global system for mobile communication
ACS	Adjacent channel selectivity
PAR	Peak-to-average ratio
PAE	Power added efficiency
SAW	Surface acoustic wave
MIPS	Million instructions per second
UMTS-FDD	UMTS-frequency division duplex
BER	Bit error rate
BLER	Block error rate
W-CDMA	Wideband code division multiple access
CCDF	Complementary cumulative probability density function
DPDCH	Dedicated physical data channel
CPICH	Common pilot channel
CCPCH	Common control physical channel
PICH	Paging indicator channel
SCH	Synchronization channel
SF	Spreading factor
TDMA	Time division multiple access
FDMA	Frequency division multiple access

LO	Local oscillator
LNA	Low noise amplifier
IP2	Intercept point
OSR	Oversampling rate
MRC	Maximum ratio combining
MUI	Multiuser interference
MMSE	Minimum mean square error
MVDR	Minimum variance distortionless response
FPM	Finger position search and management
PCG	Pilot code generator
ML	Maximum likelihood
ZF	Zero forcing
V-BLAST	Vertical Bell Laboratories Layered Space-Time
SPICH	Secondary pilot channel
HSDPA	High-speed downlink packet access
APP	A posteriori probability

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