Balanced Optical Phase-Locked Loop Based on Four-Wave Mixing in Semiconductor Optical Amplifiers

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An optical phase-locked loop (OPLL) has often been used for subharmonic clock extraction in high-bit-rate transmission systems because it provides a high-speed operation and a low relative phase error. In this paper, we propose an OPLL containing an all-optical phase comparator in a balanced symmetric configuration. The phase comparator is based on four-wave mixing (FWM) in semiconductor optical amplifiers (SOAs). Due to the balanced symmetric configuration, the phase error signal used to control the voltage-controlled oscillator (VCO) is DC-balanced and can have positive or negative sign depending on whether the phase difference between data and clock pulses is positive or negative. The proposed scheme for optical clock recovery is investigated by numerical simulations and results are presented.

1. Introduction

Clock recovery units capable of extracting a high quality clock from an incoming optical signal are required in all-optical routers, 3R regeneration components as well as for an error free receiving of high-speed signals at the end nodes.

Various methods for optical clock recovery at high data rates have been studied recently [1, 2, 3, 4, 5, 6, 7, 8, 9, and 10]. An accurate timing extraction is required by all transmission subunits such as optical receivers, 3R regenerators, cross-connects, and OTDM demultiplexers. The main requirements on the recovered clock are low timing jitter, low amplitude fluctuation, polarization independence, and short acquisition time (clock-synchronization time).

Optical clock recovery circuits can be classified into three categories: optical tank circuits, injection locking techniques, and techniques employing a phase-locked loop (PLL). The last one is a very promising technique for subharmonic clock extraction because it provides a high-speed operation with a low relative phase error.

A method for high-speed optical clock recovery based on a balanced phase-locked loop is proposed in this paper. It comprises an all-optical phase comparator based on four-wave mixing (FWM) in semiconductor optical amplifiers (SOAs). We used two SOAs in order to achieve a symmetric balanced configuration. Feasibility and key parameters of the balanced OPLL are investigated by means of numerical simulations.

2. Architecture

The proposed structure of a balanced optical phase-locked loop is shown in Fig. 1. It consists of an optical phase comparator, a voltage-controlled oscillator, and a tunable mode-locked laser. This scheme exploits four-wave mixing (FWM) in SOA and allows fast extraction of timing information from the incoming data signal. Due to the balanced configuration, the error signal used to control the voltage-controlled oscillator (VCO) can have positive or negative sign depending on whether the phase difference between data and clock pulses is positive or negative. This overcomes the well-known problem of an optical phase comparator that the error signal has only one polarity.

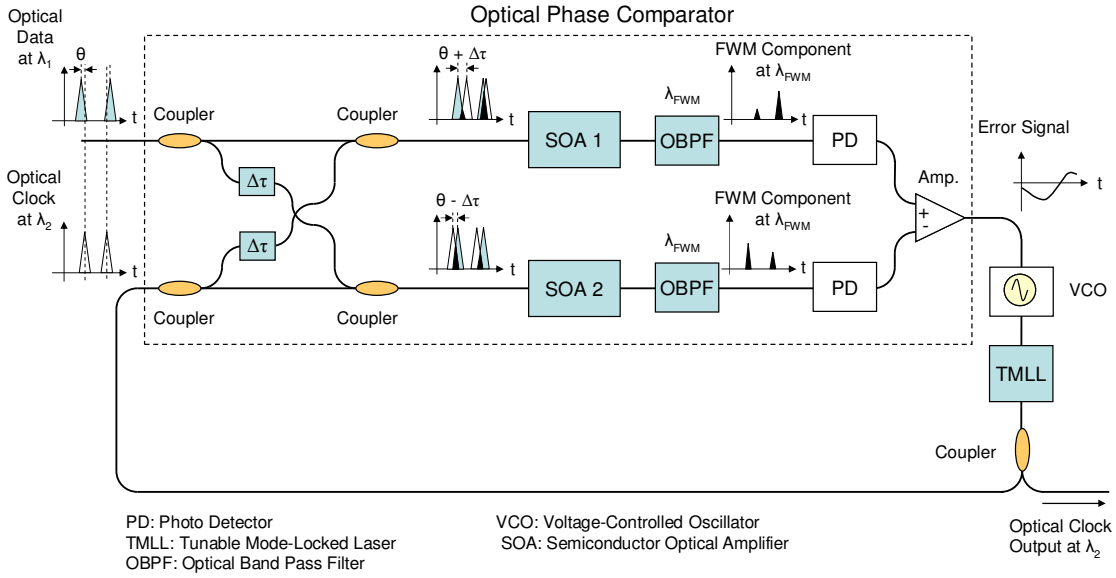

Figure 1: Schematics of the proposed clock recovery method.

In the optical phase comparator, incoming data signal is mixed with local clock in two SOAs by means of FWM. Because the optical clock signal is delayed by $\Delta\tau$ before traversing the upper SOA (SOA1), and similarly, the incoming data signal is delayed by the same delay before the bottom SOA (SOA2), the FWM component after SOA2 will be larger than that after SOA1 when data pulses precede clock pulses (negative phase difference - θ). On the contrary, the FWM component in the upper arm will dominate when clock pulses precede data pulses (positive phase difference). Thus, after receiving the FWM components by two slow photodiodes we can obtain an error signal at the output of the differential amplifier. The error signal has a positive sign for a positive phase difference and a negative sign for a negative phase difference. If data and clock signals have the same frequency and phase, the strengths of the FWM components in both arms will be the same, and consequently, the error signal becomes zero. The error signal is used to control the frequency of the voltage-controlled oscillator (VCO). Thus, the frequency of the VCO is increased or decreased by Δf depending on whether the phase difference is positive or negative, respectively. The electrical clock generated in the VCO is used to modulate the tunable mode-locked laser (TMLL), which produces a high quality optical clock signal. Note that this structure represents a first-order PLL because it does not include any loop filter, and thus, large phase margins can be easily obtained. The main bandwidth limiting components in the system are the two slow

photodiodes. Thanks to the symmetric structure of the phase comparator, both the fundamental frequency of the data signal as well as DC offset at the output of the comparator can be efficiently suppressed. Moreover, if both SOAs, which are chosen to have similar properties, are thermal coupled, the whole structure becomes more stable and less sensitive to changes in temperature.

3. Numerical Simulations

Numerical simulations were performed in order to investigate the proposed scheme regarding achievable lock-in time. For this purpose, we used the VPIsystems simulation software. The main simulation parameters are shown in Table 1.

Parameter	Value	Unit
SOA length	500	µm
Width of the active region	3.5	µm
Thickness of the active region	0.18	µm
Confinement factor	0.35	
Group effective index	3.7	
Linewidth enhancement factor	4	
Nonlinear gain coefficient	1×10^{-23}	m^{-3}
SOA current	250	mA
Bandwidth of the photodiode	500	MHz
Delay $\Delta\tau$ (ranges between 0 and $T_{bit}/2$)	2.5	ps
Peak power of data pulses	50	mW
Width of data pulses (FWHM)	2	ps
Peak power of clock pulses	50	mW
Width of clock pulses (FWHM)	1.5	ps

Table 1: Key parameters used in simulations of balanced optical phase-locked loop.

We first investigated the transient time response of the error signal for different initial phase steps of $\pm T_{bit}/8$, $\pm T_{bit}/4$, and $\pm T_{bit}/2$, where T_{bit} is the bit period of the data signal. In our simulation set-up, 160 Gbit/s data was generated and injected in the structure depicted in Fig. 1. At the output of the structure, a high-quality 40 GHz optical clock was extracted.

The width of clock pulses was adjusted to be 1.5 ps (FWHM) and that of incoming data pulses to 2 ps (also measured as FWHM). The transient responses for all six phase steps indicate that the clock recovery unit only requires 4 ns to completely lock to the phase shifted signal and to approach the steady-state value (see Fig. 2).

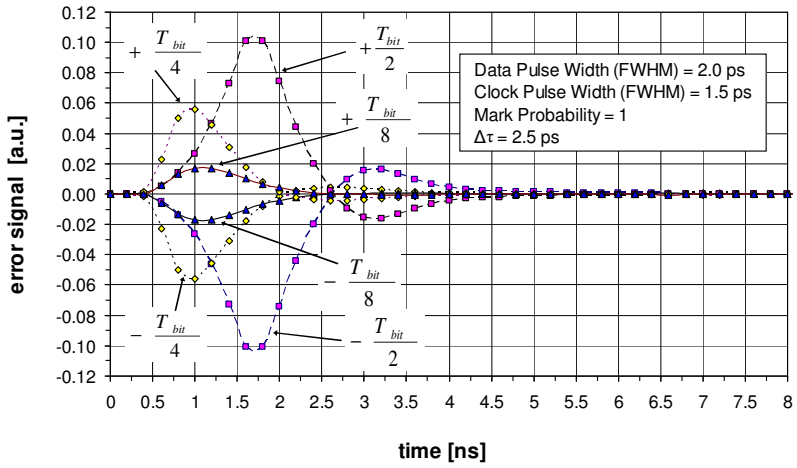

Figure 2: Transients of the phase error signal for different initial phase shifts of $\pm T_{bit}/8$, $\pm T_{bit}/4$, and $\pm T_{bit}/2$.

The transient time response of the error signal at the input of the VCO for three mark probabilities (MPs) is shown in Fig. 3. The error signal fast approaches the lock condition from an initial unlocked state. In this case, the data pulses were inserted with an initial phase difference of $+T_{bit}/4$ relative to the clock pulses. For a mark probability of 1.0, i.e., when there were only "ones" in the data signal, we could obtain a clock acquisition time below 4 ns. A setting time of about 5 ns was observed for PRBS sequences with MP = 0.7 and MP = 0.5. After the PLL phase-locked to the input data, it started to generate a stable and high quality clock.

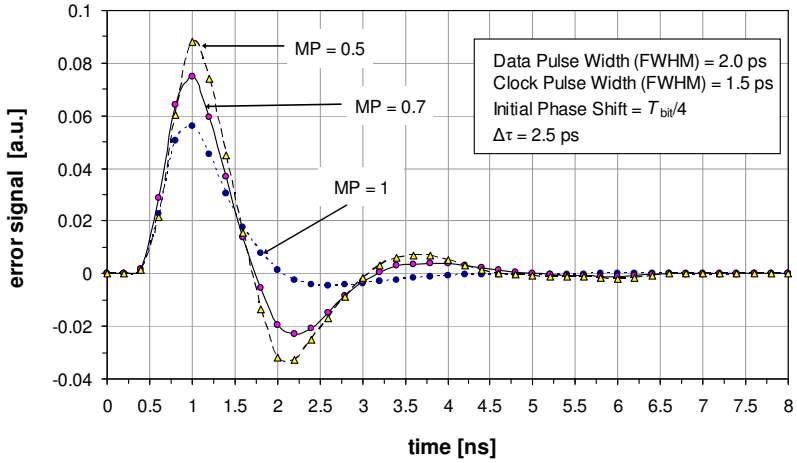

Figure 3: Transient time response of the error signal for three different mark probabilities (MPs).

It is of particular interest to study the influence of data pulse properties on behavior of the phase-locked loop. In particular, we were interested in ranges of various parameters, within which the scheme allows short lock-in times and a stable operation, as well as in the required accuracy of the delay line $\Delta\tau$. The results shown in Fig. 4 and Fig. 5 indicate that the scheme is not very sensitive to variation in pulse properties such as width and peak power (P_{peak}). That is, a lock-in time less than 10 ns was obtained for pulse widths form 1.2 ps to 4 ps and for peak powers from 3 mW to 400 mW.

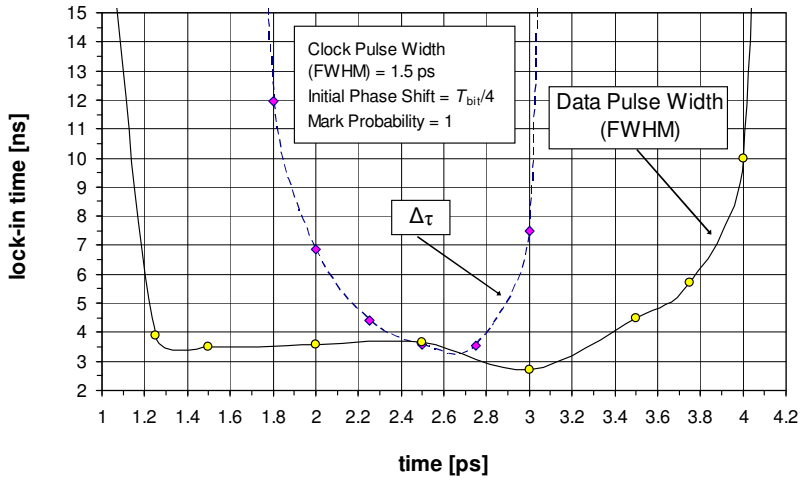

Figure 4: Lock-in time for different values of Δτ and data pulse widths.

By observing Fig. 4, it becomes evident that the scheme is sensitive to the accuracy of the optical delay line Δτ. This delay line should be adjusted to be between 1.9 ps and 3 ps in order to achieve a short lock-in time of less than 10 ns. The lock-in time increases fast outside of this range. The shortest values of lock-in time were obtained for Δτ = 2.6 ps and P_{peak} = 100 mW. Regarding the peak power, lock-in times shorter than 4 ns are possible within a wide range between 5 mW and 225 mW.

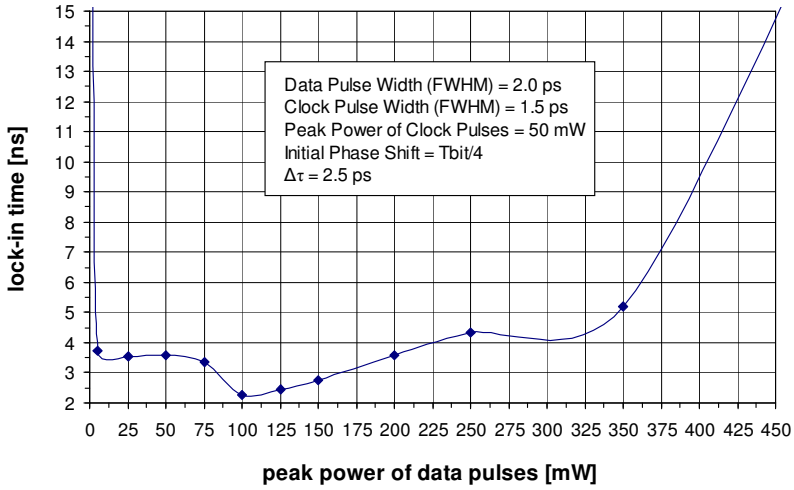

Figure 5: Lock-in time vs. peak power of data pulses.

4. Conclusion

In conclusion, we proposed and investigated a scheme for clock recovery based on a balanced optical phase-locked loop. To compare the phase of an incoming return-to-zero (RZ) data signal with the local clock we used two semiconductor optical amplifiers in a symmetric configuration. Our results obtained by means of numerical simulations have shown that this method allows a fast clock acquisition and a stable operation even for large initial phase differences and low mark probabilities of data

sequences. It is not such sensitive to changes of main properties of the incoming data pulses such as peak power and width, which are usually impaired during signal transmission. Only the delay $\Delta\tau$, which is locally used to induce a delay between pulses of the incoming data and the local clock, has to be adjusted precisely.

Acknowledgements

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