Fast Clock Recovery Methods for Application in All-Optical Networks

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Abstract—**Two different clock recovery schemes suitable for application in all-optical networks are described and analyzed by means of numerical simulations. The scheme based on an injected mode-locked ring laser produces an optical clock with a low timing jitter and a low amplitude variation if a Fabry-Pérot etalon is inserted at the input of the structure. The second scheme is a phase-lock loop (PLL) with an all-optical differential phase comparator. It extracts a high quality clock from PRBS data within a short acquisition time.**

Keywords—**Clock Recovery, All-Optical Networks, Phase-Lock Loop, Mode-Locked Laser, OTDM**

I. Introduction

In high-speed optical transmission systems, extraction of a high-quality clock from the received optical signal is an important task. An accurate timing extraction is required by all transmission and processing systems. The main requirements on the extracted clock signal include low timing jitter, low amplitude fluctuation, polarization independence, and short acquisition time (clock synchronization time). The latter requirement is extremely important in packet- and burst-switched systems.

Electrical timing extraction circuits usually use a microwave mixer as a phase detector in a phase-lock loop (PLL) configuration. The operating speed of such circuits is limited by the phase detector to about 40 GHz. The main advantage of approaches using a PLL is that the phase of the incoming signal is constantly compared with the phase of the local oscillator. Consequently, a low relative phase error can be achieved.

To overcome the speed limitation of electrical timing extraction circuits, various methods employing photonic technology have been studied [1, 2, 3, 4, 5, 6, 7, 8]. The semiconductor laser based approaches such as self-pulsating laser diodes (SP-LD) and mode-locked laser diodes (ML-LD) have the advantage of being compact and mechanically stable [1, 5]. The laser is synchronized with the incoming signal by injection locking. Thus, the clock is generated all-optically.

A phase-locked loop with an all-optical or optoelectrical phase comparator could overcome the speed limitation of conventional electrical circuits caused by large response times of the phase comparator, especially when a subharmonic clock extraction from data signals beyond 100 Gbit/s is required. A semiconductor optical amplifier (SOA) can be used as an optical phase comparator [3,4]. In this approach, the phase difference between incoming optical signal and local clock pulses is detected by exploiting either the gain modulation effect or four-wave mixing (FWM) in SOA. Optical PLLs that use the fast FWM process in SOA are of the particular interest because of their small size and stable, ultrahigh-speed response.

Other candidates for phase comparators are electroabsorption modulators (EAMs) [9] and interferometric optical switches based on SOAs such as terahertz optical asymmetric demultiplexer (TOAD) [10, 11], symmetric Mach-Zehnder interferometer (SMZI) [12], semiconductor laser amplifier in the loop mirror (SLALOM) [13], and ultrafast nonlinear interferometer (UNI) [14].

This paper presents two fast optical clock recovery schemes suitable for application in all-optical network nodes and 3R regenerators. These schemes include a SOA-based mode-locked ring laser (MLRL) and a novel clock extraction circuit based on a differential configuration of the optical phase comparator that exploits four-wave mixing (FWM) in semiconductor optical amplifiers.

II. SOA-Based Mode-Locked Ring Laser

The schematic of the clock recovery based on a mode-locked ring laser with a semiconductor optical amplifier (SOA) in its cavity is shown in Figure 1. The SOA with sufficient gain to ensure lasing in the ring cavity at wavelength λ_2 is used as a gain element. The incoming data signal at λ_1, which is injected into the MLRL through a Fabry-Pérot filter and a coupler, modulates the gain of the SOA. Thus, the amplitude of the signal in the loop is modulated by exploiting the cross gain modulation (XGM) in SOA. The length of the loop can be adjusted precisely by the tunable optical delay element τ. The Fabry-Pérot filter with a free spectral range equal to the data rate of the incoming signal is placed at the input of the structure in order to compensate for the pattern effect in SOA [15]. An isolator within the ring cavity ensures unidirectional operation.

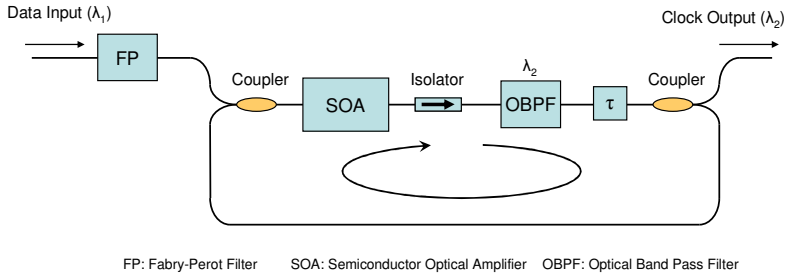

Figure 1: All-optical clock extraction circuit based on a SOA-based mode-locked ring laser

In our study, we observed the relative variation of peak power (i.e., amplitude jitter) and the timing jitter of generated clock pulses at the output. The relative variation of peak power is defined as $v = (P_{max} - P_{min})/(P_{max} + P_{min})\cdot 100\%$. The results we obtained by using VPI Systems simulator for 40 Gbit/s return-to-zero (RZ) data are shown in Figures 2 to 5. The key parameters used in simulations are listed in Table 1.

Parameter	Value	Unit
Fabry Pérot Filter		
Free spectral range	40×10^9	Hz
Mirror transmission	0.04	
SOA		
Length	900	µm
Width of the active region	2.5	µm
Thickness of the active region	0.04	µm
Group effective index	3.7	
Bias current	350	mA
Data pulses		
FWHM	5	ps
Peak power	50	mW

Table 1: Key parameters used in simulations of SOA-based mode-locked ring laser

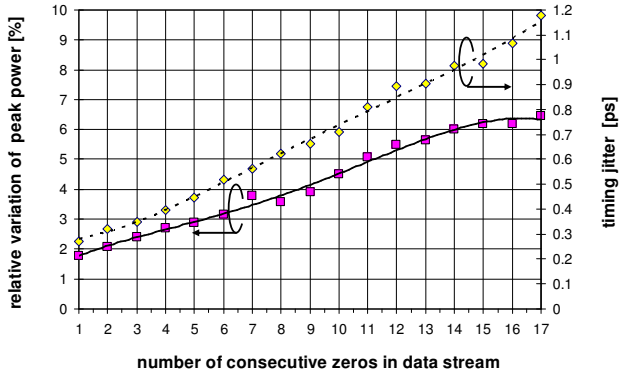

Figure 2: Relative variation of peak power and timing jitter vs. number of consecutive "zeros"

The influence of occurring data sequences with many consecutive "zeros" is shown in Figure 2. It can be seen that both the relative variation of peak pulse power and the peak-peak timing jitter increase with increasing the number of consecutive "zeros". A power variation lower than 6.5 % and peak-peak timing jitter up to 1.2 ps have been obtained for data sequences containing up to 17 consecutive "zeros". Figure 3 shows the quality of generated optical clock versus mark probability of the input data. Both the timing jitter and the relative peak power variation increase with decreasing the mark probability of PRBS data sequences. A maximum timing jitter value of 1.83 ps and a power variation of v = 3.58 % have been obtained for a mark probability of 0.3.

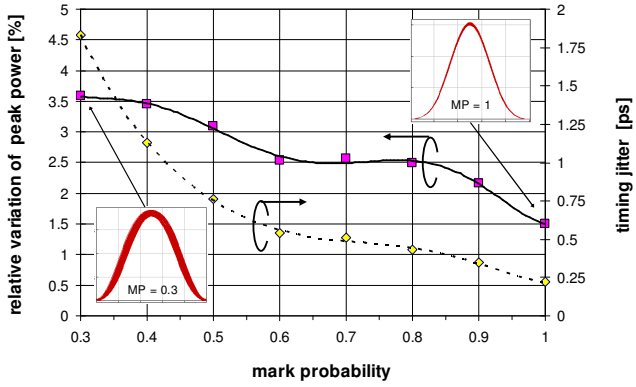

Figure 3: Relative variation of peak power and timing jitter versus mark probability of PRBS data

Further, we investigated the influence of pulse power of data signal on timing jitter and amplitude fluctuation of the generated clock. As it can be seen in Figure 4, the structure produces high quality optical clock for a wide range of power of data signal. The best result we obtained for a peak power of 10 mW. At this point, the timing jitter and the peak power variation of clock pulses are 0.5 ps and 1.3 %, respectively. For an increase of the peak power up to 100 mW, the timing jitter remains almost constant, while the relative variation of the clock amplitude increases to slightly more than 3 %. If the power of the data signal is lower than 5 mW, the modu-

lation of SOA is not deep enough, and consequently, both timing jitter and amplitude jitter become large.

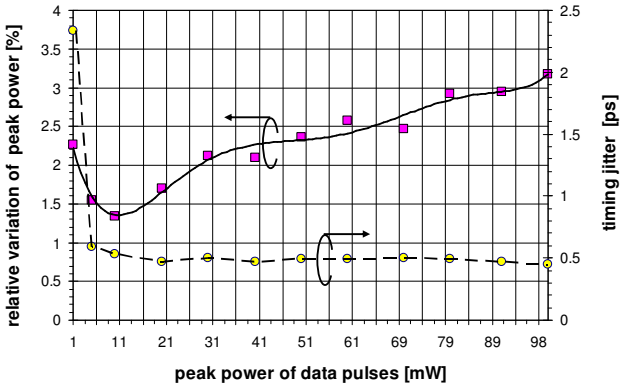

Figure 4: Influence of data pulse power on clock quality

We also studied the effect of different data pulse widths on generated clock. The best results were obtained for a pulse width of 2.5 ps (see Figure 5). A clock signal with a timing jitter below 0.6 ps and a relative variation of peak power less than 3 % can be generated for data pulse widths within the range from 2 ps to 6 ps. When the pulse width exceeds 6 ps, both timing jitter and especially amplitude modulation of clock are strongly impacted by overlapping of neighboring data pulses. If the pulse width becomes shorter than 2 ps, both timing jitter and relative variation of peak power increase.

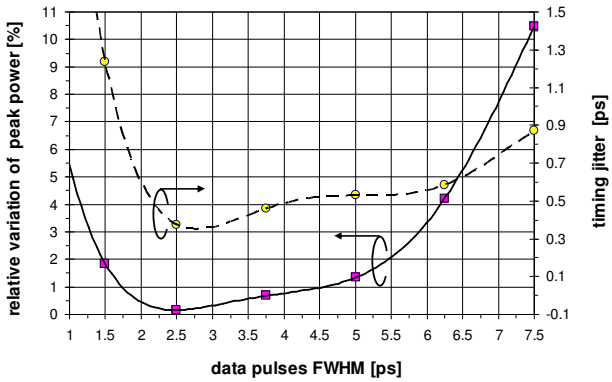

Figure 5: Influence of data pulse width on clock quality

III. Optical Phase-Lock Loop

An optical phase-lock loop (PLL) is a very promising technique for subharmonic clock extraction because it provides a high-speed operation with a low relative phase error. Thus, it is well suitable for high data rate OTDM applications.

Figure 6 shows the proposed structure of an optical phase-lock loop with an all-optical phase comparator that consists of two SOAs in a differential configuration. This scheme exploits four-wave mixing (FWM) in SOA and allows fast extraction of timing information. Due to the differential configuration, the error signal used to control the voltage-controlled oscillator (VCO) can have positive or negative sign depending on whether the phase difference between data and clock pulses is positive or negative. This overcomes the well-known problem of an optical phase comparator that the error signal has only one polarity.

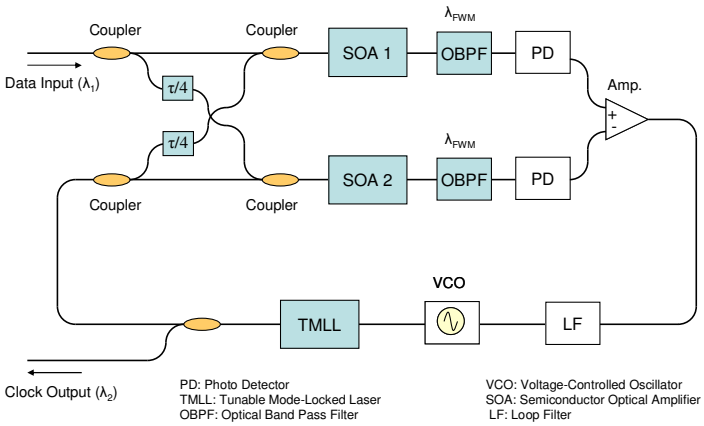

Figure 6: Schematic diagram of the phase-lock loop with a differential optical phase comparator

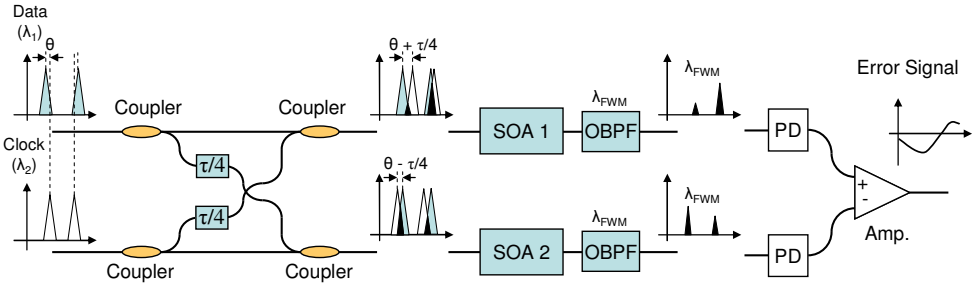

Figure 7: Principle of operation of the all-optical phase comparator

The principle of operation of the optical phase comparator is depicted in Figure 7. Because control pulses are delayed in the upper SOA (by τ/4) and data pulses in the bottom SOA (also by τ/4), the FWM component after SOA2 will be larger than the FWM component after SOA1 when clock pulses precede the data pulses (positive phase difference - θ). On the contrary, the FWM component in the upper arm (after SOA1) will dominate when data pulses precede clock pulses (negative phase difference). Thus, after receiving the FWM components by two slow photodiods we can obtain an error signal at the output of the differential amplifier, which has a positive sign for the negative phase difference and a negative sign for the positive phase difference. Thus, the frequency of the VCO will be increased or decreased by Δf depending on whether the phase difference is negative or positive, respectively. If data and clock pulses are in phase with each other, the strengths of the FWM components in both arms are the same, and consequently, the error signal becomes zero.

Numerical simulations were performed to investigate the proposed clock extraction scheme. In the simulation set-up, 80 Gbit/s PRBS data was generated and injected in the structure from Figure 6. The frequency of the VCO was set to approx. 10 GHz. The width of clock pulses was adjusted to be 3.25 ps FWHM and that of incoming data pulses to 4 ps FWHM. Some of parameters used in simulations are shown in Table 2.

Parameter	Value	Unit
Length of the SOA	500	µm
Width of the active region	3.5	µm
Thickness of the active region	0.18	µm
Confinement factor	0.35	
Group effective index	3.7	
Linewidth enhancement factor	4	
Bias current of the SOA	350	mA
Bandwidth of the photodiode	500	MHz
Delay τ/4	4.5	ps
Peak power of data pulses	50	mW
Peak power of clock pulses	50	mW

Table 2: Key parameters used in simulations of optical phase-lock loop

The transient time response of the error signal at the input of the VCO for three mark probabilities (MPs) is plotted in Figure 8. The error signal fast approaches the lock condition from an initial unlocked state. In this case, the data pulses were inserted with an initial phase difference of + $T_{bit}/4$ relative to the clock pulses.

For a mark probability of 1.0, i.e., when there were only "ones" in the data signal, we could obtain a clock acquisition time below 4 ns. A setting time of about 5.5 ns was needed for PRBS sequences with MP of 0.7, while the PLL approached the stable locked state in 6.5 ns for a mark probability of 0.5. After the PLL phase-locked to the input data, it started to generate a stable and high quality clock whatever mark probability is.

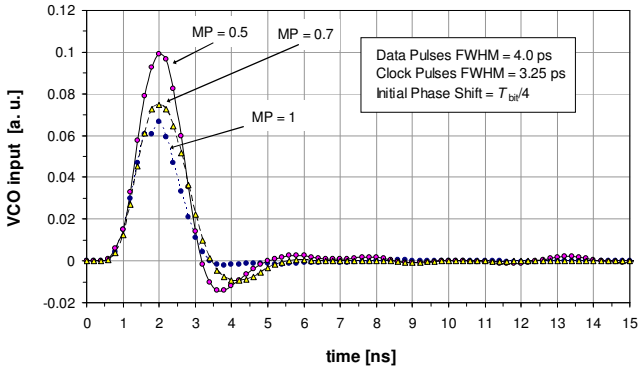

Figure 8: Transient time response of the error signal for three different mark probabilities (MPs)

In order to investigate the behaviour of the clock recovery in the case of data bursts we generated first a 1000-bits long data sequence containing only "ones" to ensure that PLL has perfectly phase-locked to the data. These 1000 pulses were followed with 150 "zeros", and finally, we generated another sequence containing 1000 successive pulses that were time delayed with respect to the first sequence. The results we obtained for six values of the phase difference between the two pulse trains, i.e. for phase steps $\pm T_{bit}/8$, $\pm T_{bit}/4$, and $\pm T_{bit}/2$, where T_{bit} is the bit period of the data signal, are shown in Figure 9. The transient responses for all six phase steps indicate that the clock recovery unit only requires 4 ns

to completely lock to the phase shifted signal and to approach the steady-state value.

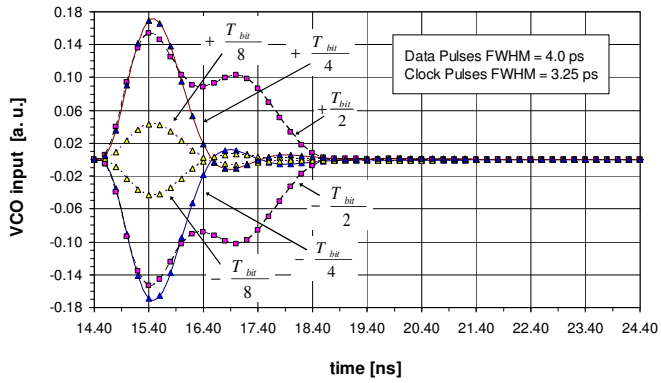

Figure 9: Error signal for various phase steps of $\pm T_{bit}/8$, $\pm T_{bit}/4$, and $\pm T_{bit}/2$

IV. Conclusion

We performed numerical simulations in order to investigate two optical clock recovery schemes regarding quality of generated clock and clock acquisition time. These schemes include a SOA-based mode-locked ring laser and a phase-lock loop with all-optical phase comparator. The first scheme uses a semiconductor optical amplifier as the gain element and a Fabry-Pérot (FP) filter to reduce the pattern effect. Our results concerning different number of consecutive "zeros" within the data stream, different mark probabilities of pseudorandom data sequences, as well as various values of signal power and pulse width have shown that this scheme produces a high quality optical clock for a relatively wide range of considered parameters. The second scheme is a phase-lock loop with a novel structure of all-optical phase comparator. It was investigated regarding the clock acquisition time. We obtained a short acquisition time of 4 ns for a data signal with only "ones" and 6.5 ns for PRBS data with a mark probability of 0.5.

Acknowledgment

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