A 100GHz Bandwidth Matched Chip to PCB Transition Using Bond Wires for Broadband Matching

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Abstract

A transition between a microstrip line on a radio frequency integrated circuit (RFIC) made of silicon and a microstrip line edged on a printed circuit board (PCB) consisting of Rogers 3003 substrate is presented. This transition uses a specially designed and optimized arrangement of bonding wires to achieve a matched bandwidth of nearly 100GHz. This extremely large bandwidth is needed for applications in frequency flexible or very broad band systems [1] or for ultra high frequency devices [2] to be operated on a PCB, which is mandatory for commercial usage. The parasitic inductance of a bond wire does not become a problem at moderate frequencies. Newer technologies like automotive radar [3], [4] or point to point transmitters operate at several dozens of gigahertz. At these frequencies connections by bond wires represent a major problem, because the impedance of the bond wire increases approximately linearly with frequency [5]. Equation (1) shows that even moderate inductances provoke very large impedances at a frequency of 100GHz, hindering efficient transmission of waves. The dramatic influence of these inductances, even for frequencies as moderate as 10GHz, is shown in [6].

$$Z_L = j\omega L \tag{1}$$

The Challenge of Broadband Interconnects

The characteristics of single bond wires and their disadvantageous influence on interconnects at a frequency of up to 110GHz are well described in [7] and [8]. Multiple bond wires on the same interconnect enable a reduction of the effective impedance. Unfortunately this approach is limited by the effect of mutual coupling between the wires, resulting in more than 1/N-th of the impedance when using N wires [9], [10] and is – even more important – limited by available space. Bond wires for ground connections, as presented in [11] and also depicted in Fig. 1 and 2, make use of a larger number of bond wires, as ground pads usually do not need to match a certain impedance and thus space is not at premium as much as on signal pads.

While minimization of transmission loss for a single frequency band of operation will already be impaired by losses in the matching elements (stubs, shorts, discrete capacitors and inductors), wideband matching to a specific characteristic impedance can not be achieved by these techniques. An interesting narrow band approach is shown in [12], an approach that enlarges the bandwidth by the use of two lumped but locally distributed capacitors is presented in [13].

Minimization of return loss by the use of matching elements is not a viable way to overcome this broadband transmission challenge, because all matching elements available offer highly frequency dependent values. The only exception is the characteristic impedance of a transmission line, as long as it is operated in mono-mode. While the impedance referenced to the input of a non matched transmission line depends on its length, the characteristic impedance of the line itself is well known to be extensively frequency independent. Thus the successful approach to design a matched transition for chip microstrip (MS) to a PCB MS is to approximate some kind of transmission line.

The method proposed is to approximate a transmission line by adding specially arranged bond wires. This approach is the optimum for the chip production because the tools to install bond wires are already available in each semiconductor fab. The added bond wires serve the purpose of adding purely distributed capacitance against ground to the distributed inductance of the signal bond wires. When distributed capacitances to ground C' and distributed inductances along the line L' are known for a transmission line, the characteristic impedance Z_{char} can be calculated by (2).

$$Z_{char} = \sqrt{L'/C'} \tag{2}$$

Approach to a wideband bond wire interconnect

(2) shows that a constant capacitance to ground along the bond wire would be desirable. A first step towards the calculation of bond wire transmission line structures is presented in [14]. [15] presents transmission lines and their characteristics built from bond wires, but as they are parallel and only analyzed at constant height over substrate, this is impractical for a chip to PCB transmission, which is usually manufactured with curved bond wires with different heights over ground for the start and the end of the wire. To circumvent the height difference, the chips are occasionally incorporated into a cavity, which is milled into the board. In this setup the bond wires can be installed horizontally. The problem of this solution is that an additional work step is needed during production and that this technique is unfeasible with molded integrated circuits that are meant to be soldered on top of an edged board, as the pads of the chip will not touch the PCB anymore. Another challenge is the different size of structures on chips and PCBs. Generally a MS (and its keep-out area) on a PCB is larger by at least one order of magnitude compared to the same structure on a chip. This prohibits the use of simple Co-Planar Wave-Guides as well matched transitions.

Test setup for the transmission analysis

The test setup consists of a chip made of silicon (relative permittivity of 11.9, tangent delta is variable over several process parameters and crystal quality). The chips height is 400 microns. A 10 microns thick ground plane is embedded within the chip at a height of 310 to 320 microns. The chips ground plane is connected to the PCBs metallization by a via-ring. The PCB metallization under the chip is connected to the PCBs ground plane by a rectangular array of vias. The thickness of the Rogers 3003 substrate (relative permittivity of 3, tangent delta of 0.0013) is 200 microns with 10 microns of metallization for tracks, planes and the ground plane. The chip is modeled with a cubical plastic mold (relative permittivity of 4), which is 1 mm high and encloses the whole chip including the bond wires and the first 250 microns of the PCBs microstrip. The test PCB has a side length of 7.5mm. The chips size is 2.15 times 2 mm. While the 50 Ohms microstrip transmission line is 63.4 microns wide and 5 microns thick on the chip, it is 510 micron wide and 10 microns thick on the PCB. All materials have been considered lossless for the simulation, as material losses cannot be avoided by changing structures and will affect both cases to a quite similar extent.

Design of Transition

The common basis for our analysis is the typical radio frequency (RF) chip to PCB connection, which is found in nearly all available RF designs. It consists of a silicon chip die that is mounted on a PCB. The signal path consists of a microstrip line on top of a chip that ends in a pad. This pad is connected to the microstrip line on the board by some bond wires; usually between 1 and 3 for low power output devices. We chose a connection consisting of two bond wires for our evaluation. This is the maximum quantity of bond wires that can be put on a 63 micron wide pad conveniently; broader pads would have different impedance than the preceding line – resulting in reduced matching quality. The chips ground is also connected via two times five bond wires on each side of the chip, additionally to the ground connection from the landing pad of the PCB. As the length of the bond wires is roughly 1.1mm, an inductance of slightly more than 1nH for one bond wire is expected. This inductance results in a serial impedance of approximately 600 Ohms at 100GHz according to (1); 300 Ohms for the parallel placement of 2 bond wires. 300 Ohms of series impedance are six times larger than the characteristic impedances of the lines, what causes a major part of the wave to be reflected.

To transform an inductor with a distributed inductance of 1nH to a transition line with a characteristic impedance of 50 Ohms, a distributed capacitance of 20pF along the line is desired. This value is calculated by an adapted version of (2). A capacity of 20pF is feasible by placing additional ground bond wires in the proximity of the signal bond wires. As it is practically impossible to calculate the capacitance distribution between two non parallel, bend bond wires from a chip to a PCB as an implicit function, a numerical field solver for radio frequency systems has been used.

The 3D finite difference time domain (FDTD) field solver Empire™ Xcel by IMST GmbH has been used for this purpose. The three dimensional views of the simulation setups, captured in the field solver, are depicted in Fig. 1 and Fig 2. Fig. 1 shows the basic chip to PCB microstrip transition with a typically arranged set of two bond wires. This reference setup already uses good engineering practices like a good ground connection; details are listed in the legend of Fig. 1. Fig. 2 presents the optimized setup using 6 additional ground bond wires placed in close proximity to the bond wires that are in charge of the signal connection. A less intuitive but more detailed two dimensional drawing of the simulation setup is displayed in Fig. 3. While the chips mold in made translucent for Fig. 1 and Fig. 2, Fig. 3 shows the outline of the chips plastic mold.

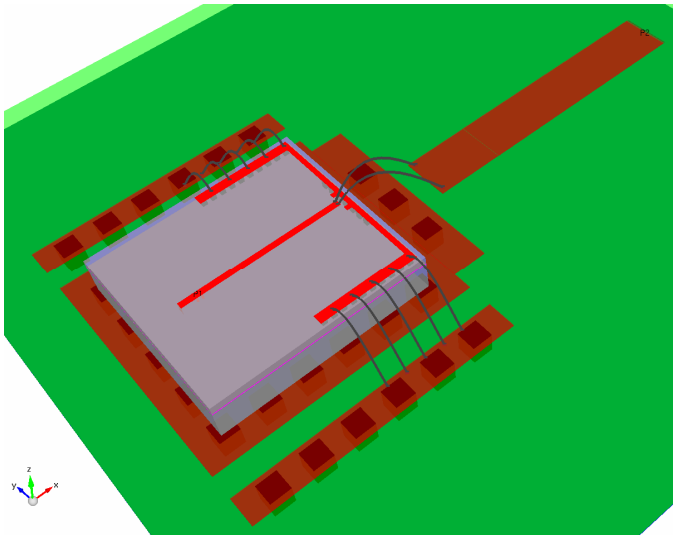

Fig. 1 – the non-matched chip to PCB transition already uses several techniques to reduce transmission losses, an array of ground bonds, 2 parallel signal bonds to reduce inductance of the interconnect and a chip ground plane that is well connected to the PCBs ground plane by multiple parallel vias. The chips mold is made translucent for this picture to maintain good visibility of the structures.

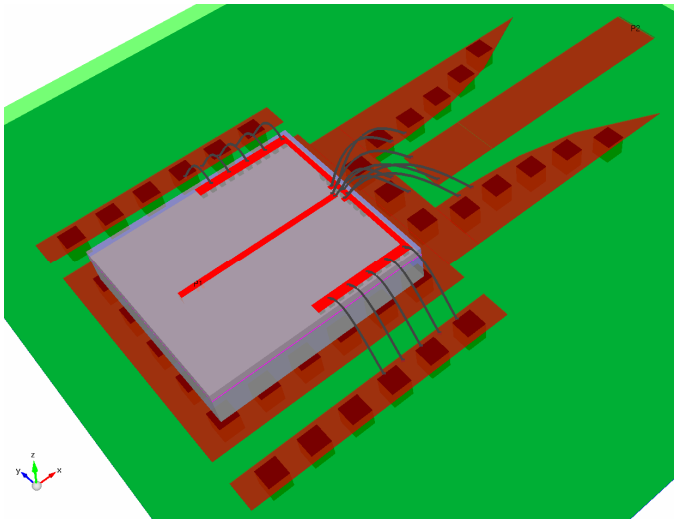

Fig. 2 – the matched chip to PCB transition uses additional ground wire bonds in the close proximity of the signal wire bonds to add a distributed capacitance and thus approximate a transmission line. All the other techniques described in Fig. 1

are used further on. To ensure ground connections for the additional ground bonds the microstrip is headed by an approximated coplanar waveguide to microstrip transition that has not been optimized for the simulations. The placement density of the bond wires varies with the relative permittivity of the chip mold. The chips mold is made translucent for the 3D graphics. A relative permittivity of 4 for the mold is used for the analysis; higher permittivity chip mold will allow larger distances between the bond wires. An extensive study of bond wires in a molded chip can be found in [16].

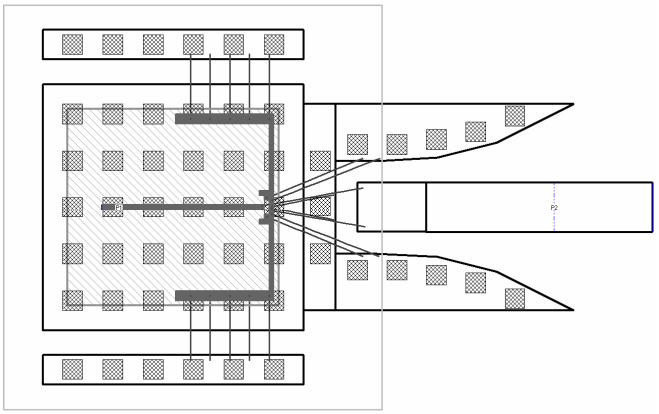

Fig. 3 – the engineering drawing of the optimized setup. The PCBs metallization and the bond wires are depicted in black. The short bond wires connected to the extension of the ground plane to the chips ground tracks are hidden underneath the signal tracks bond wires in this bird eye view drawing. The chips mold is outlined in light grey; the silicon chip is shown in shaded medium grey. The metallization on the chip is drawn in dark grey; the bracket-shaped ground track on the chip is connected by vias to the chips ground plane, which in turn is connected to ground by a metal ring embedded into the chip. The checkered squares depict the PCBs metallization to ground plane vias.

Results

The numerical analyses of the structures show that the proposed setup offers a considerable improvement over the non-optimized variant. The optimized setup offers a 3dB bandwidth of more than 100GHz and a 1dB bandwidth of slightly more than 51GHz, with an additional range offering less than 1dB attenuation between 68GHz and 97GHz; so 80GHz are covered with a transition attenuation of less than 1dB. The non-optimized setup has an essentially lower area of operation; the 1dB bandwidth is less than 14GHz, less than one-fifth of the proposed setup. The 3dB bandwidth is 74GHz, 26GHz less than in the optimized case. Especially for important frequencies like – the automotive radar frequencies – a distinct advantage is achieved. At 24 GHz the optimized attenuation is 0.24dB while the non-optimized structure would attenuate the signal by 2dB. At 77GHz the difference is even more significant. Typically 5.7dB would be lost at the transition. The proposed setup will only lose 0.3dB or 4.4 per cent in field strength. Qualified in power transmission efficiency the difference is even more obvious. The optimized setup transmits 93 per cent of the power while the reference setup is only able to transmit 23 per cent of the incoming wave's power. To compensate that losses a chip using the non-optimized version would need to be able to generate about four times as much power as a chip embedding our proposed version. Because microwave power capabilities at 77GHz are expensive, a reduction of required power by 75 per cent is very beneficial.

Please find the results of the transmission analysis as scattering parameter S21 in Fig. 4. The results of the return loss analysis (S11) are shown in Fig. 5.

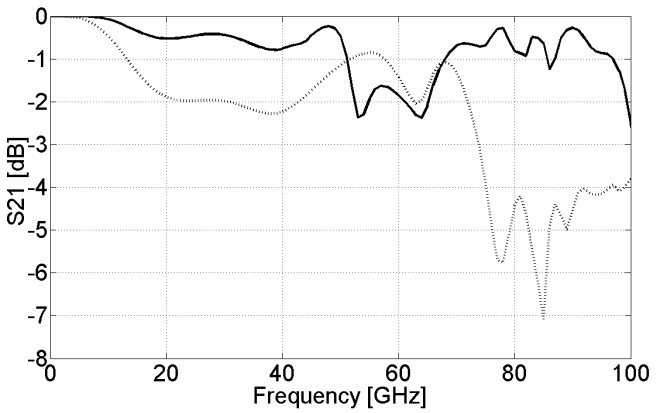

Fig. 4 – graphs of the transmission characteristic S21. The black massive line shows the characteristics of the optimized setup. The doted dark grey line represents the non-optimized reference setup. Attenuation is less than 1dB over a range of 80GHz after optimization; only 14GHz of bandwidth are achieved before optimization. The 3dB bandwidth of the proposed setup is even slightly more than 100GHz; only 74GHz for the reference setup. All frequencies below 97GHz are attenuated by less than 2.5dB.

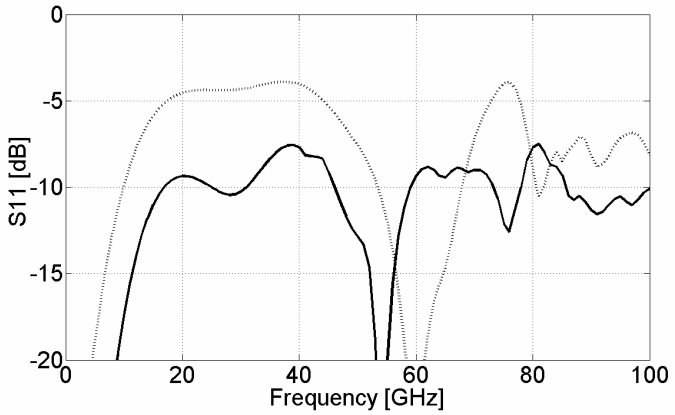

Fig. 5 – graphs of the return loss scattering parameter S11. The black massive line shows the return loss of the optimized setup. The doted dark grey line represents the non-optimized reference setup. Our proposed setup offers a maximum return loss of -7.5dB, equaling less than 18 per cent of undesirable power reflections. The non-optimized setup offers a maximum return loss a considerably worse return loss of up to -4.5dB, equaling 35 per cent of reflected power.

Conclusions

An easily producible matched transition between an on-chip microstrip line and a microstrip line edged on a PCB, for frequencies of up to 100 GHz, has been presented. It has been shown that the proposed setup is superior to the previously used connections. The main advantage is the low loss caused by reflections at the bond wires, as the proposed setup shows characteristics of a matched broadband transmission line. The signal attenuation calculated for the transition is always lower than 2.5dB within 100GHz and even lower than 1dB for a 80GHz within this band. The advancement is caused by just adding additional grounded bond wires that cancel a part of the magnetic field of the signal bond wires, because the ground bond wires carry opposing currents, and additionally cause parallel distributed capacitance to ground – a requirement for transmission line characteristics. Therefore embedding of the chip in a cavity milled out of the PCB is not required by this technique. A fact that saves cost and production time and enables standard soldering techniques for the use of the chip on printed circuits as well as a good connection to ground.

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