# 4-Channel/Antenna Multi-Band RF Transmitter Operating from 525 MHz to 6 GHz

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***Abstract*— A multi-band transmitter front-end featuring four channels in the range from 525 MHz to 6 GHz is presented. This design is perfectly suited for convenient integration into software defined radio (SDR) applications [1]. The transmitter features a shared selectable low phase-noise local oscillator (LO) for carrier frequency generation and 4 direct conversion I/Q-modulators that meet the specifications for spread spectrum (e.g. CDMA2000, UMTS) and OFDM(A) (e.g. WiMAX) systems. The four I/Q channel inputs are designed to be controlled by A/D-converters. So the channels can be used for different sub-channels, operated as MIMO/diversity transmitter, used for digital beam-forming or for a combination of these possibilities. The loosely packed prototype circuit has been designed on a six-layer PCB that measures less than 40 times 80 mm without baseband connectors but including powerful voltage regulators and is thus smaller than an actual mobile handset. For phase or error vector magnitude (EVM) critical systems (especially) in the upper bands, the four transmit paths have been designed for precisely matched delays and transmit powers.**

## I. Introduction

Permanent network connections of different occurrence are becoming ubiquitous for mobile devices and costumer electronics.

The typical frequencies of operation and communication for products in the mass market is going to range from the 700 MHz band, previously auctioned in the US, up to the 5.9 GHz band used for Car2Car-Communication with the IEEE 802.11p standard [2], in the near future.

A major challenge for the development and maintenance for these devices is the permanently growing plurality of standards and frequency allocations for network services. Designing a networked device, which is enabled to communicate with all services of interest, even just for a certain regional area, is a challenge. Designing a comparable device for worldwide interoperability and thus for a lot of different licensed frequency bands is nearly impossible.

The reason is the vast amount of different baseband chips and radio frequency (RF) frontends needed to comply with the huge amount of different standards around the world. Only a portion of the installed electronics is useful in any regional area of the world, but all of the electronics have to be installed, if worldwide applicability is desired.

This leads to increased printed circuit board (PCB) area, additional (standby-) current drain, consequently larger batteries, larger weight of the device, higher bill of material (BOM), device costs and added device volume. In summary: A less attractive and more expensive device; An outcome that is definitely not desired.

For the future of baseband technologies the actually preferred answer to this challenge seems to be SDR. Different companies are continuously developing new products. Like NEC Electronics fully integrated baseband filter with a tuneable bandwidth ranging for 400 kHz to 30 MHz [3], or – for the digital domain – Infineon's new software configurable multi-standard baseband solution for cellular, connectivity and satellite system, that is based on a multi-DSP solution [4]. Thinking of Moore's law [5] the computing power for SDR will be available in the future – not mentioning whether the near or remote future is meant. A summary of the vision and the grade of current feasibility, along with several circuit examples, is presented in [6] and [7].

The design of the analog part of a transmitter is influenced by the laws of physics to a larger extend. A resonant circuit will not feature a higher ability of frequency adaptation just by using a more advanced production process. Building a device that is capable to transmit different signals with two antennas instead of one still requires embedding a second signal chain, whereas baseband for both signals could be covered by a single, but faster processing unit. Details for that condition and design suggestions for mobile SDR hardware can be found in [8].

Based on the preceding thoughts and to achieve the desired and required bandwidth our transmitter design completely abstains from narrow-band techniques for frequency generation, signal distribution, amplification and modulation. To avoid the requirement of IF or RF filters, highly linear direct conversion (homodyne) modulators are used. A very low phase noise voltage controlled oscillator (VCO) controlled by an integer-N phase locked loop (PLL) generates the LO-frequency. The reference frequency for the PLL is made available by a precise fractional-N PLL voltage controlled crystal oscillator (VCXO) synthesizer that is digitally tuneable from 8 to 230 MHz.

## II. Design Considerations

### A. Designated Frequency Bands

Our design goal has been to develop a transmitter for a communication device. The device shall fulfil the requirement to be able to operate within any communication network available to mobile users.

An additional requirement is that the device should be operable in any country on each continent. The design goal of worldwide applicability implies that the transmitter has to be able to work and a large variety of frequency bands. The lowest target frequency is 700 MHz, an old analog television band that is now auctioned off for wireless network use (e.g. in the US) or unused at all since the advent of digital TV technologies and waiting for a new purpose in many countries worldwide.

The pleasant propagation characteristics of this quite low frequency makes it interesting for suburban and rural high data rate networks, like the upcoming 4th generation networks (e.g. IEEE 802.16e mobile WiMAX or the UMTS successor LTE).

The upper operational frequency limit has been set to 6 GHz. This frequency was chosen as the IEEE 802.11p (pre-) standard used for Car2Car-Communication and Car2Infrastructure-Communication is situated around 5.9 GHz. Hence 5.9 GHz is the highest frequency that mass market communication devices are transmitting today. All the other systems of interest are residing between these limiting bands (e.g. UMTS around 2 GHz).

### B. Number of Transmit Channels

In order to expand the capabilities of the transceiver further, four transmit channels have been specified, all of which are able to be modulated individually.

Since all new communication standards employ novel smart antenna technologies, like phased arrays or multiple input – multiple output (MIMO) technologies (WiMAX, LTE, UMB, IEEE802.11n,…), this flexibility is demanded by future usage scenarios. Additionally to phased arrays and MIMO systems, the individual channels can also be used to set up multi-channel transmitters with low Crest-Factor (peak to average power ratio (PAPR)), use transmit diversity technologies or combine any of these techniques.

For instance a mobile WiMAX Wave 2 (MIMO) transmitter combined with a two antenna beamforming for each of the two channels is feasible; in a single channel system like GSM all channels could be used for range extension. Such a four antenna beamforming system offers an array gain of 6 dB and thus a range extension by a factor of two, assuming free space propagation.

### C. Modulation Bandwidth

Channel bandwidths used today and in the near future are between 200 kHz (as GSM) and 20 MHz (maximum for LTE and WiMAX). So 20 MHz are set as the infimum for the modulation bandwidth specs. To allow for multi-channel transmissions as described in section B. a 100 MHz modulation bandwidth was set as goal.

## III. Concept of the Proposed Transmitter

### A. LO Frequency Generation

To reach our design goals, a direct-up-conversion architecture was chosen. The architecture for the LO frequency generation is depicted in Fig. 1. The LO frequency can be precisely adjusted by two settings. The first option is to set the reference frequency by a fractional-N reference PLL-VCXO synthesizer. The second option is to set the divider of the main PLL-VCO synthesizer that is in charge of the final LO frequency generation. By these two settings a very fine carrier frequency setting is possible.

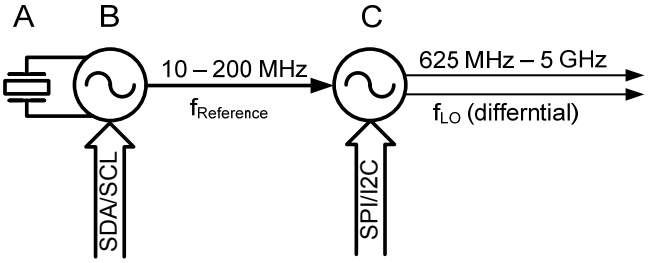


Fig. 1 Block diagram of the frequency generation system. The device marked A is a quartz crystal oscillator resonating between 8 and 32 MHz. Device (B) is the fractional-N PLL-VCXO synthesizer, that uses device (A) as its reference and is able to generate frequencies between the crystal's frequency and 230 MHz. Device (C) accepts 10 – 200 MHz as reference, so the output of device (B) is limited to that values. Device (C) is the LO frequency generator. It is build from a digitally controllable integer-N PLL with integrated VCO synthesizer. Device (C) is able to generate frequencies from 625 MHz to 5 GHz in several bands. This part is replaceable by two different synthesizers with the same pin-out to cover the whole frequency range between these two values. The next version of the transmitter prototype is going to feature switchable LO generators to cover the complete frequency range. The arrows on the bottom of this figure represent the digital busses used to control the frequency system.

### B. LO amplification and distribution network

The LO frequency is generated as a differential signal by the PLL-VCO synthesizer. The output power of the synthesizer has a typical level of 0 dBm. As each of the four modulators needs a drive level of -6 to +7 dBm, the need for amplification arises.

Additionally to the power division (-6 dBm for 4 sinks) the divider network itself also inserts attenuation. The challenge for the distribution of the LO frequency signal is the wide range of frequencies. Nearly all power divider technologies are narrow banded. A lot of different power dividing strategies have been evaluated for that reason. For instance the popular Wilkinson divider has a relative bandwidth of approximately 20 percent, not compliant to our specifications. Transformer based dividers (e.g. [9]) offer comparatively low insertion loss and a nearly satisfactory bandwidth, but have different disadvantages that hinder implementation. Their technical downside is non-satisfactory matching of the output signal's phase and amplitude. But there is also a severe economic drawback. The up to date technically best qualified part [9] is not feasible for mass production as it is rather large (6.35x7.87x5.08 mm) and way to expensive for a consumer product (about 20$ each, three would be needed).

As none of the evaluated low loss variants meets the major design goals, another suboptimum but specification compliant variant – the resistive divider – has been chosen. This resistive divider has one input port and four output ports. The ports are connected in star topology with five 30 Ohm resistors, so each port is matched to 50 Ohms, the characteristic impedance of the microstrips.

Unfortunately a resistive divider for four channels inserts additional 12 dB of attenuation ($1/4^{th}$ of the power (-6 dB) for each channel and 6 dB of losses). Hence the differential LO signal has to be amplified by at least 6 dB to meet the driving requirement of the modulators.

For this amplification a single ended broadband amplifier with an extensively frequency independent gain of 12 dB has been used for each of the two lines carrying the differential signal.

The lengths and attenuations of all paths have to be precisely the same to avoid phase and amplitude imbalance. For the connection of all modulators crossings of the LO+ and the LO- signals are not avoidable. A well performing method would be to use [10]. But to avoid a different count of RF signal crossings of the differential LO signals, the synthesizer and the modulators are situated on different sides of the printed circuit board (PCB), separated by two ground planes. This allows using exactly one similar top-layer to bottom-layer transition in each LO+ and LO- signal path and thus amplitude matched and equally phased signals. The LO distribution and amplification is shown in figure 2.

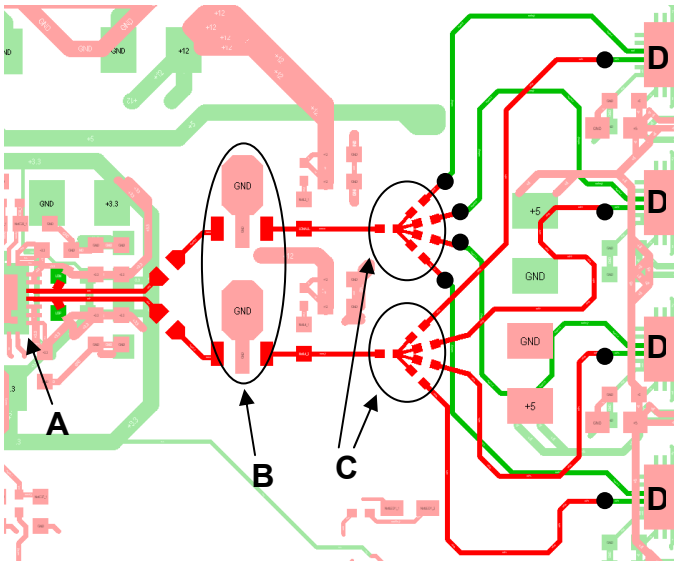


Fig. 2 The local oscillator frequency distribution network is shown. The LO tracks are highlighted by higher color saturation. Tracks on the PCB's top are shown in red/dark grey, tracks on the bottom are plotted green/medium grey. Non highlighted tracks from the actual PCB's layout are depicted in pallid colours. The LO generator is marked with (A), two tracks with the LO+ and the LO- signals are leading towards the two single ended 12 dB gain amplifiers, which are marked as (B). The next steps in the signal chain are the resistive power dividers (C), consisting of five 30 Ohms resistors each. They split the incoming wave in four phase and amplitude matched signals. To avoid signal crossings on the same board side (as possible with [10]), the modulators (D) are placed on the bottom of the board to get exactly one via transition (black dots) in each signals track.

For a homodyne system without intermediate or radio frequency filtering it is mandatory to keep the error vector magnitude (EVM) and the spurious emissions as low as possible. To get a picture of the expectable signal perturbance, the signal levels in between the signal chain's building blocks have to be reviewed. The level plan is depicted in Table I.

TABLE I
LEVEL PLAN OF THE TRANSMITTER, TYPICAL VALUES

| **Component** | **Gain [dB]** | **Output Level [dBm]** | **Output IP3 [dBm]** | **1 dB GCP [dBm]** |
|---|---|---|---|---|
| PLL-VCO | - | 0 | - | - |
| Track and Capacitor | -0.2 | -0.2 | - | - |
| Amplifier | 12 | 11.8 | 35 | 20 |
| Resistive Divider connecting Track | -12.5 | -0.7 | - | - |
| Track to Modulator | -0.3 | -1 | - | - |
| Incoming Power at the LO Port of the Modulators: -1dBm | | | | |
| Modulator *frequency dependent values | ~ 2* | 0 – 2* | 13 – 30* | ~ 10 (6 @ 5 GHz+) |

The listing of the power level values shows that all levels are well within the linear range of the building blocks, as the signal level is very well below the third order intercept point (IP3) and the 1 dB gain compression point (1 dB GCP).

### C. *Array of Modulators*

The Array of modulators is fed by LO signals of equal phase and amplitude for any frequency setting, because the line length and attenuation has been matched. This is important especially for the use of the four channels as a four antenna beamforming array, due to the fact that the pointing direction is controlled by phase differences there. Different line length and attenuation could be compensated in the digital signal domain, but this would require additional processing power for the correcting vector multiplication (1). Where M is the desired signal point from the constellation diagram, A is the attenuation of the line, λ is the actual wave length and Δl is the line length deviation.

$$M_{corrected} = M \frac{1}{A} e^{\frac{-j2\pi\Delta l}{\lambda}} \qquad (1)$$

Since the line lengths are equal this correction can be omitted and the carrier can be directly modulated by the desired I/Q symbols. The used modulators offer an output frequency range of 400 MHz to 6 GHz. The modulation bandwidth within 0.1 dB of gain variation is 100 MHz.

The modulators offer an output power of 0 to 2 dBm, depending on the frequency setting, resulting in an overall transmitter output power of 6 to 8 dBm.

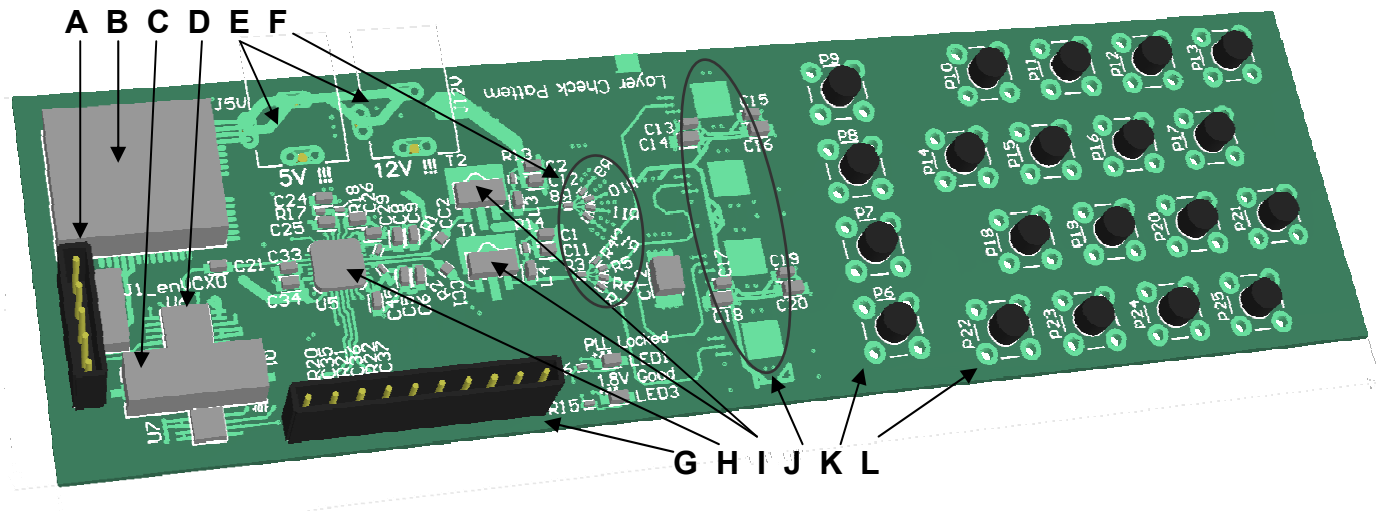


Fig. 3 Three dimensional plot of the developed transmitter board. The complete board measures 40 times 140 mm; the transmitter without the prototype connectors is 40 times 80 mm, including the digital pinout and low voltage converters. The digital connections for the reference oscillator are marked with (A). (B) is a low noise switching power regulator capable of providing 1.5 amperes at a voltage of 3.3 volts. The reference crystal (C) is placed very closely to the reference PLL-VCXO (D) to avoid line inductance and parasitic capacitance. The 5 and 12 volt connectors are marked with (E). (F) shows the power dividers, previously described in section III. B. and Fig. 2. The SPI/I²C control connection of the main PLL VCO (H) is marked as (G). The LO+ and LO- lines are individually boosted by the broadband amplifiers (I). (J) shows the top side cooling pads of the modulators. The modulators themselves are placed on the bottom of the PCB to allow matched LO signals to all modulators (details in section III. B.). The array of the four single ended an AC-coupled antenna outputs are labelled (K). The last item (L) shows the array of baseband I/Q inputs. I/Q signals are fed differentially, so 4 connectors per channel are required.

### *D. Digital Control Interface*

The reference oscillator is controlled by an SDA/SCL interface. Via this interface the divider ratios of the PLL can be set, outputs can be switched on and off and the power saving mode is controllable. The main oscillator is controlled by an SPI/I²C interface. VCO output amplitude, charge pump current, counters and divides can be controlled by that interface.

Further a VCO auto-calibration can be commanded or the lock detector flag can be read.

## IV. Conclusions

The concept and development of a very flexible four-channel transmitter prototype has been shown. The transmitter is now being manufactured and measurements will be included in the final document.

The device operates in frequencies between 625 MHz and 6 GHz. This set of frequencies allows the proposed architecture to be operated worldwide without any change in design.

Four channels are individually controllable. They feature individual inphase and quadrature inputs. These features allow using the antennas for different multi-antenna schemes. Examples are transmit diversity, MIMO, phased array antennas, low PAPR multichannel design without the need for a digital crest factor reduction engine and further multichannel and multiantenna technologies.

The design without prototype connections is small enough to fit inside even small consumer equipment before optimization for space.

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