# UHF RFID Transponder Chip and Antenna Impedance Measurements

*Jasmin Grosinger, Christoph F. Mecklenbräuker and Arpad L. Scholtz*
*Vienna University of Technology*
*Institute of Communications and Radio-Frequency Engineering*
*Gusshausstrasse 25/389, 1040 Wien, Austria*
*jasmin.grosinger@tuwien.ac.at*

***Abstract*** **- The communication performance between reader and transponder in radio frequency identification (RFID) in the ultra high frequency (UHF) range strongly depends on the matching between transponder chip and transponder antenna. To assure power optimization in the forward link the input impedance of the antenna must be the complex conjugate of the chip's input impedance. In this contribution a measurement method is introduced to determine the transponder chip's input impedance in absorbing mode versus chip input power. A prematching test setup with impedance tuners assures high measurement accuracy. Additionally, an antenna is presented which is designed to perfectly match the chip. Its input impedance is simulated and measured versus frequency. Finally, the matching between chip and antenna is calculated in terms of a power transmission coefficient.**

## I. INTRODUCTION

Radio frequency identification (RFID) in the ultra high frequency (UHF) range relies on the wireless communication between an interrogator (or reader) and one or more transponders (or tags) [1]. In the forward link the reader transmits radio frequency (RF) power and data to the tag. Because in passive RFID a tag does not have its own power supply, all power required for the operation of the tag must be drawn from the electromagnetic field radiated by the reader. In the return link – whenever a reader command requires a tag response – the tag starts its data transfer using modulated backscattering. This means, the signal from the reader is partly reflected by the tag depending on the data to be transmitted to the reader.

An RFID tag consists of a chip and an antenna. Depending on the match or the mismatch between chip and antenna impedance, power is absorbed or reflected by the tag. Thus – to realize modulated backscattering – the chip changes its input impedance to reach reflection of the RF power received from the reader. This is achieved with a shunt transistor that is implemented in the transponder chip. Switching on the transistor destroys the impedance matching between chip and antenna which results in power reflection at the chip.

The matching of tag antenna and chip strongly influences the communication performance between reader and tag. Since the input impedance of a chip cannot be chosen arbitrarily due to technological limits, the antenna has to be designed to match the chip's impedance. In [2] it is found that for a given transponder chip, there exists two distinct optimum antenna impedances. One maximizes the power available for the chip's internal circuitry – this means power optimization of the forward link – and one maximizes the signal that is reradiated towards the interrogator – this means power optimization of the return link. The power matching condition to optimize the forward link is $Z_{ant} = Z^*_{chip1}$. $Z_{ant}$ is the antenna impedance. $Z_{chip1}$ is the chip impedance in absorbing state – absorbing impedance – with the shunt transistor switched off. The chip impedance in reflecting state with the shunt transistor switched on is denoted as reflecting impedance. If this matching condition is realized, the entire power available at the tag antenna can be used by the chip.

To realize matching between chip and antenna, the knowledge of the chip impedance is mandatory. In [2] the chip input impedances in both the absorbing and the reflecting state as a function of input power of commercially available RFID chips are determined using a measurement setup which provides a carrier modulated with a command sequence that causes the transponder chip to respond. Additionally, to assure high measurement accuracy a prematched impedance test setup with tuners is implemented. Monitoring both impedances over chip input power leads to the minimum input power, which is necessary to operate the chip, known as chip sensitivity. The obtained quantities – input impedance and sensitivity – are in good agreement with the chip manufacturers data sheets. In [3] the chip impedance versus power and frequency of two commercially available RFID chips is measured in absorbing mode, however no prematching is performed. The chip sensitivity is determined using a specially designed RFID reader.

In this paper the input impedance of an RFID transponder chip in absorbing state is measured versus chip input power. A prematching test setup with two double-slug tuners is used to assure high measurement accuracy. Following the chip impedance measurement, a specially designed antenna is investigated referring its input impedance. The antenna impedance is measured versus frequency, the used measurement method was first introduced in [4]. Finally, the match between chip and antenna is computed in terms of a power transmission coefficient.

## II. CHIP IMPEDANCE MEASUREMENT

The input impedance in absorbing state is measured versus chip input power of a UHF RFID transponder chip including its package – $Z_{chip1} = R_{chip1} + \jmath X_{chip1}$ – with a prematching test setup introduced in [2]. Typical input impedances of passive UHF transponder chips are highly reactive. When such a chip is directly connected to a $50\,\Omega$ system of a vector network analyzer (VNA) to measure its input impedance, a large voltage standing wave ratio (VSWR) occurs on the measurement cable due to large reflections at the chip input. The accepted power of the chip could in principle be calculated from the VNA's source power and the reflection coefficient determined at the chip's input. However, at small input powers measurement errors occur at the chip's input impedances because of small signal-to-noise ratios in the VNA. At high VSWRs any measurement error of the reflection coefficient strongly impacts the accepted power determined in this way [5]. To increase the measurement accuracy and decrease the VSWR, impedance tuners are used to provide static prematching between the $50\,\Omega$ output of the VNA and the chip. The tuners are set to provide the conjugated chip input impedance. This prematching transforms the transponder chip impedance into the $50\,\Omega$ system impedance leading to more accurate measurement results due to a VSWR of almost $1:1$.

The chip measurement setup is depicted in Figure 1. A VNA (R&S ZVA24) is used to measure the chip's input impedance. Two double slug tuners (Microlab/FXR SF-11S) provide the prematching of the chip to the $50\,\Omega$ measurement system. The chip is connected to the tuners via a miniature coaxial connector (U.FL series by Hirose Electric Co. LTD.) mounted on a custom-built test fixture. To shift the measurement reference plane to the chip's input pins, a calibration with match, short, and open standards is done after prematching. Test fixture and custom-built calibration kit – printed on FR-4 substrate with a thickness of 1.6 mm – can be seen in Figure 2. A power meter (R&S NRP-Z11) is used to perform a power calibration directly at the tuner input. Assuming matching between tuners and chip, a constant power loss of 0.8 dB is introduced by the tuners. The signal which is applied to the chip does not contain any information or a wake-up signal for the chip. Thus, the chip is in absorbing mode during measurement and does not start processing any data.

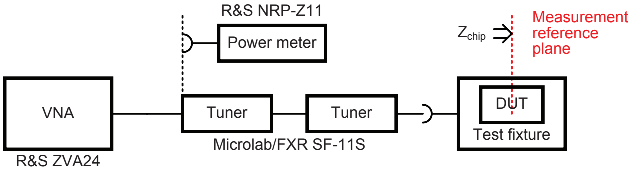

FIGURE 1 - CHIP IMPEDANCE MEASUREMENT SETUP

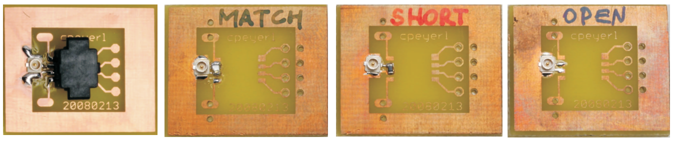

FIGURE 2 - TEST FIXTURE AND CALIBRATION KIT FOR CHIP MEASUREMENT

As a result of static prematching, the matching between chip and tuners changes quite significantly with increasing power. This is because the chip's impedance varies for different input powers. In Figure 3 the reflection coefficient $|S_{11}|$ at the input of the tuners with the chip as load is depicted versus the input power at the tuners $P_{tuner}$ for a frequency $f = 864\,\mathrm{MHz}$. It can be seen that matching is achieved at small input powers, i.e. matching is achieved at the chip's absorbing impedance $Z_{chip1}$. At higher power levels the absorbing impedance converges to the reflecting impedance [2]. The reason for this is that the shunt transistor is intentionally turned on to regulate the internal power supply of the chip. In summary, this prematching achieves that when the chip is in absorbing mode all available power is provided to the rectifier and no power is returned. Thus, the presented measurement is very accurate for a power range of $-30\,\mathrm{dBm}$ to $-10\,\mathrm{dBm}$, since in this power range the VSWR is very small due to the prematching.

For calibration of the VNA, three calibration standards – match, short, and open – are designed [6]. The match standard is equipped with a parallel circuit of a $910\,\Omega$ resistor and a $0.5\,\mathrm{pF}$ capacitor. The big capacitance of $0.5\,\mathrm{pF}$ should dominate the parallel circuit referring to non-ideal effects due to the resistor's parasitic capacitance. Using a $50\,\Omega$ resistor as a calibration standard is not optimal for calibrating this measurement setup. More accurate calibration in a prematched setup is achieved when a match standard that minimizes reflections at the load is used. This is achieved with the introduced standard. Measurements of the match standard after prematching and calibration leads to an impedance of $Z_{match} = (129.4 - \jmath 317.7)\,\Omega$ at a frequency of $f = 864\,\mathrm{MHz}$. This corresponds to a parallel resistance of about $909\,\Omega$ and a parallel capacitance of about $0.497\,\mathrm{pF}$, and agrees well with the defined standard. The short standard is equipped with a $0\,\Omega$ resistor, while the open standard is left empty. Table 1 lists the definition of the calibration standards in the VNA – parallel resistance $R$ and parallel capacitance $C$.

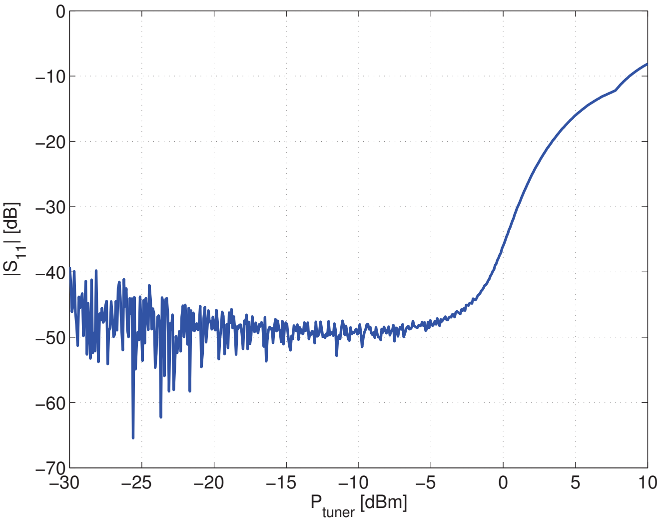

FIGURE 3 - INPUT REFLECTION COEFFICIENT $|S_{11}|$ OF TUNERS WITH CHIP AS LOAD VERSUS TUNER INPUT POWER $P_{tuner}$ AT $f = 864\,\mathrm{MHz}$

TABLE 1 - DEFINITION OF CALIBRATION STANDARDS FOR CHIP MEASUREMENT

| **Standard** | $R$ [Ω] | $C$ [pF] |
|---|---|---|
| Match | 910 | 0.5 |
| Short | 0 | 0 |
| Open | ∞ | 0 |

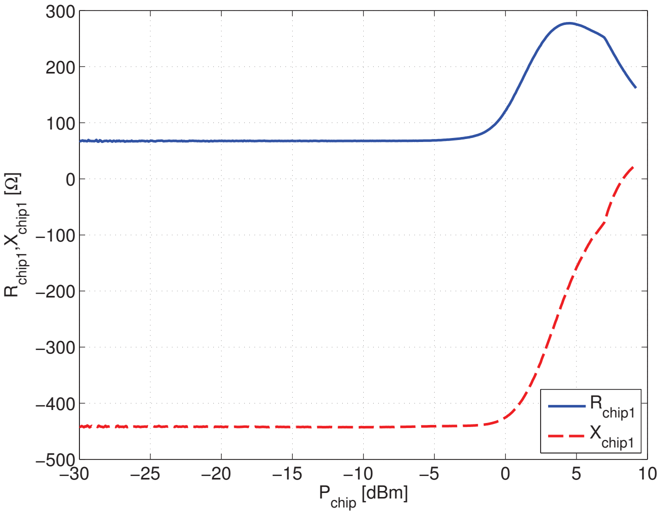

FIGURE 4 - CHIP IMPEDANCE IN ABSORBING MODE $Z_{chip1}$ – RESISTANCE $R_{chip1}$ AND REACTANCE $X_{chip1}$ – VERSUS CHIP INPUT POWER AT $f = 864\,\mathrm{MHz}$

The measured chip impedance in absorbing mode is $Z_{chip1} = (68 - \jmath 442)\,\Omega$ for low power at $f = 864\,\mathrm{MHz}$. The results can be seen in Figure 4. Resistance $R_{chip1}$ and reactance $X_{chip1}$ are plotted versus chip input power $P_{chip}$ (including tuner losses) for $f = 864\,\mathrm{MHz}$. The absorbing impedance of the chip changes drastically at higher power levels. This shows the above mentioned switch-on of the shunt transistor at higher chip input power to protect the chip's internal circuit. Knowing the chips absorbing impedance, it is possible to design an RFID tag antenna matched to optimize the forward link between reader and tag.

## III. ANTENNA IMPEDANCE MEASUREMENT

To realize optimum power transmission in the forward link of the RFID system, an antenna impedance of $Z_{ant} = R_{ant} + \jmath X_{ant} = R_{chip1} - \jmath X_{chip1} = Z^*_{chip1}$ is required for the microchip conjugate impedance matching at a specified frequency. In this case the complex conjugate of the absorbing impedance $Z_{chip1} = (68 - \jmath 442)\,\Omega$ at $f = 864\,\mathrm{MHz}$. Usually, most of the UHF antennas for omnidirectional tags are commonly fabricated as modified printed dipoles. To achieve a high reactive input impedance at the dipole's input several feeding strategies can be adopted for antenna tuning. One matching technique embedded in the tag antenna's layout uses a T-feed [7]. A dipole with T-feed – printed on FR-4 substrate with a thickness of $1.6\,\mathrm{mm}$ – is first implemented with Ansoft's high frequency structure simulator (HFSS) to design an antenna with an input impedance of $Z_{ant} = (68 + \jmath 442)\,\Omega$ at $864\,\mathrm{MHz}$, i.e., the tag's resonance [8] lies at $864\,\mathrm{MHz}$. The dimensions obtained by simulation can be seen in Figure 5. Second, the antenna is realized and its input impedance is verified by measurement.

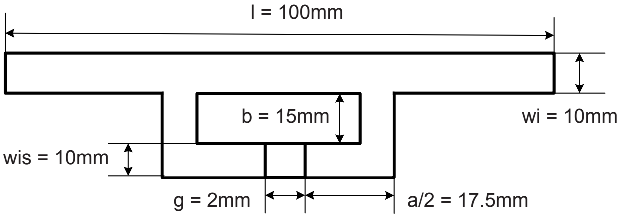

FIGURE 5 - ANTENNA DIMENSIONS

For verification the input impedance of the tag antenna designed is measured versus frequency. Figure 6 shows the measurement setup first introduced in [4]. With a VNA (R&S ZVA24) the reflection coefficient at the input of the antenna is measured. A symmetric feed is realized with a true differential signal directly from the VNA – an unsymmetric feed must be avoided for the symmetric dipole antenna, because it introduces common mode currents that will cause radiation and alter the antenna's properties. The antenna is fed by two flexible $50\,\Omega$ coaxial cables. They are connected to the antenna via miniature coaxial connectors (U.FL series by Hirose Electric Co. LTD.) mounted on FR-4 substrate (thickness: $1.6\,\mathrm{mm}$). This can be seen in Figure 7. To maintain additional symmetry the coaxial cables are fixed together with a heat shrink tube.

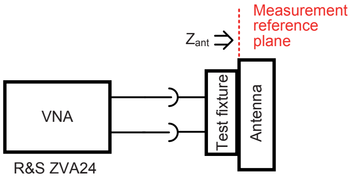

FIGURE 6 - ANTENNA IMPEDANCE MEASUREMENT SETUP

A custom-built calibration kit [6] made of FR-4 substrate (thickness: $1.6\,\mathrm{mm}$) – including match, short, open, and through standard – is used to shift the measurement reference plane directly to the input of the dipole. The match standard is equipped with a parallel circuit of two $100\,\Omega$ resistors. Figure 8 shows the calibration kit and Table 2 lists the parallel resistances $R$ of the defined standards.

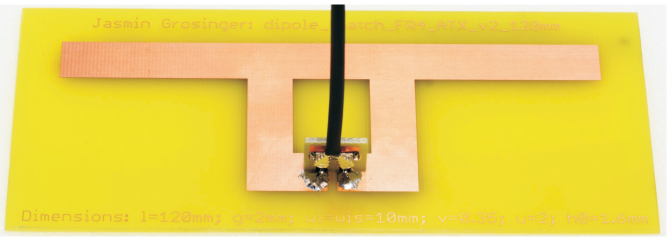

FIGURE 7 - FEEDING STRUCTURE FOR ANTENNA MEASUREMENT

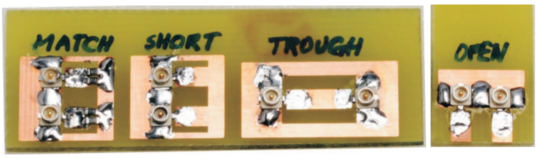

FIGURE 8 - CALIBRATION KIT FOR ANTENNA MEASUREMENT

TABLE 2 - DEFINITION OF CALIBRATION STANDARDS FOR ANTENNA MEASUREMENT

| **Standard** | **$R$ [Ω]** |
|---|---|
| Match | 50 |
| Short | 0 |
| Open | ∞ |
| Through | 0 |

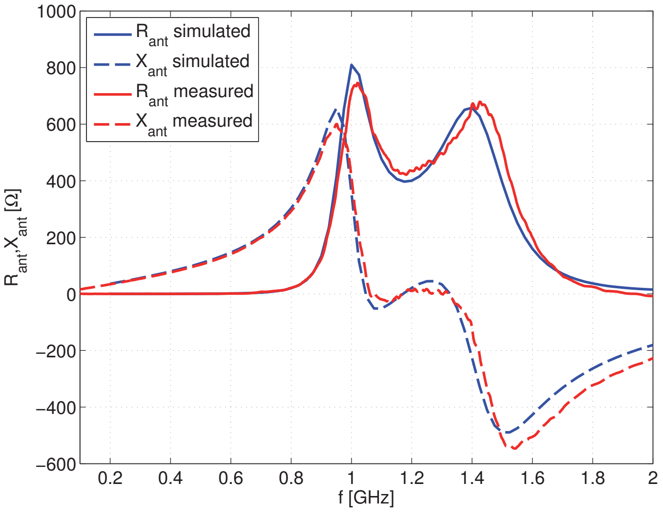

FIGURE 9 - SIMULATED AND MEASURED ANTENNA IMPEDANCE $Z_{ant}$ - RESISTANCE $R_{ant}$ AND REACTANCE $X_{ant}$ - VERSUS FREQUENCY AT $P_{VNA} = 0\,\mathrm{dBm}$

In Figure 9 measurement and simulation results of the antenna's input impedance – real part $R_{ant}$ and imaginary part $X_{ant}$ – versus frequency $f$ are depicted. The power of the VNA source is $P_{VNA} = 0\,\mathrm{dBm}$. From Figure 9 it can be seen that measurement and simulation results agree well and that the antenna measurement method is highly applicable to determine the input impedance of symmetric antennas. The simulated input impedance of the designed antenna is $Z_{ant,simulated} = (65 + \jmath 423)\,\Omega$ at a frequency of $f = 864\,\mathrm{MHz}$.

## IV. MATCHING OF CHIP AND ANTENNA

The quality of the match between the chip in absorbing state and the developed antenna can be evaluated using the definition of the power transmission coefficient $\eta_m$. The power transmission coefficient is the ratio of the power accepted by the transponder chip and the available power at the antenna port. A high transmission coefficient maximizes the power available for the chip's internal circuitry and assures a power optimization of the forward link. $\eta_m$ is defined as [8]

$$\eta_m = \frac{4 R_{ant} R_{chip1}}{|Z_{ant} + Z_{chip1}|^2}.$$

For a chip impedance of $Z_{chip1} = (68 - \jmath 442)\,\Omega$ and an antenna impedance of $Z_{ant} = (65 + \jmath 423)\,\Omega$ at a frequency of $f = 864\,\mathrm{MHz}$ the power transmission coefficient is

$$\eta_m = 98\,\% = -0.09\,\mathrm{dB}.$$

In Figure 10 isolines of the power transmission coefficient for the chip impedance of $Z_{chip1} = (68 - \jmath 442)\,\Omega$ are plotted versus different antenna impedances. The antenna impedance of the designed dipole with T-feed lies within the $-0.1\,\mathrm{dB}$-isoline. This means, a good match is achieved between chip and antenna.

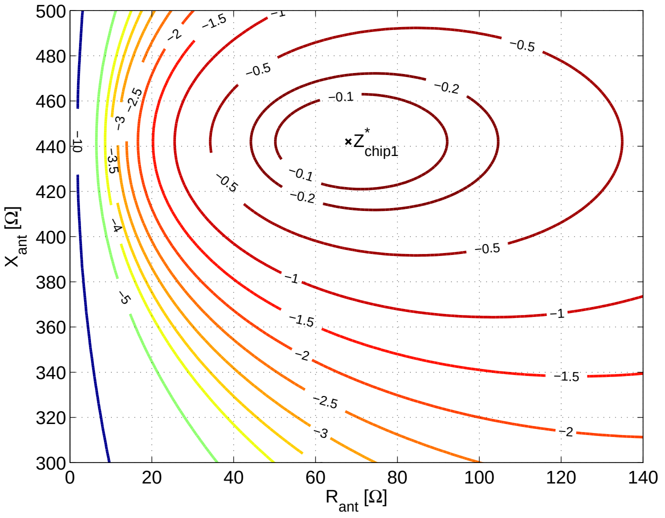

FIGURE 10 - POWER TRANSMISSION COEFFICIENT IN DECIBEL VERSUS ANTENNA IMPEDANCE

## V. CONCLUSION

UHF RFID transponder chip and antenna are investigated referring to their input impedances. With a prematching test setup an absorbing chip impedance of $Z_{chip1} = (68 - \jmath 442)\,\Omega$ is determined at a frequency of $864\,\mathrm{MHz}$. A custom-built antenna – designed to reach a tag resonance at $864\,\mathrm{MHz}$ with the chip – is investigated by simulation and measurement. Its input impedance is determined versus frequency. The measurement method used assures a differential input signal at the symmetric antenna input and thus overcomes errors due to common-mode currents. A good agreement of simulation and measurement is found. The antenna's impedance is $Z_{ant} = (65 + \jmath 423)\,\Omega$ at $864\,\mathrm{MHz}$. With this, a match between chip and antenna to maximize the power transmission of the UHF RFID system in forward direction is granted. The power transmission coefficient – the power accepted by the chip to the power available at the tag antenna input – is $98\,\% = -0.09\,\mathrm{dB}$. From this it follows that only a small part of the power available at the tag antenna input is reflected at the chip.

## ACKNOWLEDGEMENTS

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