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Modeling Switched Capacitor Sigma Delta Modulator Nonidealities in SystemC-AMS

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***Abstract*—For the design of complex systems both accurate and abstract models are required. Especially for analog subsystems this trade-off is difficult. The new SystemC AMS extensions [7] offer high simulation performance, but also serious restrictions. In this paper we model a switched capacitor sigma delta modulator using the SystemC AMS extensions. The model combines high simulation performance while modeling sampling jitter, kT/C noise, switch non-linearities and operational amplifier non-idealities (such as finite gain, finite bandwidth, slew rate, leakage and saturation effect). We present a complete set of sub-modules representing those non idealities implemented in SystemC-AMS. Finally, the proposed sub-modules are used to simulate a low-pass second order sigma delta modulator of which results are presented.** †

I. Introduction

In complex HW/SW/Analog systems functionality of the domains is more and more interwoven. Good examples are software controlled radio, or integrated sensor systems where DSP software compensates and corrects non-idealities of analog subsystems. For the development of such systems, models are required that model most important non-idealities and that allow overall system simulation over a longer time period, e.g. for estimation of bit error rates. ADCs are of particular importance for the overall functionality.

Sigma Delta($\Sigma\Delta$) ADCs are widely used in applications where low-bandwidth and high-resolution (up to 20 bits) is required; like sensor interfaces, instrumentation/measurement, audio etc. Apart from the advantage of high resolution, $\Sigma\Delta$ ADCs are mostly digital, there is no requirement of a sample and hold circuit(and hence no need of a large sampling capacitor) makes it feasible in less area. Being inherently linear with robust analog implementation, $\Sigma\Delta$ modulators reduce the need of trimming for its constituent components which in turn reduces the cost.

Although it is very easy to obtain an analytic equation of $\Sigma\Delta$ modulators based on finite difference equation method, it does not consider several real life parameters which in turn gives out non-idealities and non-linearities associated with them. In case of high performance systems, inter dependence of these parameters plays an important role in designing an accurate(and sufficient) $\Sigma\Delta$ modulator which in turn enforces requirement of optimization of all these parameters among themselves in order to ensure high-performance requirements of $\Sigma\Delta$ ADC. It is therefore important to determine these optimized parameters based on time domain simulation of a model which incorporates all these parameters and their effects in order to ensure the desired performance of the $\Sigma\Delta$ ADC.

$\Sigma\Delta$ modulators can be continuous time or discrete time in nature, depending on the integrators used. In this work we selected switched capacitor (SC) $\Sigma\Delta$ modulator keeping it's requirement in mind. Following are the factors which affects performance of a SC $\Sigma\Delta$ modulator:

1) Sampling Jitter,
2) k_BT/C_S Noise,
3) Switch Non-linearity,
4) Integrator Imperfections like as follows,
    a) Integrator Leakage,
    b) OPAMP Gain Bandwidth,
    c) OPAMP Slew Rate,
    d) OPAMP Noise and
    e) OPAMP Saturation

Circuit level models determine these parameters accurately but set a high penalty in terms of development time as well as execution time. Analog behavioral description languages like Verilog-AMS or VHDL-AMS are expressive in this context, but extremely susceptible to convergence issues (as switched capacitor models are involved with it) and hence development of such a simulation environment/model using Verilog-AMS/VHDL-AMS at first instance is not desired.

$State\text{-}of\text{-}Art$ modeling techniques involve modeling using algorithm designing tool like Matlab/Simulink ([1],[2] and [3]) lack granularity and are slow in execution speed, moreover not suitable for such kind of development.

In this work the SystemC AMS 1.0 extensions have been selected to model sub-modules, and model $\Sigma\Delta$ modulator top-level with those sub-modules in order to have a higher speed of simulation without compromising on accuracy of simulation. The selection of SystemC AMS extensions to model non-idealities enables easy integration with SystemC discrete event modules and hence easy development HW/SW co-simulation platform without the need of a foreign language interface. Non-idealities introduced as a perturbation from the ideal behavior enables early analysis and design of adaptive algorithms needed to correct the effect of non-idealities arising

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in real silicon.

Compared with State-of-the-Art, the proposed model using the SystemC AMS extensions

- can easily be integrated in HW/SW co-simulation platforms due to the C-based approach,
- uses simple equations and directed signal flow, and
- has very high simulation performance.

A particular difficulty in developing the model were restrictions of the SystemC AMS extensions. We therefore discuss and propose some additional features that make modeling easier while maintaining high simulation performance.

II. Sampling Jitter

The SC circuit samples input data where once if data is sampled, the variation of clock period has no direct effect on the circuit performance. Thus the effect of clock jitter can be incorporated in the system as imperfection associated with the sampling of input signal, which also means that sampling jitter is independent of structure and order of modulator [1].

Consider a perfect signal $x(t)$ being sampled by clock signal which has jitter, producing an error in time δt. From the definition of derivative we can write

$$\frac{x(t+\delta t)-x(t)}{\delta t} \approx \frac{dx}{dt} \tag{1}$$

$$\epsilon_{jitter} = x(t+\delta t)-x(t) \approx \delta t \frac{dx}{dt} \tag{2}$$

Where ϵ_{jitter} is the error associated with jitter. From this expression, the equation for the imperfect signal after sampling containing jitter error will be,

$$x(t+\delta t) = \epsilon_{jitter} + x(t) \tag{3}$$

$$or, x(t+\delta t) = x(t) + \delta t \frac{dx}{dt} \tag{4}$$

The coefficient δt in the Equation 4 is of interest and considered to be a random distribution representing jitter. This distribution is considered to be Gaussian as jitter in electrical circuit is caused by thermal noise, which is Gaussian in nature. The sampling uncertainty δt is a Gaussian random process with standard deviation $\Delta\tau$ [2].

Fig.1 Represents the block level description of jitter model which has been directly extracted from equation 4. This is to mention that *Delta* is the jitter coefficient which acts as a parameter, which needs optimization.

III. k_BT/C_S Noise

The source of thermal noise is the thermal excitation of charge carriers and is always active in a device. In Fig.2, in a single ended switched capacitor integrator C_S is the sampling capacitor which is periodically charged and discharged by four switches as shown. C_S is in series with a switch with ON resistance R_{on} which injects a noise voltage onto the capacitor. This is often known switch thermal noise. The total noise power is given by as follows [2],[1]

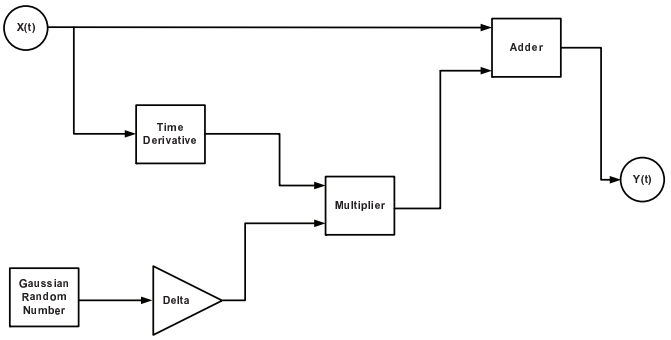

Fig. 1. Block Level representation of Jitter

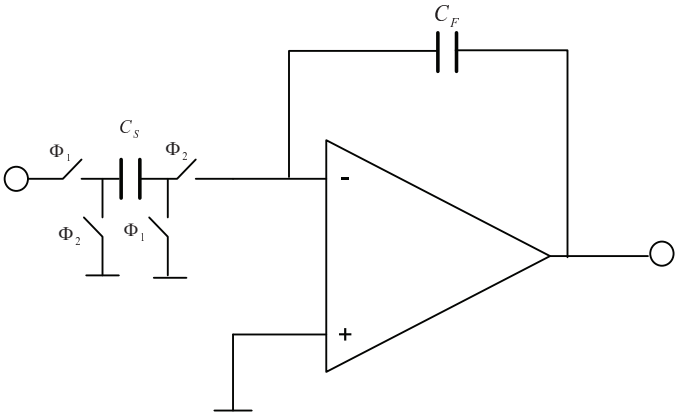

Fig. 2. Switched Capacitor Integrator

$$e_T^2 = \int_0^\infty \frac{4k_BTR_{on}}{(1+2\pi fR_{on}C_S)^2} = \frac{k_BT}{C_S} \tag{5}$$

where k_B is the Boltzmann constant and T is the absolute temperature. From Equation 5, switch thermal noise has been derived as

$$e_T(t) = \sqrt{\frac{k_BT}{C_S}}n(t) \tag{6}$$

where $n(t)$ is the Gaussian random process with unity standard deviation. $e_T(t)$ has to be added with the input signal to generate the effect of switch thermal noise.

IV. Switch Nonlinearity

Considering the load conditions of drain and source of a transistor as well as clock waveform it is difficult to model the charge voltage accurately [3]. In order to model the effect of switch non-linearity, it is considered that CMOS switch has a finite non zero resistances when it is either on (R_{on}) or off (R_{off}). In Fig.2, when ϕ_1 is closed the capacitor C_S starts charging with a time constant $2R_{on}C_S$ and the charging takes place through the time $T_S/2$, where T_S is the period of the clock. This might affect the settling of the signal when the clock frequency is high. The settling equation in such cases can be modeled as

$$V_{out}(t) = V_{in}(t)(1 - e^{-\frac{Ts/2}{2R_{on}C_S}}) \quad (7)$$

The MOS equation for current represents a parabola when it is operated in triode region. In order to ensure the current-voltage linearity, in case of MOS switches, it is always operated in deep triode region where the current-voltage relationship is almost linear. R_{on} for such switches are given by

$$R_{on} = \frac{1}{\mu C_{ox}(\frac{W}{L})[V_{GS} - V_{TH} - V_{DS}]} \quad (8)$$

In case of complimentary switched the W/L ratio is kept same in order to reduce the clock feed-through effect and hence the ON-resistance for a complementary MOS switch can be written as

$$R_{on} = \frac{R_{onp}R_{onn}}{R_{onp} + R_{onn}} \quad (9)$$

Equations 7,8 and 9 together represents the settling effect of C_S due to the switch parameter selection and allows the designer to obtain an optimized switch size against the selected C_S.

V. Integrator Imperfections

SC integrators are important constituent module for SC $\Sigma\Delta$ modulators. Non-idealities associated with SC integrators are of utmost interest as they sets major hinder while designing a high performance $\Sigma\Delta$ ADC.

$$H(z) = \frac{\beta}{1 - z^{-1}} \quad (10)$$

$$H(z) = \frac{\beta z^{-1}}{1 - z^{-1}} \quad (11)$$

Equation 10 and 11 represents simple discrete time model for delay-free and delayed integrators, where β is integrator gain. It can be easily calculated from Fig.2 that the factor β is C_S/C_F which is actually the closed loop gain for the OPAMP shown in the same figure. Thus for a chosen OPAMP as the constituent component for the SC integrator with open loop gain A_{OL} and open loop bandwidth F_{OL}, the closed loop bandwidth becomes

$$F_{CL} = \frac{A_{OL}F_{OL}}{A_{CL}} = \frac{A_{OL}F_{OL}}{C_S/C_F} \quad (12)$$

Equation 12 is extremely important which forms the basis of this section which will be clear in upcoming sections.

A. Integrator Leakage

Equation 10 and 11 represents ideal integrators where the DC gain should be infinite(undefined). The A_{OL} of the constituent OPAMP limits the DC gain of integrator by feeding some part of the integrator output onto it's input, traditionally which is known as leakage. Equations 10 and 11 in the presence of leakage modifies themselves as following

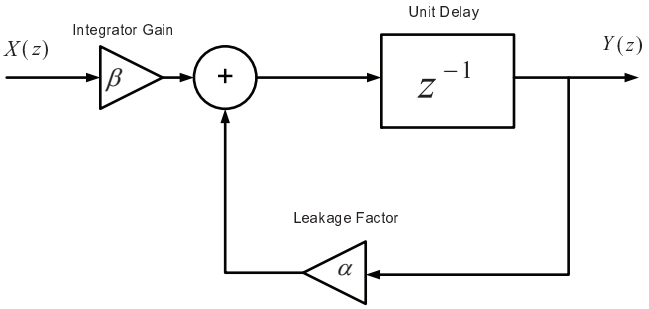

Fig. 3. Block Level Representation of Discrete Time Integrator

$$H(z) = \frac{\beta}{1 - \alpha z^{-1}} \quad (13)$$

$$H(z) = \frac{\beta z^{-1}}{1 - \alpha z^{-1}} \quad (14)$$

where α is the feedback factor responsible for the leakage. The value of α is as follows [5]

$$\alpha = (1 - \mu) \quad (15)$$

$$\mu = \frac{A_{CL}}{A_{OL}} = \frac{C_S/C_F}{A_{OL}} \quad (16)$$

Equation 16 is important in terms of optimized selection of C_S, C_F and A_{OL} in such a way that it affect integrator leakage minimally. This also forms a part of specification extraction for the OPAMP required during design procedure.

Fig.3 is the block level representation of discrete time model of a delayed integrator with gain(β) and leakage (with factor α) taken into account. Until this point the integrator is modeled efficiently using TDF MoC deploying a delay module and a module modeling scaling of input signal only.

B. OPAMP Gain-Bandwidth

In the Fig.3, scaling factor β responsible for introducing the integrator gain has the continuous time behavior of the OPAMP employed with the SC-integrator. Equation 12 forms the basis of this section, allowing to calculate the closed-loop bandwidth of the OPAMP when the open-loop gain, open-loop bandwidth and the closed-loop gain ($\beta = C_S/C_F$) are known. The implementation has been easily done by replacing the TDF scale module by a LSF continuous time transfer function with β as gain and F_{CL} as $3dB$ frequency. Parametric specification of A_{OL},F_{OL}, C_S and C_F allows flexible extraction of the OPAMP gain-bandwidth specification for the desired $\Sigma\Delta$ modulator performance.

C. OPAMP Slew Rate

The method to employ continuous time transfer function in above section is efficient only to describe small signal behavior of the OPAMP. However this completely fails to explain large signal behavior associated with the OPAMP.

Large signal behavior mainly involves the slew rate limitation and saturation of the OPAMP.

Slew rate limits the rate of output signal to change faster than a specified value allowing the designer to estimate the output currents required for the OPAMP stages. The typical definition of slew rate is the maximum allowed time rate of change of output voltage of the OPAMP and is described as follows

$$SR = max(|\ \frac{dV_{out}}{dt}\ |) \tag{17}$$

Equation 17 can be easily implemented using TDF Moc which has an access to the current simulation time.

State-of-Art methods involving using Matlab/SIMULINK requires definition of a complicated equation involving OPAMP gain-bandwidth and slew rate, whereas in case of this novel proposal, the equations can be easily distinguished for gain-bandwidth and slew rate separately.

D. OPAMP Saturation

In the Fig.2, the output of the integrator can have a value only intermediate to the supply voltage and ground voltage. In case if the output value reaches either of these, the negative input of the OPAMP no more remains tied to virtual ground and is free to attain some value which is not it's virtual ground. This leads to incomplete transfer of the input signal to the output [4]. This effect is referred to as saturation effect and must not occur for given input swing of a $\Sigma\Delta$ modulator. Architectural scaling is required under this condition. It is there fore very important to incorporate the effect of saturation in integrator model. The TDF block implements saturation by simply checking the input signal value and by saturating it with upper saturation value or lower saturation value when necessary.

E. OPAMP Noise

OPAMP in Fig.2 is a source of thermal and flicker($1/f$) noise. Also output of OPAMP contributes dc offset which can be described as input referred offset to the same OPAMP. Cancellation of flicker noise and input referred offset can be done using chopping of input and considered as out-of-scope of this article. The thermal noise due to an OPAMP is also considered as input referred noise and can only be efficiently extracted by circuit simulation methods. In this article, simulation of OPAMP circuit is out of scope and for simplicity we consider rms value of input referred thermal noise V_n is white in nature and can be modeled as a product of a noise amplitude with an uniform random distribution.

Fig.4 represents the "Real Integrator" with all above mentioned behavior.

VI. Results

Simulation has been carried on a single-bit second order $\Sigma\Delta$ modulator with above mentioned blocks. The capacitors were chosen as $C_S^{(1)} = 0.0625pF$, $C_F^{(1)} = 1.0pF$, $C_S^{(2)} = 0.25pF$ and $C_F^{(2)} = 1.0pF$ over a sampling frequency of $8MHz$.

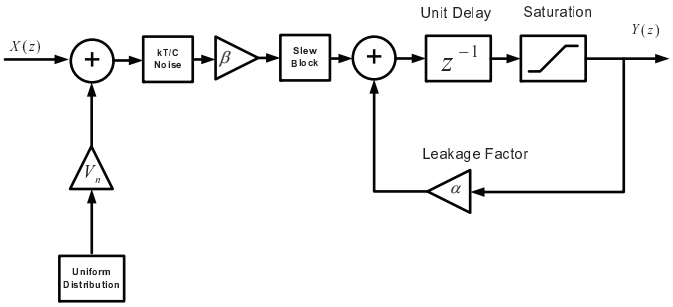

Fig. 4. Block Level Representation of Real Discrete Time Integrator

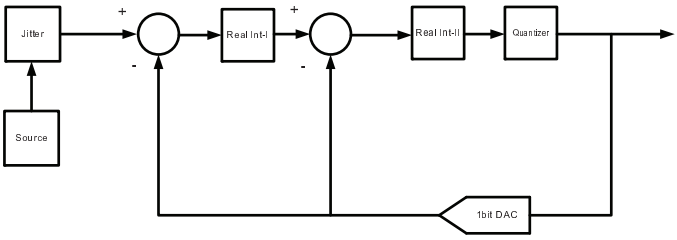

Fig. 5. Top Level Representation of Sigma Delta Modulator

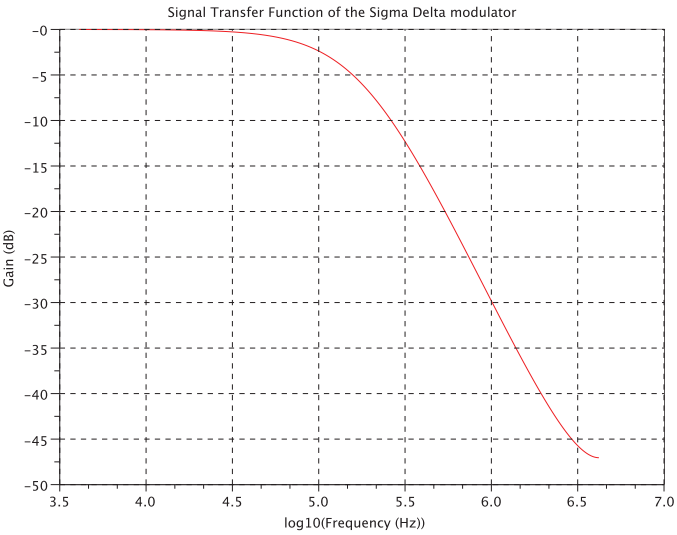

Fig. 6. Signal Transfer Function for Ideal $\Sigma\Delta$ Modulator

The Signal Transfer Function(STF), Noise Transfer Function(NTF) and FFT of the output of such a selection is shown in the Fig. 6, 7 and 8 respectively.

With the parameters defined in Table I, the output of the $\Sigma\Delta$ modulator is shown in Fig.9 showing the effect integrator leakage, effect of saturation and effect of slew rate limitation in case of an input sinusoid of frequency $50Hz$ and amplitude $530mV$. The available SFDR is 92.9 dB. This is to mention that the simulation only takes 188.0 $seconds$ including FFT computation.

Fig.10 is the SFDR characterization plot for the $\Sigma\Delta$ modulator. Until -20dB of input swing, the output varies linearly with input. When the input swing is more than -20dB, the slew

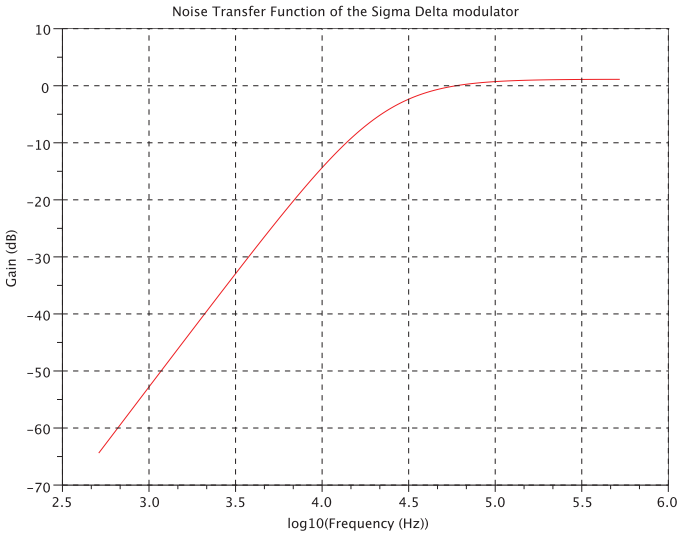

Fig. 7. Noise Transfer Function for Ideal ΣΔ Modulator

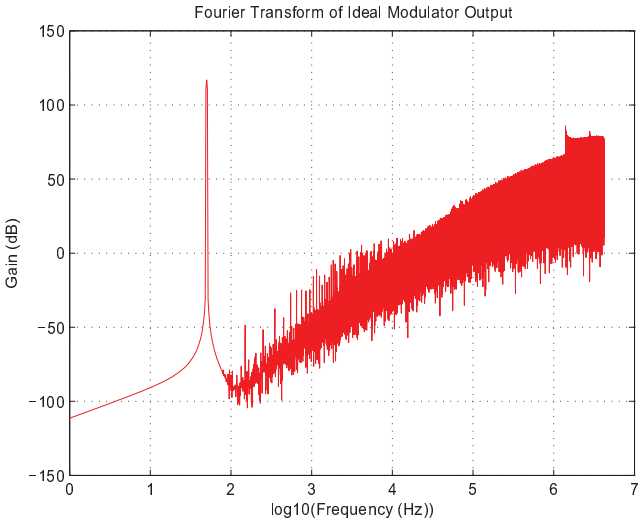

Fig. 8. FFT of the Output of the Ideal ΣΔ Modulator

TABLE I
SELECTED PARAMETERS

Sampling Frequency	$8MHz$
Vsupplyp	$3.3Volts$
Vsupplyn	$0Volts$
Reference Voltage	$1.2Volts$
Jitter Constant	$25.0pS$
Temperature	$273Kelvin$
OPAMP UGB	$100MHz$
OPAMP Slew Rate	$20Volts/\mu s$
OPAMP Input Referred Noise	$1.0nV$

rate limitation comes into picture and a part of increasing input swing goes off to compensate the slewing of the signal. This happens until -10dB, after that the slew rate limitation starts dominating and SFDR reduces. About the full swing of the

TABLE II
ANALYSIS DETAILS

Number of FFT Points	8388608
Window Type	Hanning

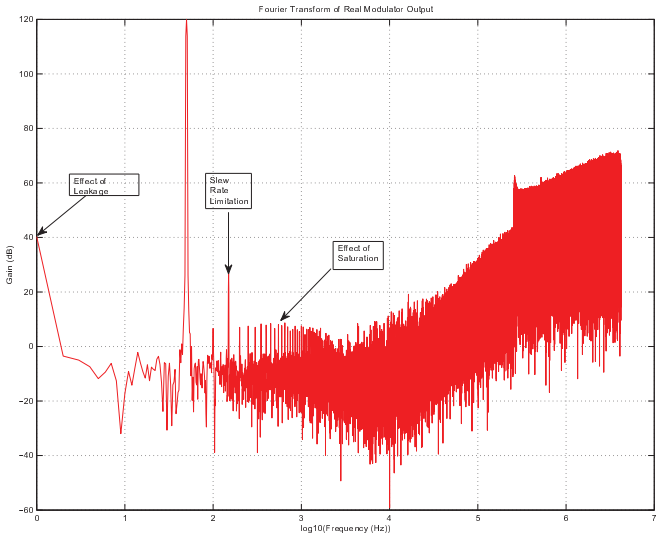

Fig. 9. FFT of the Output of the Real ΣΔ Modulator

TABLE III
EFFECT OF NON-IDEALITIES

Sampling Jitter	SNR
k_BT/C_S Noise	SNR
Switch Nonlinearity	SNR and SFDR
Integrator Leakage	Offset at Zero Frequency
OPAMP Gain-Bandwidth	SFDR
OPAMP Slew Rate	SFDR
OPAMP Noise	SNR
OPAMP Saturation	SFDR

input signal the saturation start taking place, and as a result the graph shows a steep reduction in SFDR.

Simulation also reveals effect of individual non-ideal parameters on the performance of ΣΔ modulator which has been summarized in Table III.

VII. CONCLUSION

In this paper, a set of SystemC AMS modules has been presented each of which represents respective non-idealities like sampling jitter, k_BT/C_S noise, switch non-linearity, integrator leakage, OPAMP gain-bandwidth, OPAMP slew rate, OPAMP noise and OPAMP saturation. Finally a time domain simulation result of a SC ΣΔ modulator with above mentioned sub-modules has been presented along with its optimized system parameters. This helps in accurate estimation of ΣΔ modulator SFDR, development of adaptive algorithm to correct the non-idealities associated with real life modulator in early phase and provision of a ultra fast simulation subsystem to the software developer. Future work from authors

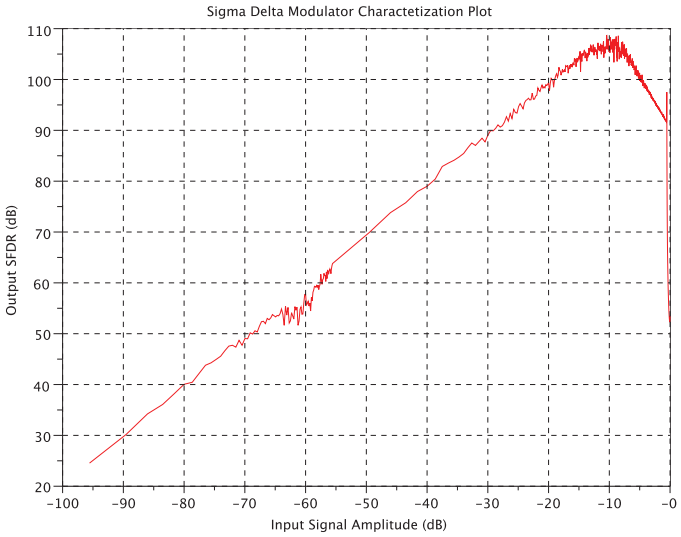

Fig. 10. SFDR Characterization Graph $\Sigma\Delta$ Modulator

will include non-idealities like band gap noise, DAC non-idealities and quantizer non-idealities.

Modeled Blocks are now a part of TUV SystemC-AMS building block library and can be downloaded through http://www.systemc-ams.org/

Although SystemC AMS extensions have been found to be useful in development and simulating these models, we missed features in SystemC AMS 1.0 standard which will be extremely useful in SW/HW interaction in mixed signal domain. Following are the points we want to mention as missing features:

1) TDF MoC:
   a) There is no possibility of events in TDF MoC. As a result the clock jitter has been implemented as a work-around. This could have been easily possible with the definition of an abstract clock which is missing
   b) There is no definition of a clock in TDF Moc, which means there is no possibility of changing clock frequency or disabling the clock. This again points towards a requirement of an abstract clock in TDF domain.
2) LSF MoC: LSF MoC would have been the best way to model continuous-time functionality. However, practically it can only be used inside encapsulated TDF MoC as LSF MoC does not provide non-ideal functionality with it. Using LSF CT function several time inside the model in this way raises a question about the conservation of notion of time. We therefore propose following set of feature addition in LSF domain,
   a) Capability of saturating the signal
   b) Slew rate filter block addition
   c) Transition filter block addition
   d) Analog event detection
   e) Addition of primitives which generates noise
3) In this article a SC $\Sigma\Delta$ modulator has been modeled using a simple SC integrator where the behavior of non-linearity is well understood. Modeling of non-idealities in case of complicated SC structures are difficult and error prone because of limited human imagination capabilities. We therefore propose a $High\ Level\ Non\text{-}Linear\ Solver$ in conservative domain consisting of pre-defined primitives like switches,OPAMPs,capacitors,resistors etc.(all with their respective non-idealities), within the native simulation environment, which enables design space exploration,feasibility analysis, specification extraction and software development in a more accurate and efficient way
4) We felt need of pole zero analysis capability while developing the discrete-time topology for the modulator and hence propose pole-zero analysis capability as a part of SystemC-AMS
5) System level $Monte\text{-}Carlo$ analysis capability allows proper selection of Capacitors, OPAMP Gain and Bandwidth.We propose $Monte\text{-}Carlo$ analysis capability as a part of SystemC-AMS extensions
6) Random numbers used in this work has been taken from GSL library [6]. The reliability of random numbers used in a simulation is always an important issue and hence we propose inclusion of a set of random number generators with SystemC-AMS library
7) The FFT calculations has been done using GSL library [6]. We propose inclusion of a set of analysis tools like FFT,PSD, Eye Diagram etc along with SystemC-AMS.

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