Solar Inverter with Active Current Ripple Compensation

K. H. Edelmoser, Institute of Electrical Drives and Machines, Technical University Vienna,
Gusshausstr. 27-29, A-1040 Wien, AUSTRIA, kedel@pop.tuwien.ac.at
F. A. Himmelstoss, Technikum Wien, University of Applied Science, Hoechstaedtplatz 5,
A-1200 Wien, AUSTRIA, himmelstoss@technikum-wien.at

Abstract

In the field of electrical solar power conversion EMC is of topical importance. In common single-phase inverter applications the current of the solar array shows a pronounced ripple. This entails two significant disadvantages: Reduced over-all efficiency due to dynamic maximum power point mismatch and reduced lifetime of the panels due to additional component stress. Furthermore, the output of the solar inverter also shows significant distortions in it's voltage and current shape. The proposed approach discussed in this paper uses a combined structure of an active filter to fulfil the given requirements: Minimized input current ripple of the cells, string-optimised maximum power point tracking and optimal power quality of the supplying grid.

1. Introduction

Based on state-of-the-art switching mode solar converter arrangements for string operation, here a solution with active input ripple minimization and optional active mains current filtering (harmonics minimization) is proposed (c.f. Fig. 1).

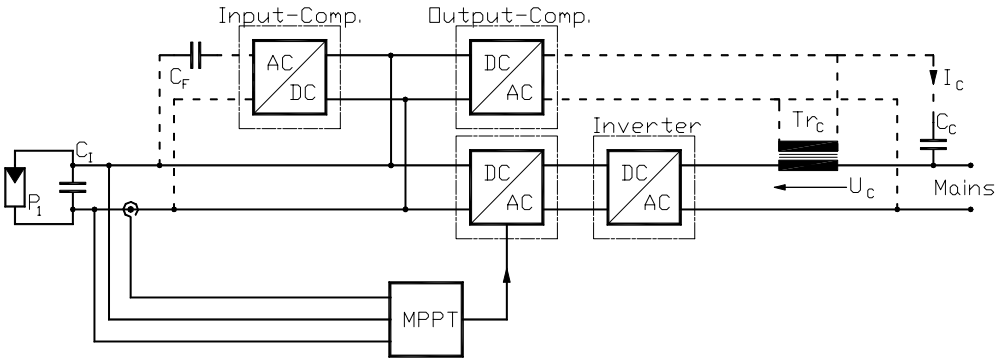

Fig. 1. Innovative solar inverter array with active ripple compensation and filtered power-line interface (series or parallel line interfacing by Tr_C or C_C, optionally)

The starting point of our investigations was a solar inverter with a DC-to-DC converter for voltage level adaptation similar as depicted in Fig. 1. The converter was enhanced by two compensators: An input- and an output compensator where added to minimize the influence on each side of the converter. On the input side the mains current ripple can be eliminated and with the second inverter the mains current harmonics can be minimized [1,2].
In Fig. 2 the energy flow in the system is depicted for detailed analysis. As one can see both compensators require operation power from the generator: P_{IL} are the losses of he input compensator and P_{OL} come from the output compensator, if both are controlled in such a way that the average of the power pulsation is equal to zero. The second energy direction of each compensator clarifies the energy recuperation feasibility, which can be used to minimize the energy storage requirements in each compensator cell (C_{IS} and C_{OS}, respectively).

ISBN 978-3-8007-3431-3

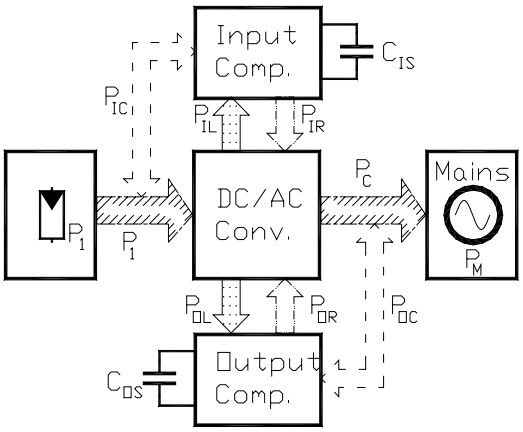

Fig. 2. Energy flow in a full compensated solar inverter arrangement

The requirements to eliminate the low frequency ripple from the solar cells differ from the goal of minimizing the mains current ripple and harmonics. In the first case a rather huge storage capacitor or a virtual weak DC-link is necessary, while in the second case the higher dynamics of the DC-to-AC inverter require only a smaller capacitor. An approach for mains current ripple minimization on input side is depicted in Fig. 3. In this solution the voltage sources U_1=U_4 and U_2=U_3 represent divided DC-link capacitors. They are controlled in such a way that the PV-compensator can be operated at only a partial voltage of the DC-link. So the switching losses can be reduced.

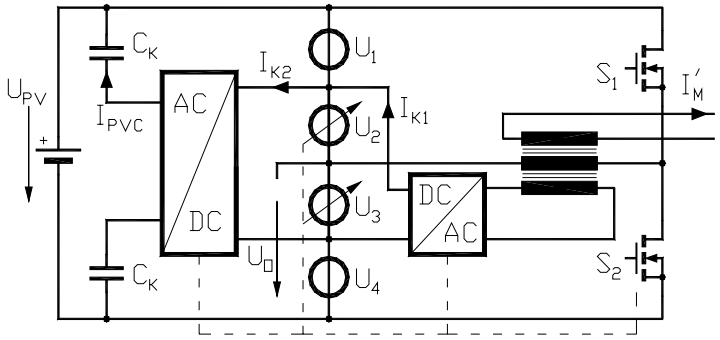

Fig. 3. Innovative solar inverter array with active input ripple compensation and dynamic power storage in divided DC-link capacitors

Figure 4 shows a possible solution for mains ripple compensation. Here also only a partial voltage of the DC-link is used to feed the compensator.

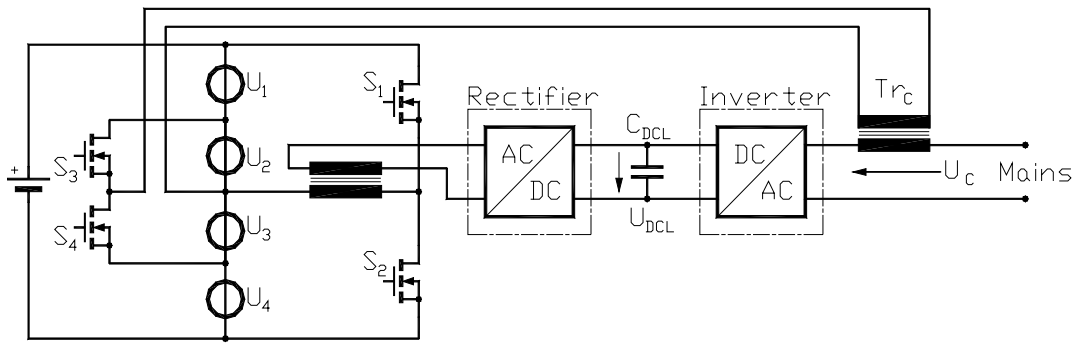

Fig. 4. Innovative solar inverter array with active mains current ripple compensation

In both cases (Fig. 3 and Fig. 4) the voltage U_0 represents the fixed, symmetric DC-link center point, while the capacitive voltage dividers represented by C_1 / C_2 and C_3 / C_4 (c.f. Fig. 5) in conjunction with the compensators are controlled dynamically depending on the point of load.

The big advantage of this topology is that the compensator operates at a reduced supply voltage, which is controlled dynamically during the mains period, and a significantly increased switching frequency leading to minimized losses. The compensator injects a DC-free current into the load and therefore only the losses of the auxiliary converter have to be covered by the supply. This is realized by an extension of the main inverter.

2. The Basic Problem

The principle of our system is the dynamic control of the capacitive voltage divider with respect to the energy storage. As one can see in Fig. 5, a controlled current injected at $I_{PV,C+}$ and $I_{PV,C-}$ respectively can be used to control the voltages U_{C2} and U_{C3} and therefore different energy levels can be stored in our system.

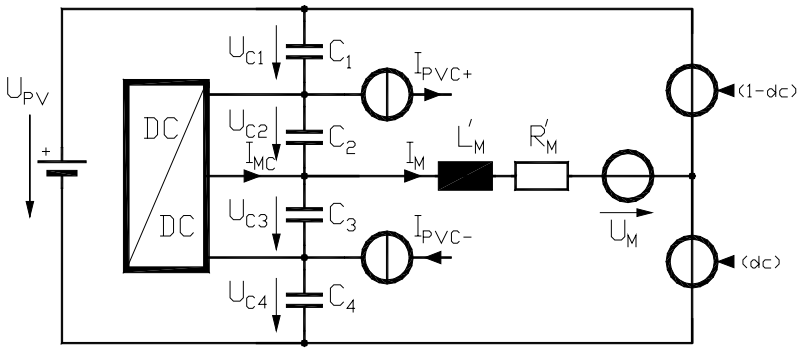

Fig. 5. Active energy recuperation of the compensator power in case of mains compensation

The energy stored in a capacitor is described by $W_C = C \cdot \frac{U^2}{2}$.

In conjunction with the requirements that

$U_{DCL} = U_{C1} + U_{C2} + U_{C3} + U_{C4}$ and $\overline{U_{C1} + U_{C2}} = \overline{U_{C3} + U_{C4}}$

we can use this system to diversify the energy stored for compensation purpose with reduced influence to the total energy maintained.

For example, it can be assumed that the compensator is operated at 10% of the DC-link voltage and an operation voltage band of another 10% is allowed. Without external control one can assume that $C_1 = C_4 = C$ and $C_2 = C_3 = 4 \cdot C$.

This leads to an effective capacitor of $C_{EFF} = 5 \cdot C$ for the compensator.

From the point of view of the DC-link, the total energy storage capacitor remains unchanged, according $C_{DCL} = \frac{C}{3}$.

In Fig. 6 one can see the basic problem of the conventional system on the input side. The dynamic MPPT mismatch leads to reduced over-all efficiency and generator lifetime. Due to the varying array-current, a respectively large averaging energy buffer (C_{IN}) is needed to smoothen the solar array's current. A standard gauge of approximately 5000µF / kW-peak at 200V solar voltage range is a good starting point to keep the voltage ripple within the recommended 2% of the MPP-voltage [3,4].

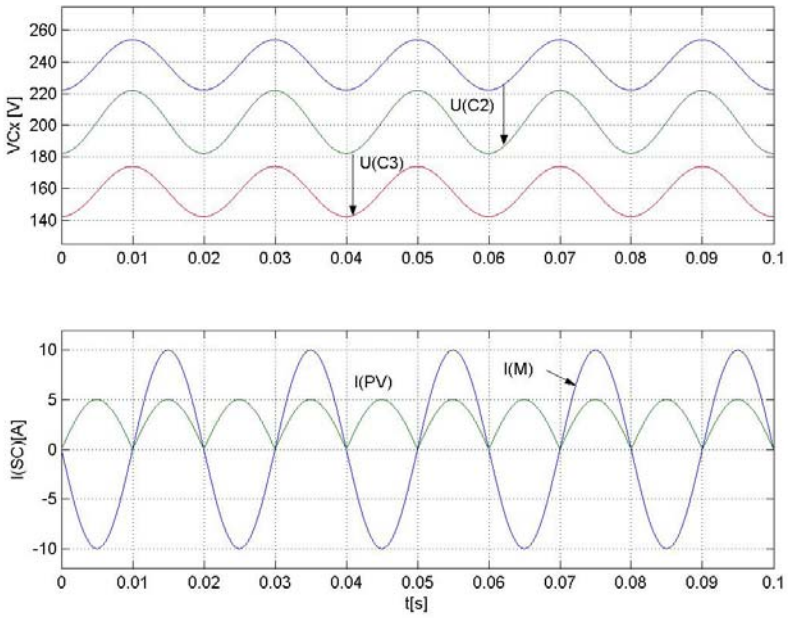

Fig. 6. System behavior in solar array side without compensator and input filter capacitor usage: The upper picture shows the capacitive voltage divider, while the input current shape I_{PV} and the load current I_M are shown below (green line: U_0)

3. The Compensator Approach

Based on the system given in Fig. 5, an energy path between the voltage dividers (C_1/C_2 respectively C_3/C_4) and the input of the converter (c.f. P_{IC} in Fig. 2) was established. This path is used to smoothen the input current ripple of the converter. Figure 7 shows the schematic of the compensator stage and the converter for DC-link voltage adaptation. The operation principle is based on the insertion of a controlled phase offset of 90deg between the mains current and the input current ripple by the compensator (c.f. Fig. 8).

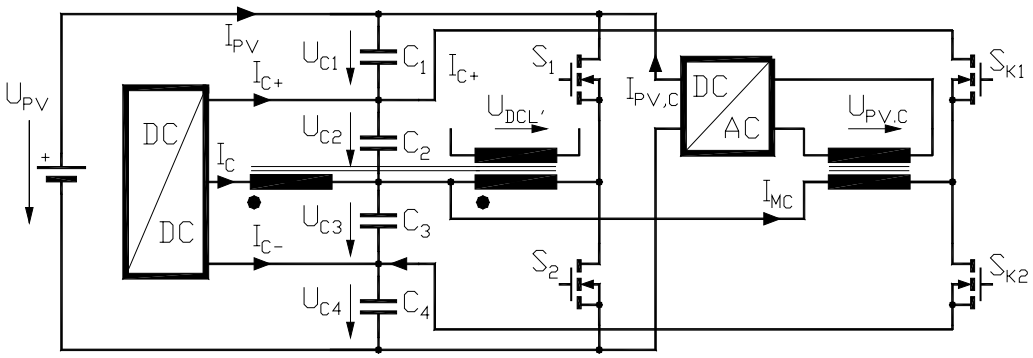

Fig. 7. Input current ripple compensation, dynamic current sharing

The advantage of this topology is the simplified system structure of the filter which can use the energy storage capacitors of the DC-to-DC converter built by S_1 and S_2. Due to the approach of a DC-free compensation current injection $P_{PV,C}$, the auxiliary DC-to-DC converter is only necessary for feeding I_{C+} and I_{C-} to provide the losses of the compensators (S_{K1}, S_{K2}).

3.1. The Supply of the Compensator

For a high efficiency compensator the losses can be covered by the DC-link capacitor balancing network. Another approach is a balancing system based on a rectifier coupled to the inverter stage.

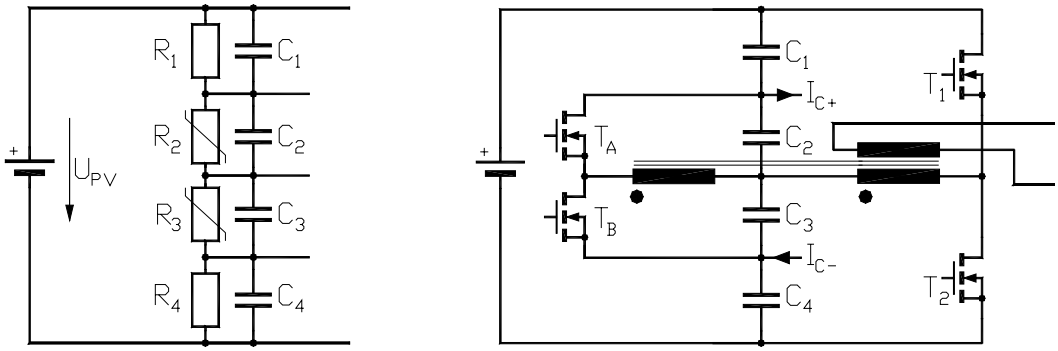

Fig. 8. Balancing solutions: a: resistive and b: transformer coupled with active control

To increase the system efficiency an active voltage balancing can be achieved. A possible solution was given in Fig. 8.b.

4. System Simulation

To clarify the advantages of the proposed topology, the simplified filter structure for both filters, the low-frequency input-ripple buffer was simulated in detail.

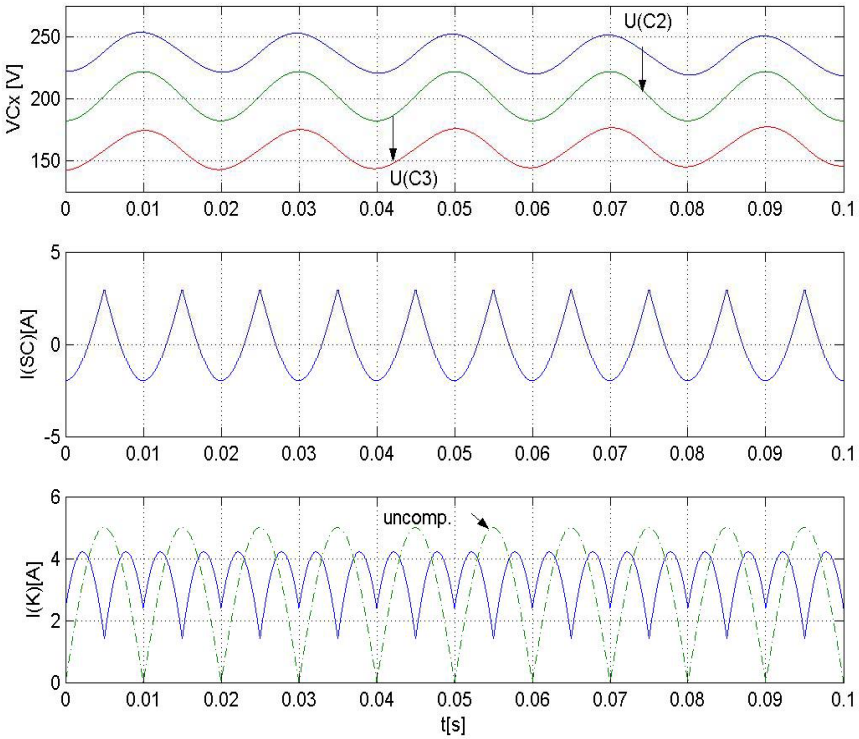

Fig. 9. System behavior on solar side without compensator usage: The upper graph shows the capacitive voltage divider, while the input current I_{PV} and the load current I_M are shown below

In Fig. 10 a 2kW system was simulated to clarify the compensator operation. From top to bottom one can see the operation of the capacitive voltage divider, the current injected by the compensator fed from the DC-link and the compensated input current (blue line). Contrary to the original input current (dashed green line) the ripple current here is reduced by more than 40%.

As a result the source is loaded with a significantly reduced current ripple which easily can be filtered by a small storage capacitor. The compensator helps to hit the maximum power point without any significant dynamic distortions. Furthermore, the input capacitor can be decreased, because a common energy storage element is used operating at higher voltage with higher efficiency. Here under several circumstances also batteries can be used giving the possibility of building a redundant UPS-system.

The power stage of the used filter consists of a simple half bridge arrangement feeding the ripple current. The converter is operated at several 1kHz and 10kHz, respectively, leading to a tolerable low output current ripple.

The effective usage of multi-phase input cells coupled with an active filter shows us the capability to reach the goal of high efficiency, reduced current harmonics and improved EMC.

5. Conclusion

The proposed approach discussed in this paper uses a combined structure of an active filter to fulfill the given requirements: Minimized output current ripple of the cells, string-optimized maximum power point tracking and optimal power quality for the supplying grid. The topology presented in this paper shows a remarkable improvement of the over-all efficiency as well as a significantly enhanced EMC. Consequently, it is well suited for solar power inverter applications. As a result, the source is only loaded with a perfect DC-current, which helps to hit the maximum power point without any dynamic distortions. Here, the input capacitor can be decreased, because a common energy storage element is used operating at higher voltages with higher efficiency. On the other side the current ripple generated by the mains inverter can be kept under control and held below the limits. The proposed topology can be used as an alternative to multi-stage converters with a constant DC-link voltage and an active switching DC-to-AC inverter [3]. The topology presented in this paper is a simple and effective solution for small to medium power grid coupled applications. The concept is well suited for wind-, solar- and renewable energy as well as for aerospace applications.

6. Literature

[1] Veerachary, M.; Senjyu, T.; Uezato, K.: “Maximum power point tracking control of IDB converter supplied PV system”, Proceedings of the IEE Electric Power Applications 2001, Vol.: 148 , Issue: 6, pp.: 494 - 502

[2] Duran, E.; Galan, J.; Sidrach-de-Cardona, M.; Segura, F.: “An application of interleaved DC-DC converters to obtain I-V characteristic curves of photovoltaic modules”, Proceedings of the 34th IEEE Annual Conference of Industrial Electronics, IECON 2008, pp.: 2284 - 2289

[3] K. H. Edelmoser, F. A. Himmelstoss: "A Simple, Efficient, and EMI-Optimized Solar Array Inverter, WSEAS Transactions on Circuits and Systems, Issue 9, Vol. 9, Sept. 2010, pp.597-606, ISSN: 1109-2734.

[4] K. H. Edelmoser, H. Ertl, F. C. Zach: "A Multi-Cell Switch-Mode Power-Supply Concept Featuring Inherent Input Voltage Balancing", Proceedings of the 10th WSEAS International Conference on Circuits, Systems, Communications and Computers CSCC '06, July 10.-15. 2006, Athens, Greece, CD-ROM, ISBN:960-8457-47-5, 534-373.pdf.

Acknowledgement

The authors are very much indebted to the 'Fonds zur Förderung der wissenschaftlichen Forschung' which supports the work of the Power Electronics Section at the University of Technology Vienna (Project number L 531-N14).