Measurement of harmonic distortions and impedance of HF RFID chips

Nikola Gvozdenovic, Lukas W. Mayer, and Christoph F. Mecklenbräuker
Christian Doppler Laboratory for wireless technologies for sustainable mobility, Institute of Telecommunications, Vienna University of Technology, Vienna, Austria
Email: nikola.gvozdenovic@tuwien.ac.at

***Abstract*—In this contribution, we focus on the characterization of the nonlinearity of an HF RFID (high-frequency radio frequency identification) chip. We discuss and analyze recent measurements of the chip impedance: the HF RFID chip's response at the fundamental frequency as well as at several harmonics. The HF RFID chip's behavior is presented both versus input power and frequency (at the discrete frequencies of the harmonics). The chip impedance is extracted from the measured S_{21} parameter, and a simple equivalent model of integrate circuit is applied.**

***Index Terms*—HF RFID, chip impedance measurement, harmonic distortion**

I. Introduction

Contact-less chip cards, defined in [1] are used in a variety of applications, like for identification or for credit cards. Notable implementation of these cards is in electronic ticketing systems, biometric passports, for identification as HF RFID (high-frequency radio frequency identification), in smart phones as NFC (near-field communication), etc.

Frequency of operation is 13.56 MHz and the information is transmitted through magnetic coupling. Typically, a card consists of an integrated circuit (IC) and an antenna. As antenna a planar spiral inductor (coil) is used. Additionally, a capacitor can be used for tuning. For designing a card, a good model of both the coil and the chip is essential.

Antenna design of the rectangular spiral coils used in HF RFID is analyzed in depth in [2] [3], using PEEC (partial element equivalent circuit) EM model. In our recent paper [4] we analyze and measure circular spiral coils.

Impedance of UHF RFID (ultra high frequency RFID) chips is measured and analyzed by Nikitin et al. in [5] and [6]. Chip measurement and analysis of HF RFID chips, on the other hand, is presented in [7]. In both contributions chip impedance is found from S_{11} measurement using the reflection method.

In our contribution we extract the chip's impedance from an S_{21} measurement. Additionally, we also measure signals that are generated by the chip at harmonic frequencies.

This paper is organized as follows: in Sec. II we discuss our approach for measuring the impedance at the fundamental frequency and the harmonic signals produced by the chip. Here we propose our measurement method and show a simple equivalent model of the chip. In Sec. III we describe our measurement setup and measurement procedure. Results of the chip's impedance are given in Sec. IV. Before we conclude, measurement results of the harmonic distortions are presented in Sec. V.

II. Measurement approach

The goal of our measurement is to characterize the nonlinear behavior of the chip in a measurement setup that provides a defined load situation at all frequencies. The reason for this is that voltage and current of the chip in its intended application are strongly influenced by the impedance that is presented to the chip at fundamental and harmonic frequencies. Also, the load situation in this case is influenced by detuning of the coil which is caused by materials in its proximity. The load situation of a chip in its intended application is generally unknown which makes interpretation of the results difficult. On the other hand, measuring voltage and current directly at the chip introduces errors due to imperfections of the probes used.

The circuit of our measurement setup is shown in Fig. 1. It is obvious that at the fundamental frequency the chip is powered by a source with an equivalent source impedance of $100\,\Omega$. Furthermore, the chip is terminated at all harmonic frequencies with a load of $100\,\Omega$ as well. This setup can be easily reproduced in simulation, and measured and simulated results can be compared.

As an example, from our measured results we extract Lissajous curves, that are commonly used in chip-design. The current and voltage are obtained by solving the measurement circuit shown in Fig. 1 according to the following expressions:

$$\underline{U} = \underline{U}_s - 2\underline{U}_2 \tag{1}$$

$$\underline{I} = \frac{\underline{U}_2}{Z_0}. \tag{2}$$

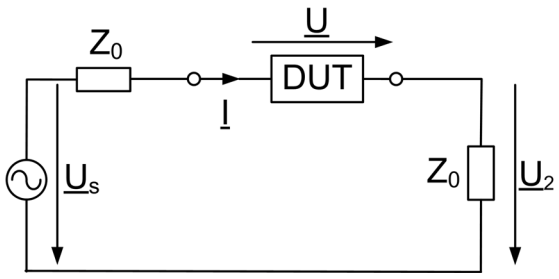

Fig. 1: Proposed measurement approach.

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We analyze the chip's response at harmonic frequencies ($2f_0, 3f_0$ etc.) as a function of the available power at the fundamental frequency of $f_0 = 13.56\,\text{MHz}$.

An equivalent circuit model commonly used for HF RFID chips [8][9] is shown in Fig. 2. Elements of this model are:

- input capacitor C_{In} for tuning the antenna,
- full-wave rectifier (consisting of diodes like in Fig. 2 or of transistors),
- shunt voltage regulator for stabilizing the internal DC voltage,
- capacitor C_{TP} for storing the DC charge, and
- resistor R_L as the load of the digital circuitry.

We use this model for checking our measurement results for plausibility.

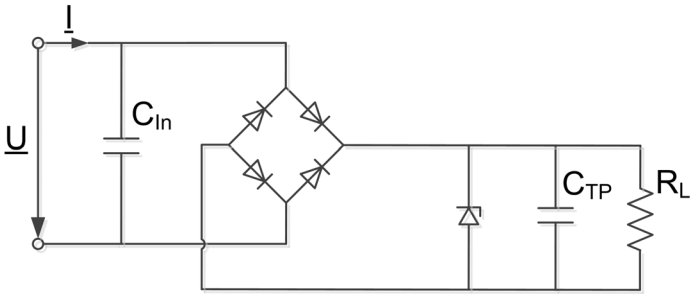


Fig. 2: Non-linear integrated circuit model [8].

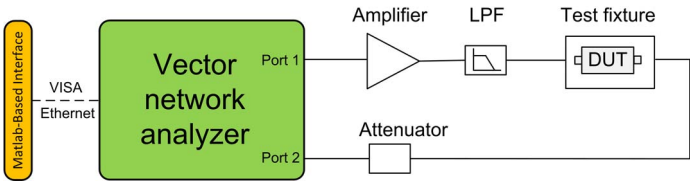
III. Measurement Setup

To measure the input impedance at the fundamental, we use a VNA (vector network analyzer). There are two principal methods to characterize impedances with a VNA [10]. The reflection method uses one port and the impedance is calculated from the wave quantities—typically S_{11}. Since the transponder chip is expected to have very high impedances values (kΩ) the reflection method is prone to error, mainly caused by imperfect calibration. Measurement accuracy can be improved by the shunt or series method which uses two ports of the VNA. These methods benefit from a higher dynamic range and less noise of the VNA when measuring transmission coefficients (S_{21}) between two ports. For high impedances the series setup (Fig. 3a) gives the best results. Impedance is calculated from the S_{21} measurement at the fundamental. The generated harmonics are related to the incoming wave at port 2 of the VNA (b_2).

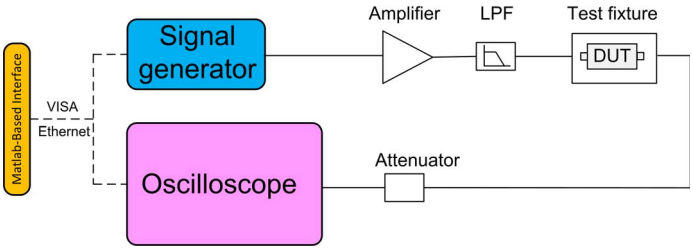
During the measurement port 1 of the VNA generates a signal at the fundamental frequency at specified power levels. This signal is fed through an amplifier to achieve power levels of up to 0.5 W. The internal source of the VNA and the power amplifier introduces their own harmonic distortions that would corrupt the measurement of the harmonic power levels produced by the DUT. A specially designed low-pass filter was used that

- suppresses all harmonics from the VNA and power amplifier, and
- provides an impedance of 50 Ω for all harmonic signals that come from the DUT.

This is vital to maintain the validity of the measurement circuit in Fig. 1 for harmonic frequencies. We use a ZVA8 VNA by Rohde&Schwarz and utilize Matlab to control the measurement and evaluate measurement data.



(a) Setup 1.

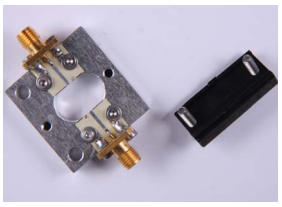


(b) Setup 2.

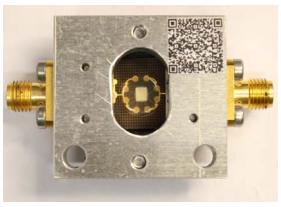
Fig. 3: Two measurement setups.

For most accurate calibration of this measurement a custom test fixture was designed (Fig. 4). 50 Ω microstrip transmission lines extend to the connection points of the chip at which the antenna will be mounted. Parasitic capacitance to ground was minimized by removing metal structures from the vicinity of the chip. A custom made calibration kit allows to shift the measurement reference planes to the ends of the microstrip lines. An overview of the measurement setup with the VNA is shown in Fig. 3a.

In a second measurement setup, the VNA is replaced by a signal generator that produces the same power levels at the fundamental, and an oscilloscope that samples $\underline{U}_2$ in the time domain. From these results, the cross-frequency phase relations between the fundamental and the harmonics are determined.



(a) Disassembled fixture.



(b) Fixture's downside.

Fig. 4: A photo of the test fixture.

IV. Chip Input Impedance Measurement on the Fundamental Frequency

To find the chip impedance, first we measure the S_{21}-parameter at the fundamental frequency versus power. We calculate the chip's fundamental impedance according to:

$$Z_{\text{chip}} = \frac{2Z_0(1 - S_{21})}{S_{21}}. \quad (3)$$

In Fig. 5 we show real and imaginary part of the chip impedance vs source power in a range from -5 to 27 dBm. We observe that the chip starts to exhibit nonlinear behavior for power levels above 2 dBm. At this point the diodes of the rectifier in Fig. 2 start to conduct.

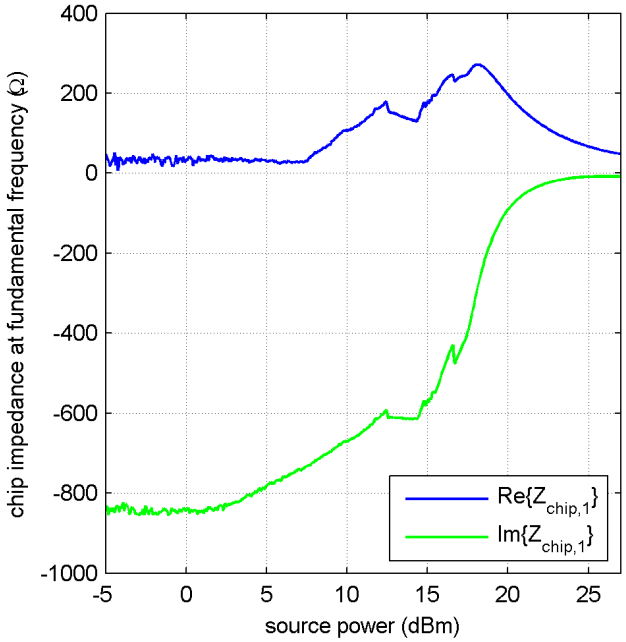


Fig. 5: Real and imaginary part of the impedance (from S_{21}).

In Fig. 6 we show the equivalent parallel resistance and capacitance of the chip, where $R_p = 1/\text{Re}\{1/\text{Z}_{\text{chip}}\}$ and $C_p = \text{Im}\{1/\text{Z}_{\text{chip}}\}/\omega_0$. We observe that the resistance and the capacitance have approximately constant values until an available power level of 7 dBm (20 kΩ in parallel to 15 pF). In this region the chip can be considered as a lossy capacitor with linear behavior. The chip is not operable in this range. Please note that the available power level of our measurement setup is not directly related to the minimum operating power of the chip. For power levels higher than 7 dBm the rectifier starts conducting and the equivalent parallel resistance drops. With increasing power, strong nonlinear behavior is observed.

V. Chip Harmonic Distortion Measurement

In this section we investigate the harmonic signals generated by the chip as a function of available input power. For the model and the extraction of Lissajous curves, the amplitude and phase of the harmonic signals with respect to the fundamental signal has to be known. The two measurement setups (Fig. 3) are used to achieve high accuracy of the results. We measure the amplitude of the harmonics with the VNA which gives high accuracy due to cross-frequency power calibration. The second measurement setup that uses an oscilloscope measures the signal $\underline{U}_2$ in the time domain.

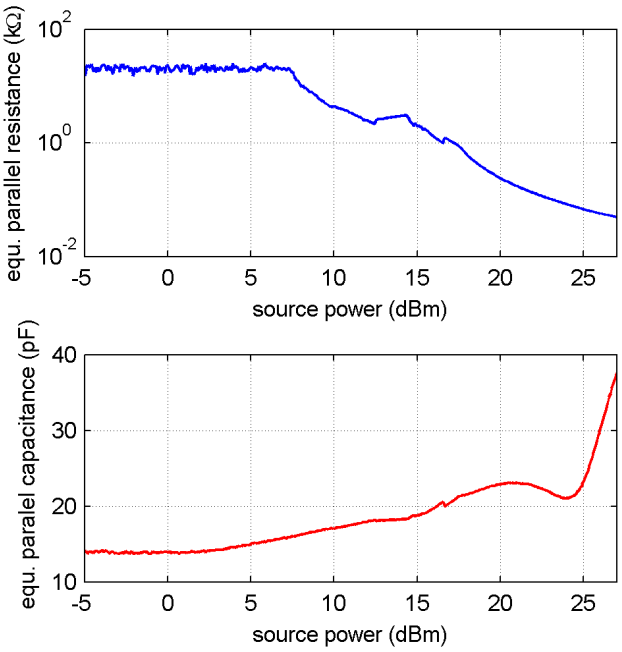


Fig. 6: Resistance and capacitance of the equivalent R_p and C_p calculated from S_{21}.

From the time domain measurement the cross-frequency phase of the harmonics can be determined by Fourier transformation. In the spectrum of the signal we find the precise phases of the harmonics with respect to each other. To relate the phases of $\underline{U}_2$ with the phase of the source voltage $\underline{U}_s$, the result from the VNA measurement at the fundamental frequency (S_{21}) is used. This is possible because we performed a phase calibration with the VNA at the fundamental frequency using a through standard instead of the chip.

In Fig. 7 we show the magnitudes of the chip voltage $\underline{U}$ measured at the fundamental and the first 9 harmonics versus input power level calculated from $\underline{U}_2$. For reference, also the amplitude of $\underline{U}_s$ is shown. The limiting behavior of the internal shunt mechanism can be seen as a limiting of the fundamental chip voltage. We can furthermore observe that odd numbered harmonics are stronger than even numbered. This is a typical behavior of rectifiers. Furthermore, we conclude that harmonic signal levels can be quite high (e.g. the signal at $3f_0$ can be only 18 dB below the fundamental) which causes spurious emissions. In combination with coils that behave as antennas at higher frequencies, the eavesdropping distance is larger than in [11].

In Fig. 8 we show the phases of the chip voltage $\underline{U}$ at the fundamental and the harmonics versus input power level measured in the time domain and calibrated by the S_{21} measurement in the frequency domain. It is seen that the phases shown stronger variation with higher harmonic number.

In Fig. 9 and 10 exemplary Lissajous curves of current $\underline{I}$ and voltage $\underline{U}$ are depicted.

In Fig. 9 we show the Lissajous curves for available power levels below 16 dBm. For very low input power the Lissajous curve has the shape of an ellipse. This is consistent with the

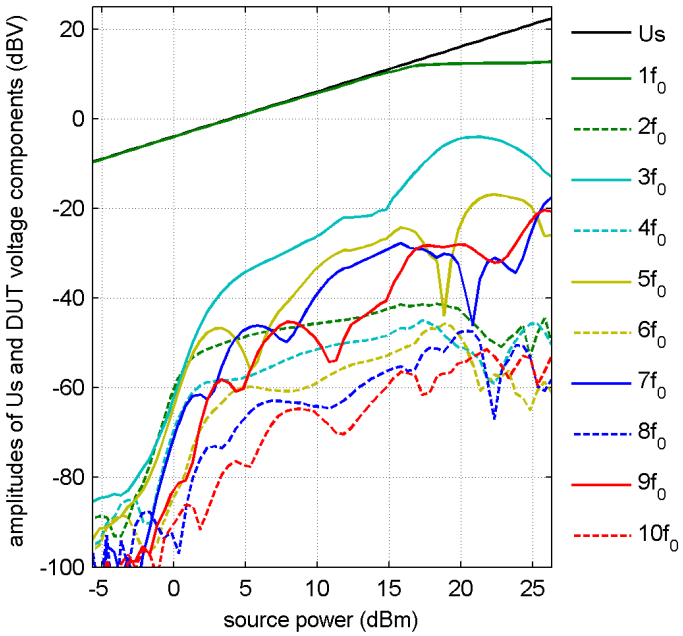


Fig. 7: Amplitude of U_s and DUT voltage components on the harmonic frequencies.

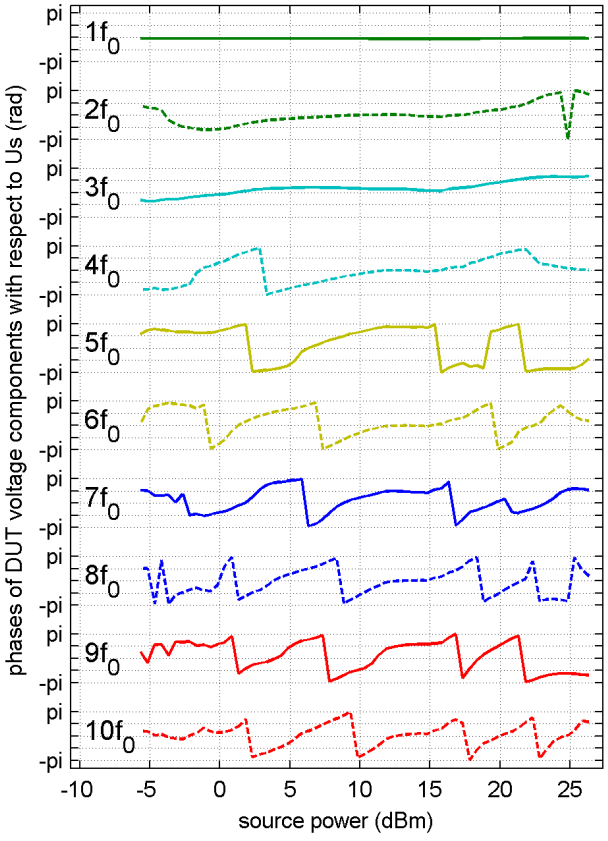


Fig. 8: Phases of DUT voltage components on the harmonic frequencies with respect to U_s.

chip resembling a lossy capacitor. With increasing available power the ellipses start to change their shape which is because of nonlinear effects in the rectifier.

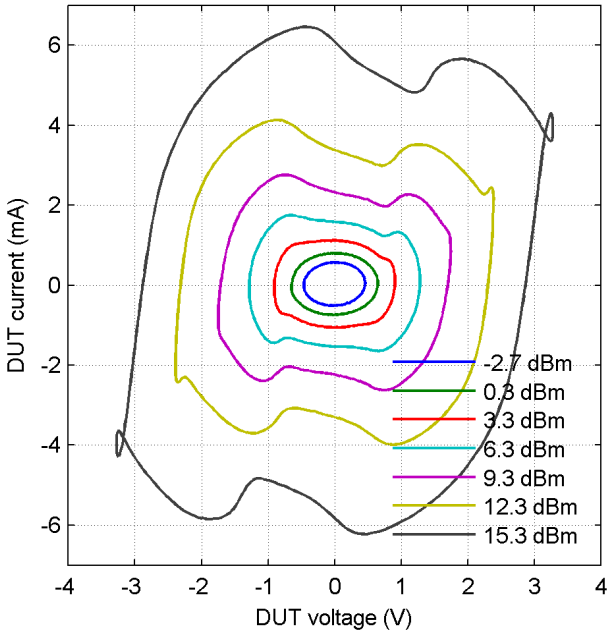


Fig. 9: Lissajous curves for low input power range.

In Fig. 10 the Lissajous curves for available power levels above 17 dBm are shown. It is obvious, that the rectifier and the internal voltage regulator limit the input voltage of the chip. Even at available power levels as high as 0.5 W the chip voltage never increases beyond 4.2 V. With an assumed forward voltage of 0.6 V, an internal limiting of the supply voltage to a maximum level of 3 V is probable. In this region the chip is fully active and we can see that the diodes in the rectifier are switched on. Chip currents up to 90 mA have been observed at maximum power.

VI. Conclusions

In this paper, we proposed a measurement method that allows reproducible measurements of nonlinear behavior of HF RFID chips. The chip is characterized by measurements for a wide range of input power levels and up to the 30th harmonic. Results are presented as amplitudes and phases of fundamental and harmonic signal components at the chip's port. The chip behavior is consistent with a typical equivalent model. Limiting behavior of the internal shunt mechanism of the chip has been clearly observed in obtained Lissajous curves. The load modulation by the chip's frontend has been disregarded, but will be included in future work.

VII. Acknowledgements

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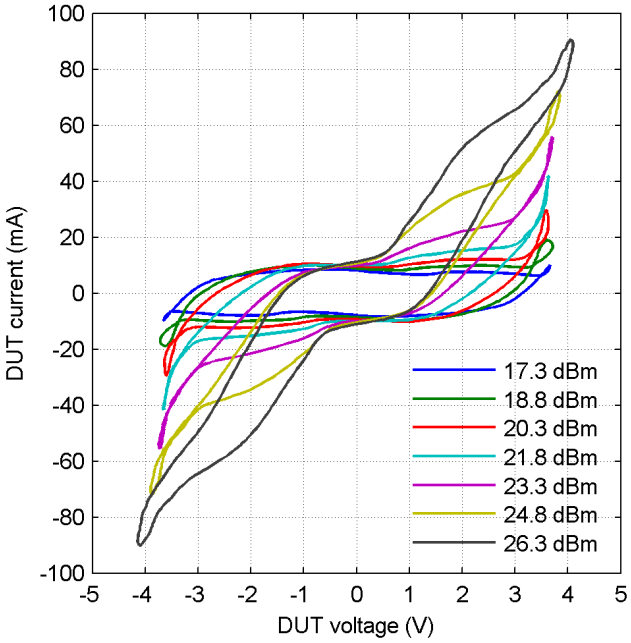

Fig. 10: Lissajous curves for high input power levels.

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