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17 GHz Receiver in TSLP Package for WLAN/ISM Applications in 0.13 µm CMOS

Christoph Kienmayer(1), Mario Engl (1,4), Andreas Desch(1,2),
Ronald Thüringer(1,2), Mohit Berry(1,3), Marc Tiebout(1), Arpad L. Scholtz(2) and R. Weigel(4)

(1) Infineon Technologies AG, Otto-Hahn-Ring 6, 81730 Munich, Germany.
(2) Technical University of Vienna, Gusshausstrasse 25/389, 1040 Vienna, Austria.
(3) University of Ulm, Albert-Einstein-Allee, 89069 Ulm, Germany.
(4) University of Erlangen-Nuremberg, Cauerstr. 9, 91058 Erlangen, Germany.
christoph.kienmayer@infineon.com, mario.engl@infineon.com

Abstract:

This work presents a fully integrated CMOS receiver in a leadless plastic package (TSLP) for high data rate WLAN applications at 17.2 GHz ISM band. The receiver offers a gain of 35 dB, input 1dB compression point of -49.6 dBm, SSB noise figure of 9.9 dB and an input IP3 of -39.8 dBm. At a power supply of 1.5 V, the receiver, which includes LNA, complex demodulator, VCO, IQ-divider and all RF-buffers, consumes only 245 mW.

1. Introduction

Wireless local area networks (WLAN) systems are increasingly used in offices, hotels and public places to provide high-speed wireless access for portable computers and other mobile devices. Wireless LANs are relatively cheap, easy to install and require no license for network operation. Current systems mostly use the 2.4 GHz or 5 GHz frequency bands, where propagation conditions yield large cells and hence allow considerable area coverage with only a few Access Points. If wireless traffic grows and network becomes congested, either the cell size must be reduced or an overlay network at another frequency band has to be deployed so that the increased capacity demand can be met.
In this work the second alternative is considered. A fully integrated 17 GHz CMOS receiver has been implemented and the performance was tested. In addition to provide larger bandwidth, operation at the 17 GHz band is also intended to be used as a backbone for 2.4 GHz or 5 GHz access points over a distance up to 100 m. Furthermore, the 17 GHz link can be used as a short range high data rate wireless link.
Especially at higher frequencies, the electrical performance of packages plays an important role. The chip is fully packaged using Infineons low-cost TSLP (Thin Small Leadless Package) [1]. Figure 1 shows the footprint of the employed package. The dimensions of the package are 3.5 mm x 3.5 mm. Au-wirebonds are used as first level interconnects. The wirebonds have a length of approximately 400 µm and a diameter of 25 µm. The parasitic effects of the wirebonds were taken into account during the chip design, thus the wirebonds act as an additional external matching network. The inductivity of the utilized wirebonds is approximately 400 pH. Similar package concepts can be found in [2] and [3].

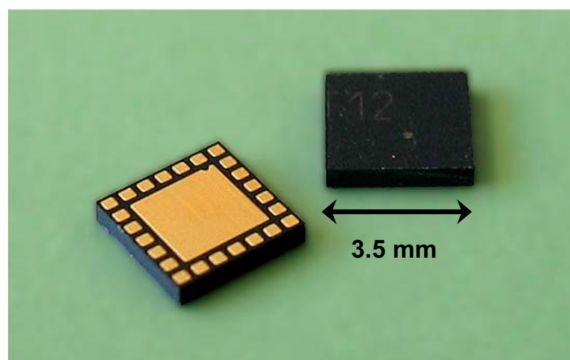

Figure 1: Footprint of the package.

2. System Architecture

In this paper, a fully integrated CMOS receiver in TSLP is presented. The chip is fully functional and features sufficient gain and linearity to enable complex modulation schemes for WLAN communications.

2.1 Package

A detailed overview of the package assembly process is shown in Figure 2. The package is based on a copper leadframe with contacts. These contacts are made of nickel with a thin gold layer for soldering purposes on top. The typical contact height is 50 µm with further potential for reduction. The chip is directly attached with its backside to a relatively large contact area. After this Die-attach step, the chip pads are wirebonded to the remaining Ni contacts on the leadframe. The entire structure is molded and the copper leadframe is completely etched away after the molding process. Next the remaining Ni-pads are plated with electroless NiAu. The individual packages are separated and electrically tested in the final step. Flip Chip as first level interconnects are supported by the package as well.

When using Flip Chip, the die is attached upside down via AuSn bumps to the Ni contacts on the leadframe.

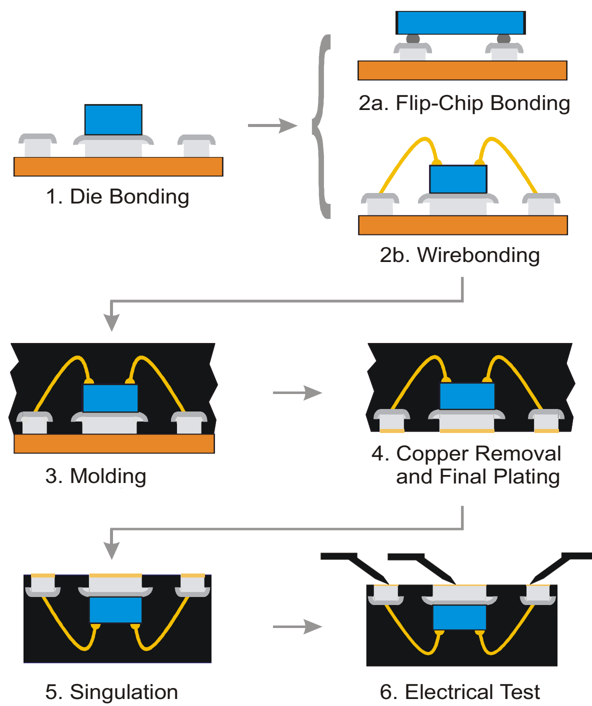

Figure 2: Assembly process.

Since the chip is directly attached to the Ni contacts, exceptional heat transfer characteristics are achieved. This makes the package an excellent candidate for power applications and applications in harsh environments e.g. "under the hood" electronics like automotive radar. The standard package height is 0.4 mm and can further be reduced. The size of the Ni contacts is 300 µm x 300 µm. These small dimensions and the contact height of 50 µm deliver very good high frequency performance especially when flip chip is used.

The package is soldered on an evaluation board. A polished cut image of the TSLP and board is shown in Figure 3.

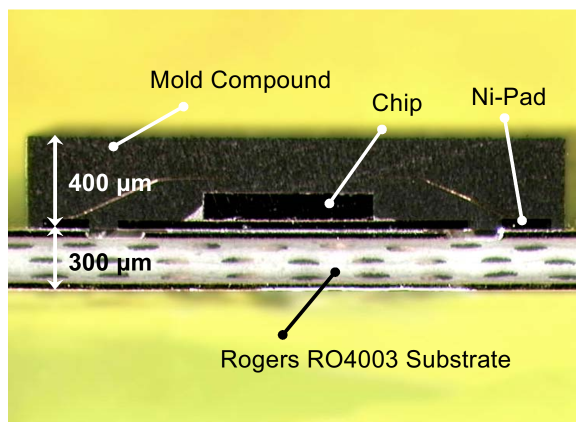

Figure 3: Polished cut image.

2.2 Receiver Architecture

A double conversion or quasi-homodyne receiver architecture [6, 7] with a division factor of four between the oscillator frequency and intermediate frequency was implemented. The dual-conversion receiver architecture avoids off-chip IF filtering by using a high IF.

Figure 4 shows the block diagram of the CMOS receiver which consists of LNA, a dual conversion stage with an intermediate frequency amplifier, VCO, a 4:1 divider and a baseband output driver. Additionally, buffers for the LO frequencies and a second 2:1 divider is implemented to provide an output for an external PLL.

In our work, the choice of 3.44 GHz IF provides 6.88 GHz frequency separation between the incoming RF signal and its image. Further, the narrow band on-chip LC filters used in the RF and IF gain stages provide a suppression of the 10.32 GHz image, avoiding the usage of an explicit off-chip IF image reject filter. The entire receiver is designed to provide sufficient gain and linearity to enable complex modulation schemes for WLAN communications. Open standardization issues [4] were replaced with the specifications for commercial 54 Mbit/s WLAN at 5.7 GHz [5] and verified with Agilent ADS system simulator.

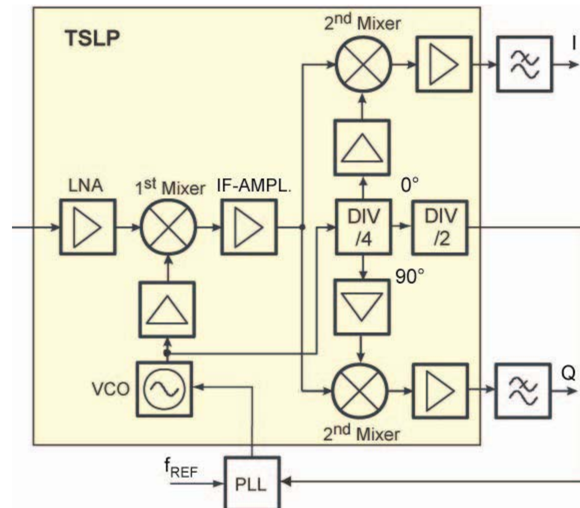

Figure 4: Block diagram of the proposed receiver.

2.2.1 Circuit Implementation

The fully differential LNA core with on-chip inductive degeneration shown in Figure 5 consists of a cascoded, inductively degenerated common source input stage that converts the available power into current. The integrated series inductors at the input improve the matching in a robust way compared to external matching or bond wire matching. The LNA-output is loaded by an integrated LC-tank, resonating at 17.2GHz in order to improve the gain.

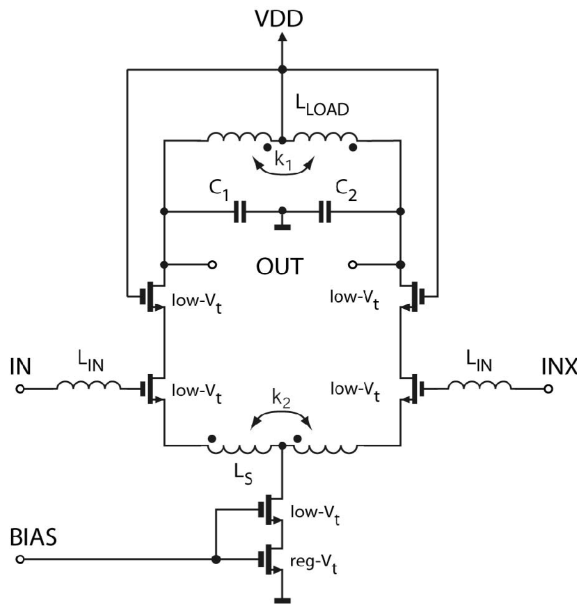

Figure 5: Schematic of the LNA.

Figure 6 shows the schematic of the 1st mixer, which downconverts the output of the LNA to an intermediate frequency of around 3.44GHz.

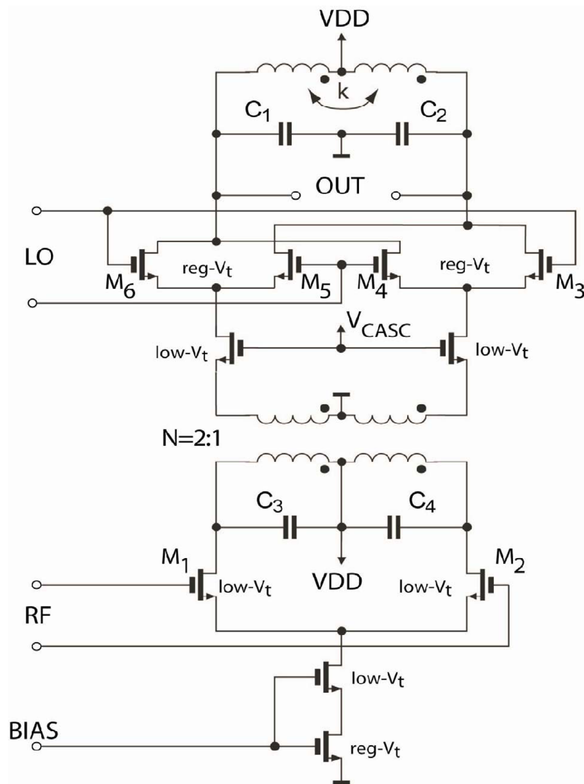

Figure 6: Simplified schematic of the first mixer.

A classical Gilbert type mixer was preferred in combination with a fully differential integrated transformer. Such a topology effectively doubles the voltage headroom available for the circuit design and enables the insertion of cascode transistors to improve the linearity and to control the current in the mixer switching stage [8]. NMOS capacitors are connected to the primary winding to achieve highest coupling between the two transformer stages.

The mixer output is loaded by an integrated LC-tank at 3.44GHz to enhance the gain and provide a second order bandpass filtering. The receiver uses the VCO and IQ-divider from the PLL design of [9].

The VCO, re-centered to the desired frequency of 13.76 GHz, features a tuning range of 4% at current consumption of 6.2 mA with phase noise performance of -105 dBc/Hz at 1 MHz offset. The output signal of the VCO is fed to the buffer of the 1st mixer as well as to the 4:1 divider, which is implemented by a static current mode logic (CML) divider circuit [9]. The 4:1 divider, which consists of two master-slave flip-flops, produces I/Q signals for the 2nd mixer stage. At the cost of extra power consumption, it was necessary to implement an interstage buffer to obtain a higher voltage swing at the mixer inputs. The divider circuit and the buffers clearly dominate the total power consumption of the receiver.

The 2nd mixer core consists of a simple differential transistor pair as input, classical Gilbert type mixer for the LO signal and the load is realized by poly-resistors. Between the dual mixing structure, a two stage IF amplifier is located. The buffers used for the LO signals have a similar topology as the IF amplifier.

2.3 Measurement Results

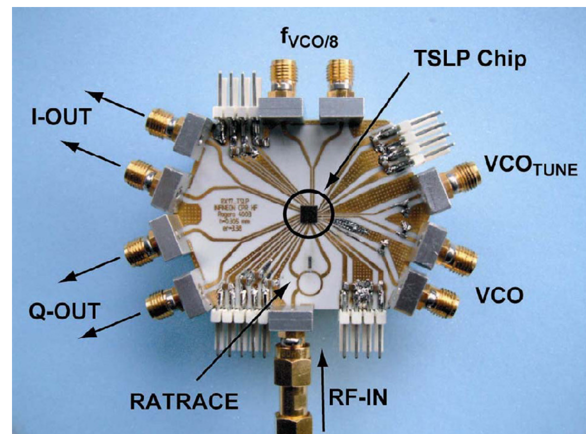

Figure 7: Evaluation board with TSLP chip.

To perform measurements, the package containing the chip was soldered on an evaluation board. Figure 7 shows a photograph of the evaluation board. At the RF input a ratrace coupler generates the differential input signals. To measure the receiver testchip, the integrated VCO is locked by an external PLL with a reference signal $f_{REF} = f_{VCO}/8$ as shown in Figure 4. This external loop could be easily replaced by the PLL of [9].

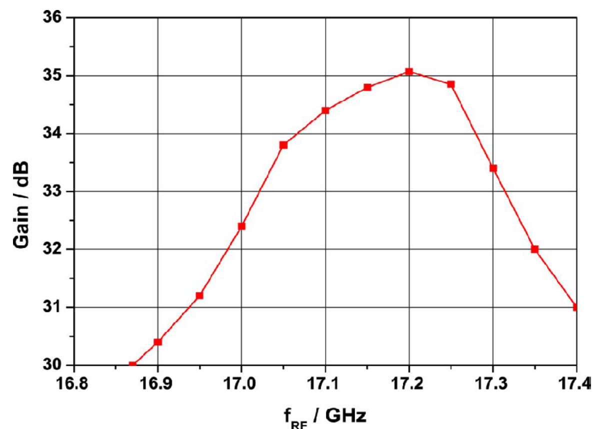

Figure 8: Gain over frequency.

Figure 8 depicts the measured gain as a function of the input RF frequency, with a fixed baseband frequency of 100 MHz. The maximum gain of the 0.13 µm CMOS receiver is perfectly centered at 17.2 GHz ISM/WLAN band. Figure 9 shows the measured compression and two tone intermodulation results with two tones 1 MHz apart. Measurements were performed using a 50 GHz Agilent E4448A spectrum analyzer with noise figure option along with a preamplifier. Typical measured performance, including the SMA-connectors and on board microstrips is summarized in Table 1.

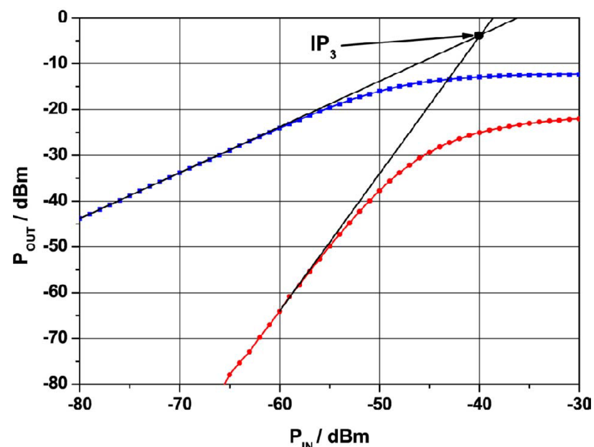

Figure 9: Measured receiver two tone test.

Supply Voltage RX	1.5V
Supply Voltage VCO	1 V
3 dB RF bandwidth	17 – 17.35 GHz
Gain	35 dB
RX Noise Figure (SSB)	9.9 dB
RX Input-CP @ 17.2 GHz	-49.6 dBm
RX Input IP3 @ 17.2 GHz	-39.8 dBm
Phase Noise @ 1 MHz offset	-105 dBc/Hz
LO1 leakage to RF	-53.6 dBm
LO2 leakage to RF	-72.5 dBm
Total Power Consumption RX	245 mW
Die Area	1.2 mm²
Technology	Standard 0.13 µm CMOS, 6 Cu-metals

Table 1: Receiver performance summary.

The chip size is 1 mm x 1.2 mm, which is clearly dominated by the pads, inductors and on-chip power supply decoupling.

3. Conclusions

This work presents a fully integrated high gain CMOS receiver in a leadless plastic package (TSLP) for high data rate WLAN applications at 17.2 GHz ISM band is presented. The receiver offers a gain of 35 dB, input 1dB compression point of -49.6 dBm, SSB noise figure of 9.9 dB and an input IP3 of -39.8 dBm. At a power supply of 1.5 V, the receiver, which includes LNA, complex demodulator, VCO, IQ-divider and all RF-buffers, consumes only 245 mW. The main improvements in the state-of-the-art include high level integrity as well as low power consumption operating at a radio frequency of 17 GHz.

References:

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