17 GHz Transceiver Design in 0.13 μm CMOS

M. Tiebout[2], C. Kienmayer[2], R. Thüringer[1,2], C. Sandner[2], H.D. Wohlmuth[2], M. Berry[2], A.L. Scholtz[1]

[1] Technical University of Vienna

[2] INFINEON Technologies AG, Corporate Research

Otto-Hahn-Ring 6

Munich, Germany, Europe

Email: marc.tiebout@infineon.com

Invited Paper

Abstract

This paper presents the research work towards a fully integrated 17 GHz transceiver in 0.13 μm standard CMOS. The simultaneous challenge of high-integration, highest frequency and low-voltage design is solved combining optimized on-chip passives and RF circuit techniques with a double-conversion sliding RF-architecture. Three measured chips clearly demonstrate the feasibility of a CMOS transceiver at highest frequency. A fully integrated $\Delta - \Sigma$ 13 GHz PLL consumes 60 mW from 1.5 V supply. The complete RF RX-path features a gain of 37dB, IIP3 of -37dBm and a SSB NF of 9.3 dB, consuming 180.8mW from 1.5 V supply. A first TX path testchip includes the second modulator and linear output driver. Consuming 93mW from 1.5 V supply, it features a gain of 4dB and an OIP3 of 13dBm.

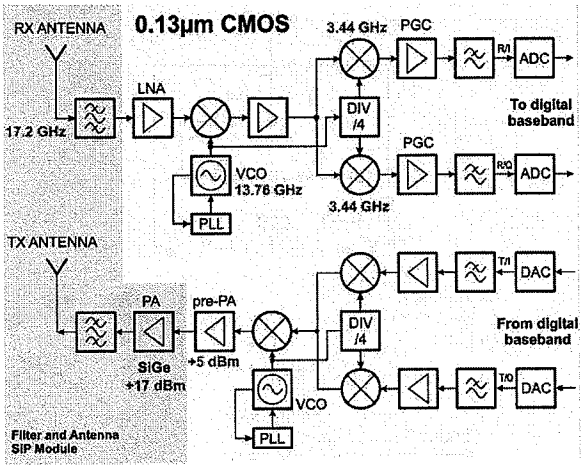

Fig. 1. Transceiver architecture

Introduction

As the frequency bands for wireless data communication below 10 GHz get more and more crowded, attention trivially goes towards higher frequency band, especially to the ISM bands at 17 GHz and 24 GHz. Due to the ever increasing high frequency capabilties of sub-micron CMOS and to possibility to exploit its huge digital processing power, CMOS is also attractive for these high frequencies offering a cheap, highly integrated SOC. The purpose of this work is to develop a completely integrated CMOS transceiver for WLAN operation at the 17.1-17.3 GHz industrial, scientific and medical (ISM) band [1], offering data rates up to 155 Mbit/s.

For the transceiver architecture, a double conversion sliding RF receiver and transmitter structure was chosen as presented in Fig. 1. This concept was proposed in [2] and is very advantageous for the integration of this highest frequency project:

- In comparison to a ZERO-IF architecture, the LO-generation is shifted downwards from 17.2 GHz to 4/5 or 13.8GHz of the input frequency. Main advantage is that the generation of I/Q signals at 17.2 GHz is completely avoided, and shifted to a frequency of 3.6 GHz.
- The LNA amplifier is loaded by one mixer instead of an IQ-mixer pair, strongly reducing the capacitive load to the LNA
- The first demodulator can be optimized for highest speed, the second demodulator for flicker noise.
- The separation of input or output frequency and LO-signals avoids the unwanted coupling to the LO, and offers the possibility to integrate the power amplifier.
- The RF gain can be optimally divided over LNA, first and second demodulator.

The next sections describe recent results of this transceiver project, consisting of three testchips: completely integrated PLL, complete receiver path and the high frequency combination of modulator and output driver (or pre-PA).

Receiver

The complete receive chain is fully differential. The LNA and mixer together determine the performance of

the front-end. For instance, although a large LNA gain is desirable, too large gain may overload the mixer and compromise dynamic range. On the other hand, the gain must be large enough to overcome the fundamentally higher mixer noise. It is also preferable to connect the LNA in some simple way to the mixer input, without a high power consuming buffer circuit. A fully differential common-source type LNA with on-chip inductive degeneration is chosen. LNA-design is one of the main challenges in the front-end design, since this circuit determines the total noise figure of a receiver [3]. The LNA core in Fig. 2 consists of a cascoded, inductively degenerated common source input stage that converts the available power into a current. This topology allows reasonable input matching with a low noise figure at a low power consumption. The inductive degeneration is employed at the common

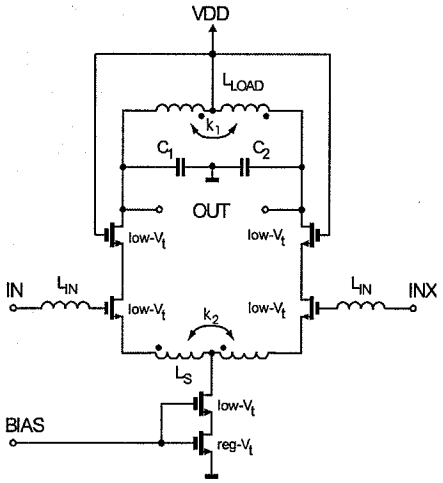

Fig. 2. Schematic of the LNA

source node of the LNA to achieve a real valued input impedance. The LNA-output is loaded by an integrated LC-tank to improve the gain. In order to get a high quality factor in the LC-tank it is necessary to minimize the total capacitance and maximize the inductance. Therefore the total capacitance seen by the inductor in the circuit is realized by the parasitic capacitance. Furthermore this tank provides a bandpass filter at 17.3 GHz. The integrated series inductors at the input of the LNA improve the input matching and the high-frequency gain in a more robust way compared to external or bond wire matchings. Due to the high frequency all inductors can nicely be integrated without significant area penalty (see chip photograph Fig. 4). The integrated series inductors at the input improves the matching in a robust way compared to external matching or bond wire matching. In order to improve the gain, the LNA-output is loaded by an integrated LC-tank, resonating at 17.2 GHz.

The amplified signal at the LNA output is downconverted to a intermediate frequency of 3.5 GHz for further amplification, filtering and detection. The downconversion mixer is an integral part of the RF front-end. In Fig.

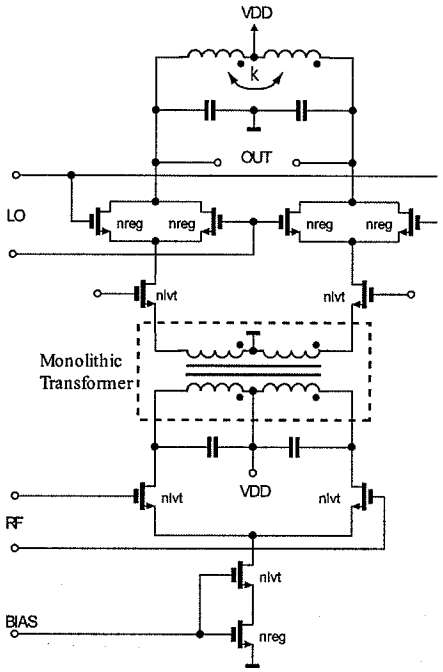

Fig. 3. Schematic of the first demodulator

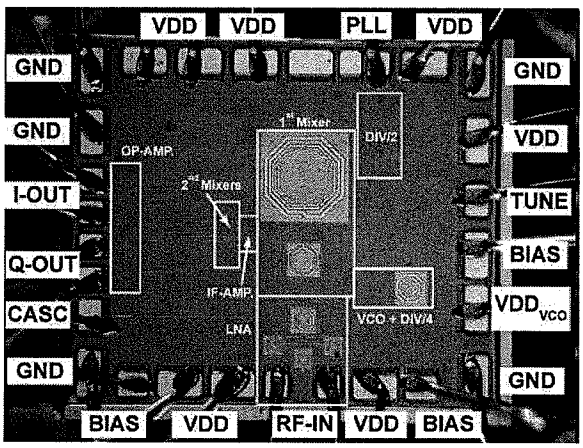

Fig. 4. RX chip photograph

3 the mixer schematic diagram is presented. The classical Gilbert type mixer [4] was preferred as the best solution to combine acceptable gain, noise figure and linearity. To overcome the problems caused by the low supply voltage of 1.5 V for the 0.13 μm CMOS process, a fully differential integrated transformer [5, 6] was inserted between the input transconductance stage and the switching pairs. Power supply is connected to the center taps of the transformer. This topology effectively doubles the voltage headroom available for the circuit design and enables the insertion of cascode transistors to improve the linearity and to control the current in the mixer switching stage. To achieve the highest coupling between the two stages

the transformer should work in resosance. This was realized by inserting two NMOS-capacitances connected to the primary winding. Due this capacitancies the transformer is tuned to the desired center frequency of 17.3 GHz. Further the mixer is loaded by an integrated LC-tank at 3.5 GHz to enhance the gain and to provide second order bandpass filtering. In order to achieve the maximal inductance the inductor is realized as cross-coupled fully differentail inductor which exploits the coupling factor to increase the inductance per chip area. The total capacitance seen by the the inductor in the circuit is realized with the inherent capacitance of the inductor (inner winding and to substrate) and the capacitance of the connected transistors (drain, gate). Also the parasitics of the interconnections must be considered, especially between two stages. This tank features a fully differential integrated 6.6 nH inductor.

An IF-amplifier with a gain of approximately 5 dB loads the first mixer, before the signal is fed to the second complex demodulator consisting of two standard gilbert mixer cells. The performance of the receiver is summarized in Table I.

TABLE I
Receiver performance summary.

Supply voltage RX	1.5 V
3 dB bandwidth	17.02 - 17.33 GHz
S_{11}	<-12 dB
Gain	37.5 dB
Noise figure (SSB)	9.4 dB
RX input 1dB-CP	-47.9 dBm
RX input IP_3	-37.4 dBm
Power consumption	188.4 mW
Die area	$1.2\,mm^2$
Technology	standard 0.13 μm CMOS

PLL

The fully integrated PLL design includes VCO, IQ-divider, prescaler, loop filter, phase frequency detector, charge pump and Δ-Σ Modulator. The IQ-divider is designed to drive the second demodulator stage directly, which explains it high power consumption. As this work aims at a single chip transceiver, special attention was invested to design the PLL as insensitive as possible to crosstalk and VCO-tuning, as well as loop filter, and charge pump use fully differential signals. The performance of the PLL is summarized in Table II, further details can be found in [7]. Reference frequency is 64 MHz.

Transceiver

The most critical part of the transmit path is the combination of the high frequency second modulator and output driver. For optimal performance these blocks have

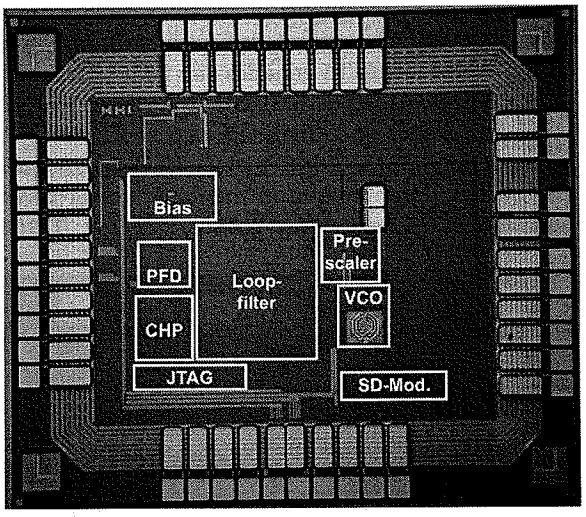

Fig. 5. PLL chip photograph

TABLE II
PLL performance summary.

Supply voltage	1.5 V
Locking range	12.6 - 13.1 GHz
Phase noise (IQ-output)	-100 dBc/Hz
@ 1 MHz offset	-100 dBc/Hz
Total power consumption	60 mW
VCO	8 mW
IQ-Divider	40 mW
Prescaler	1 mW
Loop filter	5 mW
Charge pump	3 mW
Biasing etc.	3 mW
Die area	$1.8\text{x}1.2\,mm^2$
Technology	standard 0.13 μm CMOS

to be co-designed. The required linearity for a target OFDM WLAN application, together with the high frequency of operation clearly dominate the design. The schematic of these blocks is presented in Fig. 6. The

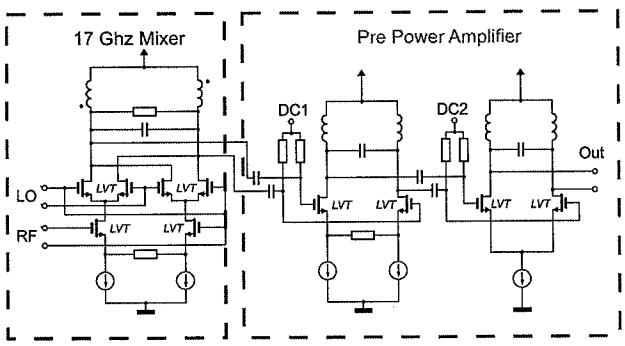

Fig. 6. Modulator+Driver schematic

mixer is a standard gilbert mixer cell loaded with an on-chip LC-tank. The output driver consists of two inductively loaded stages to enhance the gain. The inductors at the output-pads provide ESD-protection, as their low series inductance of 320 pH acts as a short circuit to the power supply for the low-frequency ESD-pulses (rise-time ca. 100 ns). More details on the linear power driver can be found in [8]. On the chip photograph (Fig. 7) the high

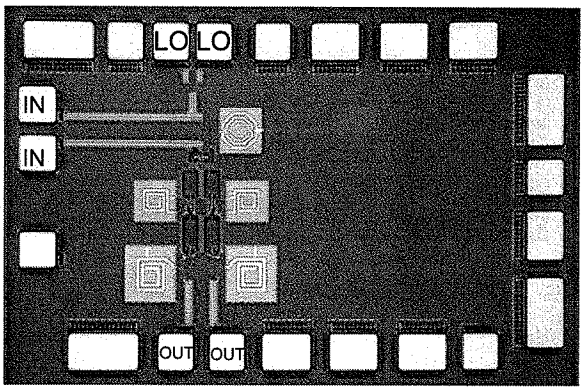

Fig. 7. Modulator+Driver chip photograph

number of coils is clearly visible. Chip area, however, is still very small due to the high frequency. Figure 8 shows

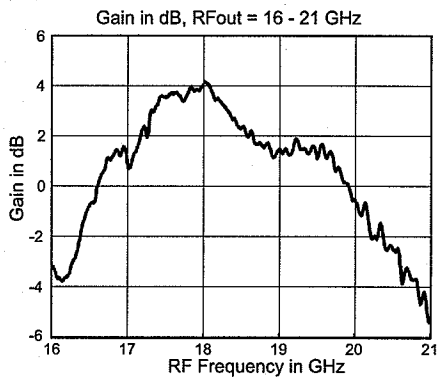

Fig. 8. Modulator+Driver measured gain

the frequency characteristic of the combination. Further measured results are summarized in Fig. III.

Conclusions

An overview of the research work towards a fully integrated 17 GHz transceiver in 0.13 μm standard CMOS was presented. Measured results for the complete PLL and receiver, as well as on the critical modulator path show a good performance at a power consumption comparable to chip-sets for WLAN at 2.4 or 5 GHz bands. These results were obtained through the combination of a double-conversion architecture with optimized circuits and optimal use of on-chip passive components.

TABLE III
Modulator+Driver performance summary.

supply voltage	1.5 V
3 dB bandwidth	16.6 - 19.6 GHz
gain	4 dB
output 1dB-CP	4.2 dBm
output IP_3	13 dBm
total power consumption	93 mW
modulator power consumption	18 mW
driver power consumption	75 mW
die area	0.5 mm^2
technology	standard 0.13 μm CMOS

References

[1] ETSI, "Hiperlink, http://www.etsi.org," .

[2] S. Tadjpour, E. Cijvat, E. Hegazi A. Abidi, "A 900 MHz Dual-Conversion Low-IF GSM Receiver in 0.35 μm CMOS," in *IEEE JSSC*, December 2001, pp. 1992–2002.

[3] C. Kienmayer, R. Thüringer, M. Tiebout, W. Simbürger, A.L. Scholtz, "An Integrated 17 GHz Front-End for ISM/WLAN Applications in 0.13 μm CMOS," in *IEEE Symposium on VLSI Circuits*, Juni 2004.

[4] B. Gilbert, "A precise four quadrant multiplier with subnanosecond response," *IEEE Journal Solid-State Circuits*, pp. 365–373, December 1968.

[5] D. Kehrer, W. Simburger, W, H.-D. Wohlmuth, A.L. Scholtz, "Modeling of Monolithic Lumped Planar Transformers up to 20 GHz," in *proceedings*. IEEE Custom Integrated Circuits Conference, May 2001, pp. 401–404.

[6] M. Tiebout, T. Liebermann, "A 1 V Fully Integrated CMOS Transformer Based Mixer with 5.5 dB Gain, 14.5 dB SSB Noise Figure and 0 dBm Input IP3," in *European Solid-State Circuit Conference*, Estoril, Portugal, September 2003.

[7] M. Tiebout, C. Sandner, H.-D. Wohlmuth, N. Da Dalt, E. Thaller, "A Fully Integrated 13 GHz Delta-Sigma Fractional-N PLL in 0.13 μm CMOS," in *ISSCC04 Digest of Technical Papers*. 2004 IEEE International Solid-State Circuits Conference, February 2004.

[8] R. Thueringer, M. Tiebout, W. Simbuerger, C. Kienmayer, A. Scholz, "A 17 GHz Linear 50 Ohm Output Driver in 120 nm Standard CMOS," in *RFIC03 Digest of Technical Papers*. 2003 IEEE Radio Frequency Integrated Circuits Symposium, june 2003.