A 5.25 GHz SiGe Bipolar Power Amplifier for IEEE 802.11a Wireless LAN

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Abstract— **An integrated wireless LAN radio frequency power amplifier (PA) for 5.25 GHz has been realized in a 40 GHz-f_T, 0.35 μm-SiGe-Bipolar technology. The single-ended 3-stage power amplifier uses on-chip inductors and a short on-chip stripline for the interstage matching. At 3.3 V supply voltage the OP1dB is 23.8 dBm, and a saturated output power of 25.9 dBm is achieved at 5.25 GHz. The PAE at the OP1dB is 24 %. The small-signal gain is 27 dB.**

Index Terms - **WLAN, power amplifiers, SiGe, onchip matching, PAE.**

I. Introduction

Wireless LAN is one of the major mass-production markets. As customers desire more data throughput at low price, first IEEE 802.11a chipsets have become available. However the power amplifiers (PA) are dominated by III/V compound semiconductors with very good rf characteristics but cost disadvantages. Today, there exist only a small amount of Si or SiGe based PA demonstrations [1], [2], [3], [4] with most of them focused on cellular phone applications.

Aim of the work presented here was the realization of an integrated power amplifier for the 5.25 GHz wireless LAN band. The amplifier circuit is based on three stages, using on-chip inductors for the interstage matching between the first two stages and a stripline for the matching to the output stage. The technology features a low-ohmic low-inductance sinker ground-connection to enable a single-ended PA at high frequencies without the need of parallel bond-wires [5]. This reduces the die size, as no ground vias are required anymore and helps to use smaller packages. With this, the whole PA was manufactured using a VQFN package for the test setup.

II. Technology

The technology used in this work is a 0.35 μm SiGe-bipolar process. Based on a volume-process presented in [6], [7] it features a bipolar junction transistor with a f_T of 40 GHz and a three layer Al-metalization with an 2.8 μm thick upper layer. Further devices are a vertical pnp transistor, poly-Si resistors, MIM capacitors, MOS capacitors and inductors. The worst-case collector-base breakdown voltage is BVCB0 = 15.5 V and the worst-case collector-emitter breakdown voltage is BVCE0 = 3.8 V. In order to realize the mentioned low-inductance, low-ohmic connection the substrate resistance is enormously decreased - down to 15 $m\Omega cm$. Using highly doped epi layers, a low inductance connection between the lowest layer of metal and substrate is achieved. The structure created in this way has a series resistance of only 50 Ω/1 mm^2 and a neglectable series inductance.

Fig. 1 shows the die photograph of the fully integrated power amplifier. The die size is 1.3 x 1 mm^2.

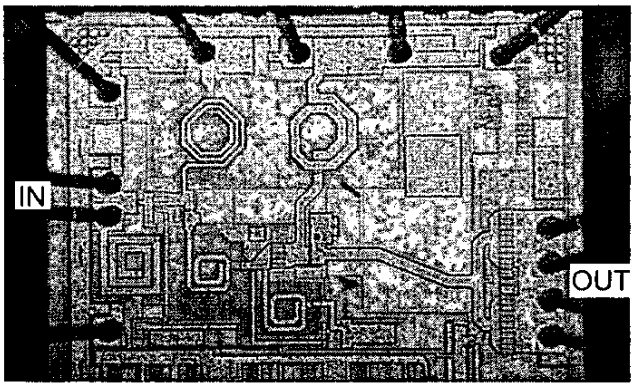

Fig. 1. Die micrograph of the power amplifier rf section. (size: 1.3 x 1 mm^2).

III. Circuit Design

Fig. 2 shows the circuit diagram of the power amplifier. The first stage is matched to the input using a shunt inductance and the input DC-block capacitor. The bias current is supplied using a resistor connected to the current-source. The effective emitter area of the first stage transistor is 90 μm^2. This first stage is matched to the second amplifier stage using a T-network consisting of two capacitors and a series inductor. To improve the quality factor of the inductances, octangular formed inductors have been used.

The second stage effective emitter area is 225 μm^2. In difference to the other stages which are biased via a resistor, the bias feeding was realized using a small inductor to prevent parasitic oscillations. The output stage transistor effective emitter area is 900 μm^2. As such a large transistor has a very low input impedance [8], a matching network with a highest possible quality factor is necessary. This can only be obtained by high quality factors in the inductance, which is limited by the used substrate and the current density limitations.

As octangular formed inductors still did not have sufficient quality factors, the inductance between output transistor and second stage was replaced by a microstrip transmission line. It was realized using the thick upper layer for the signal line and the lowest Al layer connected with the ground sinker. This guarantees a perfect ground connection at the lower ground metalization. Furthermore, the parasitic capacitance and resistance due to the substrate material is shorted. Hence lower loss in the matching network is obtained. The capacitance of the transmission line to ground is used in addition

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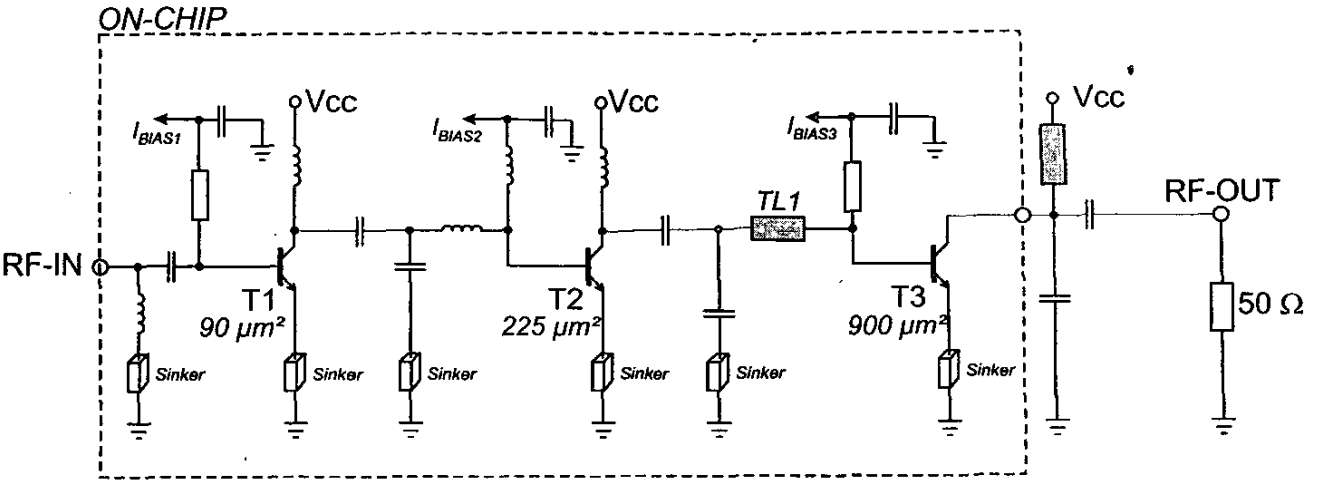

Fig. 2. Simplified Circuit diagram of the integrated power amplifier.

to the shunt capacitance and lowers the required shunt capacitance. Fig. 3 shows the simulation results for the microstrip transmission line structure.

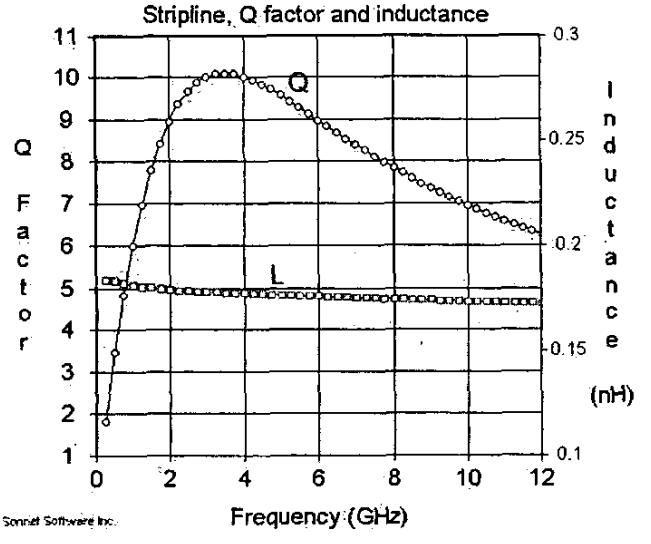

Fig. 3. Simulation results for inductance and quality factor of the microstrip transmission line structure.

The inductors and the stripline are modeled with an electromagnetic (EM) simulation software Sonnet [9]. Preassumptions on the inductances are made using inductance equations found in [10], [11]. Capacitances were realized as *m*etal/*i*solator/*m*etal capacitors (MIM-CAPs). Modeling issues on MIM-caps can be found in [12].

IV. Experimental Results

Fig. 4 shows the power amplifier test-board. The substrate material is FR4 as used for volume production. External matching networks have been built and optimized to get the desired performance with use of transmission lines and high-Q Epcos capacitors. The chip is packaged and reflow soldered onto the test-board.

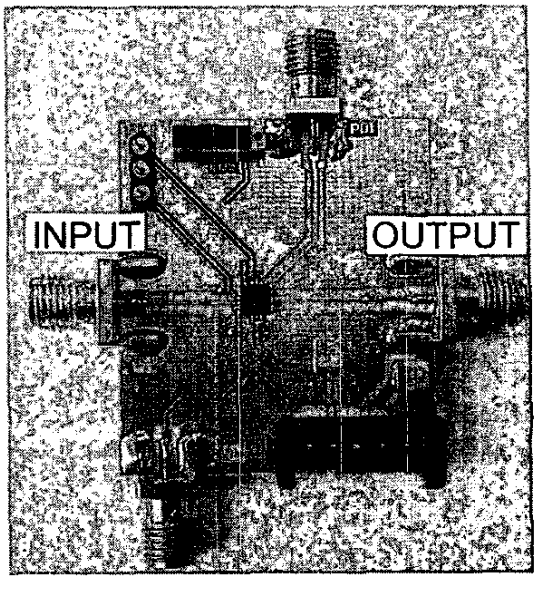

Fig. 4. Photograph of the power amplifier test board.

Fig. 5 shows the measured power transfer characteristic. The maximum output power is 25.9 dBm at 3.3 V supply voltage and 5.25 GHz. The maximum PAE is 30%. Fig. 6 shows the corresponding current consumption vs. input power additionally to the small signal gain curve. The quiescent current is 180 mA. Fig. 7 shows the frequency response for linear operation using an input power of -2.5 dBm. It shows a small deviation from the center frequency.

The linearity for wireless LAN applications was tested using an Agilent WLAN-OFDM Error Vector Magnitude measurement setup in CW-mode. Fig. 8 shows the spectral mask for several average input power levels. Additionally the Error Vector Magnitude [13] behaviour is shown in Fig. 9. It shows that the maximum average output power for a 54 Mbit/s signal is about 17 dBm. Finally, Table I shows the performance summary.

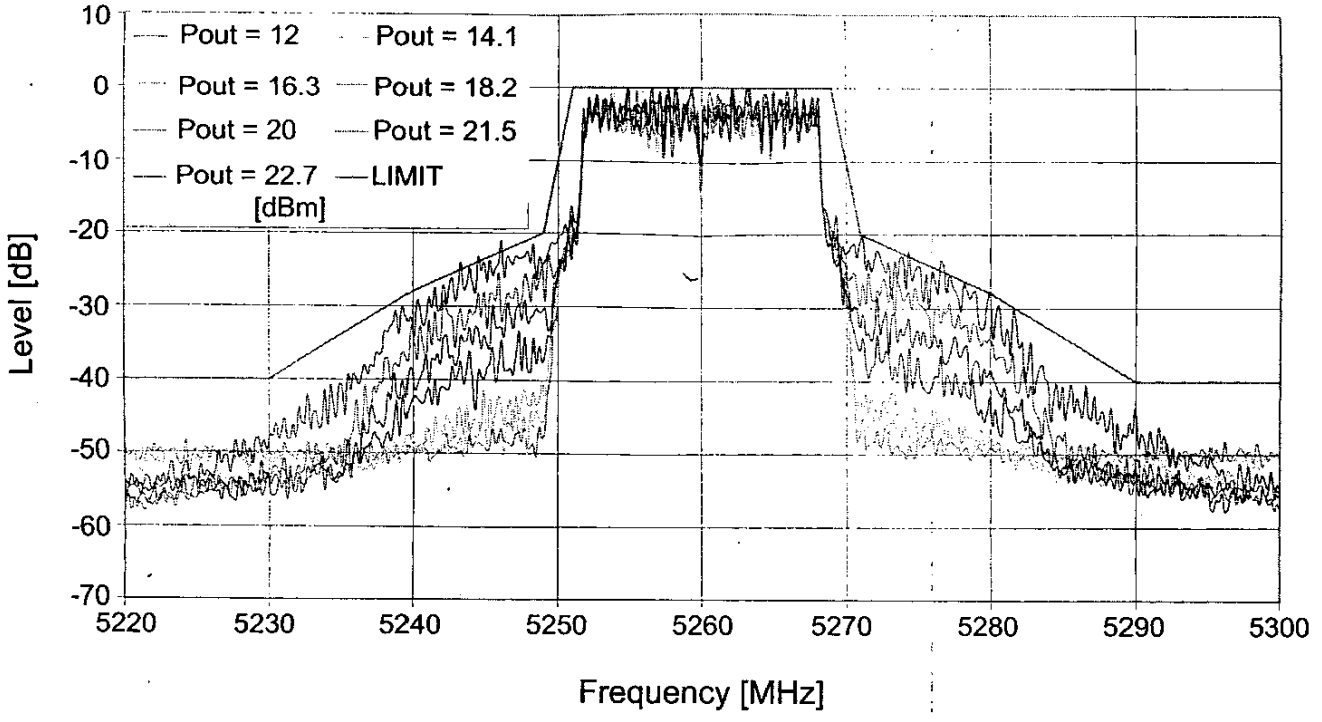

Fig. 8. Measured Spectrum Mask (OFDM 54Mbit/s, IEEE 802.11a) frequency characteristic.

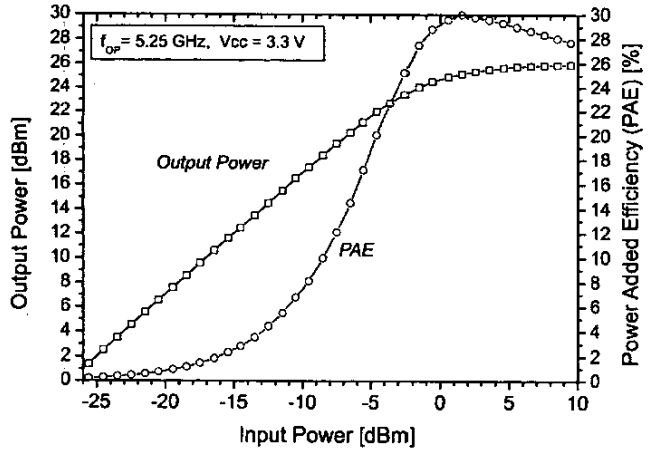

Fig. 5. Measured power transfer characteristic.

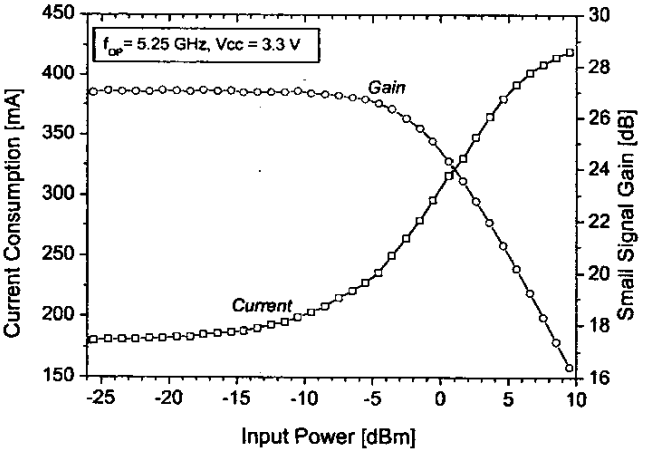

Fig. 6. Measured current consumption and small signal gain vs. input power.

V. Conclusions

We have demonstrated an integrated wireless LAN radio frequency power amplifier (PA) for the 5.25 GHz Wireless LAN band. It has been realized in a 40 GHz-f_T, 0.35 μm- SiGe-Bipolar technology using low ground inductance sinker connections for the prevention emitter degradation. The single-ended 3-stage power amplifier uses on-chip inductors and a short on-chip stripline for the interstage matching. At 3.3 V supply voltage the OP1dB is 23.8 dBm with a PAE of 24 %, and the saturated output power of 25.9 dBm is achieved at 5.25 GHz.

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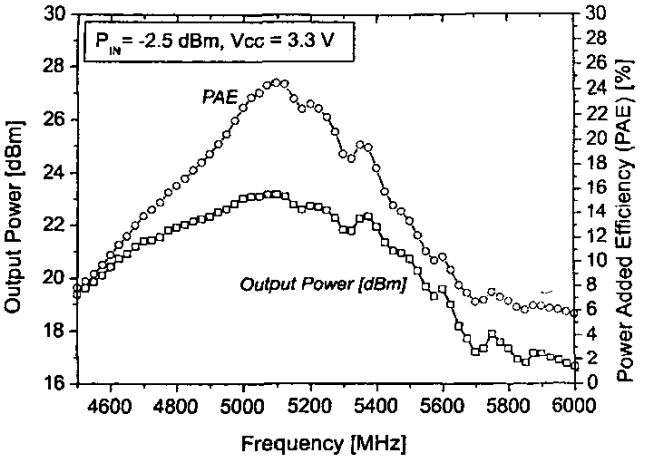

Fig. 7. Measured power amplifier frequency response.

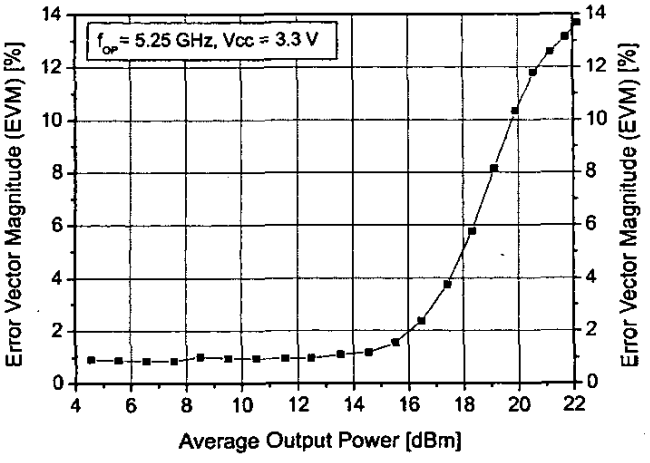

Fig. 9. Measured Error Vector Magnitude (EVM) vs. average output power.

Operating frequency	5.25 GHz
Small-signal gain	27 dB
Supply voltage	3.3 V
Maximum output power	25.9 dBm
Power-added efficiency	30%
Output 1 dB compression point (OP1dB)	23.8 dBm
Power-added efficiency @ OP1dB	30%

TABLE I
PERFORMANCE SUMMARY.

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