110-GHz Static Frequency Divider in SiGe Bipolar Technology

Saverio Trotta[1, 2], Herbert Knapp[1], Thomas F. Meister[1], Klaus Aufinger[1], J. Böck[1], Werner Simbürger[1], Arpad L. Scholtz[2]

[1] Infineon Technologies AG, Otto-Hahn Ring 6, 81730 Munich, Germany
[2] Vienna University of Technology, Karlsplatz 13, A-1040 Vienna, Austria
E-mail: Saverio.Trotta@infineon.com

Abstract — **We present a static frequency divider designed in a 225 GHz f_T SiGe bipolar technology. The divider has a divide ratio of four and it is operational from 200 MHz up to 110 GHz (limited by the measurement equipment). At a -5.2 V power supply, the circuit, including the two dividers and the input and output stages, consumes less than 260 mA.**

Index Terms — **SiGe, Static Frequency Divider**

I. INTRODUCTION

Frequency dividers are used in a wide variety of applications. For InP-based HBT technologies, static dividers operating up to 150 GHz [1, 2] and 152 GHz [3] have been presented.
Static frequency dividers in SiGe bipolar technology (HBTs) with maximum frequency of 86 GHz [4], 96 GHz [5] and 102 GHz [6] have been reported recently. In this paper we present a 110 GHz wide range static frequency divider.

II. CIRCUIT DESIGN

The divider has a divide ratio of four and consists of two master-slave flip-flops, an input clock buffer and an output buffer (Fig. 1). The circuit is fully differential. The input buffer on the one hand improves the input sensitivity at low frequencies by increasing the slew rate of the clock signal. On the other hand its bandwidth limits the maximum operational frequency of the divider. In simulation the clock signal at the output of the buffer at 110 GHz shows a swing of 85m V_{pp} single-ended.

The signal from the buffer is applied via three emitter followers (EFs, Level Shift Block) to the first flip-flop. Each flip-flop consists of two static latches. The latches are designed in ECL logic (Fig. 2). The input clock signal is applied from the buffer to the first divider via three pairs of emitter followers (Fig. 1). The performance of this flip-flop is improved by using special techniques. It has been demonstrated in [7, 8] that high-speed operation in a latch design can be achieved by using asymmetric techniques, without performance loss at low frequencies. Asymmetric means different current levels in the reading and the holding paths of the latch at high frequencies. This can be seen in Fig. 3. In this case, the sense period is larger than the store period [7, 8]. There are different ways to achieve the current behavior as shown in Fig. 3:

1) In [7], different sizes for transistors in the latch are used: The emitter size of the transistors in the holding circuit is smaller than the size in the reading circuit (Fig. 2).

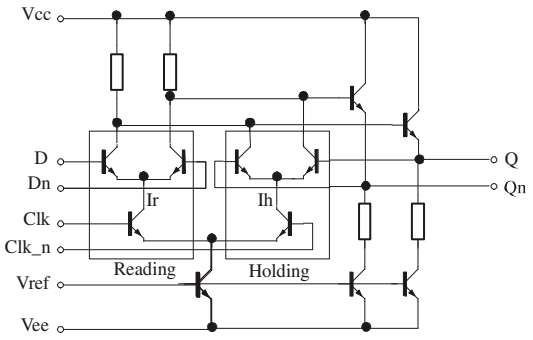

Fig. 2 Latch schematic (the emitter size of the transistors in the holding circuit is smaller than the size in the reading circuit)

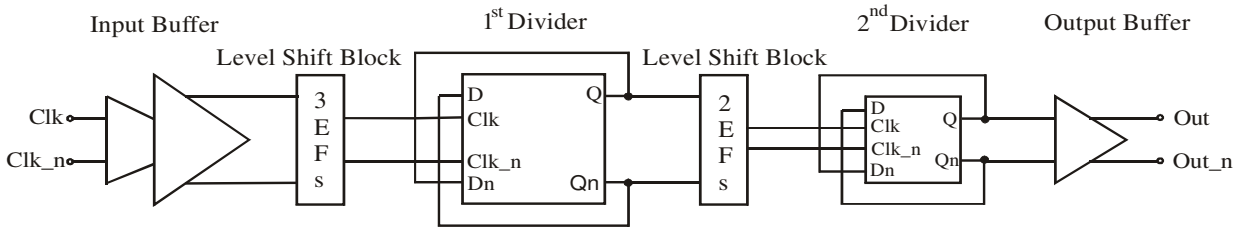

Fig. 1 Static frequency divider by 4 block diagram

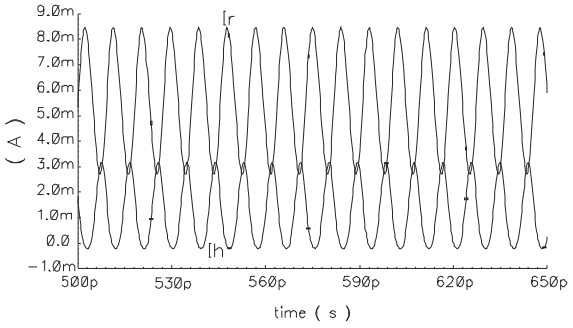

Fig. 3 Current behavior in the reading and holding path at 110 GHz: the current is unbalanced on the reading side

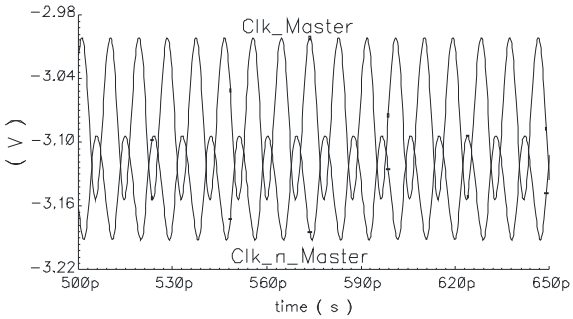

Fig. 4 DC-offset of the Clk_n signal at 110 GHz

However, the difference in the size must not be too large, otherwise, the circuit will not work at low frequencies. If the sizes show a large difference, the circuit works like a superdynamic flip-flop [9].

2) A combination of the technique explained in 1) with a different dc-level for the clock-signal at the input of the latch is used in [8] (Fig. 4). In this way, the performance of the flip-flop is improved at high frequencies.

A Level Shift Block is used to apply the clock signal to the flip-flop. The main drawback of this technique arises from this block. To achieve the DC shift, a different current density (not the optimum) is used for the emitter followers in the Level Shift Block for the clock path (Clk), the one which drives the reading path. As a result, this path is not as fast as the inverted one (Clk_n). The level shift is usually accomplished by cascaded emitter followers. For large DC offset more than two emitter followers are needed.

In this work we have used the same emitter followers in the Level Shift Block for both Clk and Clk_n paths in the latch (Fig. 5). The emitter followers operate at the same current density and we just add a resistor in the first emitter follower of the Clk_n path in the Level Shift Block to achieve the DC offset (Fig. 6). Note that this technique for generating the DC offset can be used with a different number of emitter followers.

The performance of this divider depends on the value of the DC-offset resistor. With a very large value, it is possible to achieve very high operational frequency,

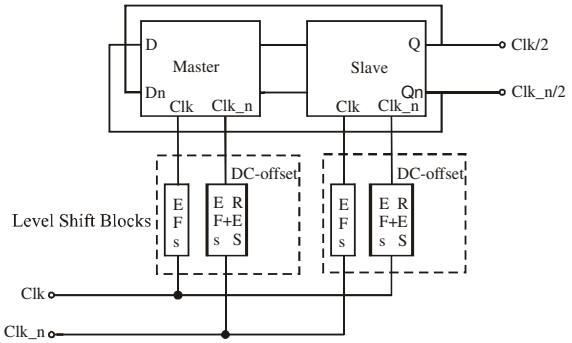

Fig. 5 Master-Slave D flip-flop in a divider configuration

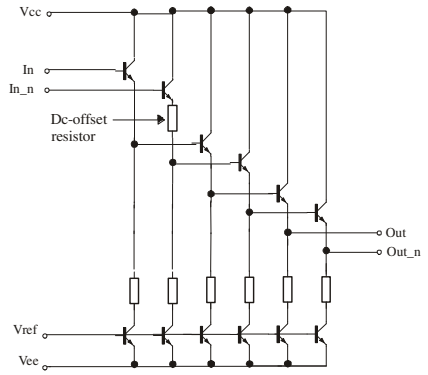

Fig. 6 Level Shift Block schematic

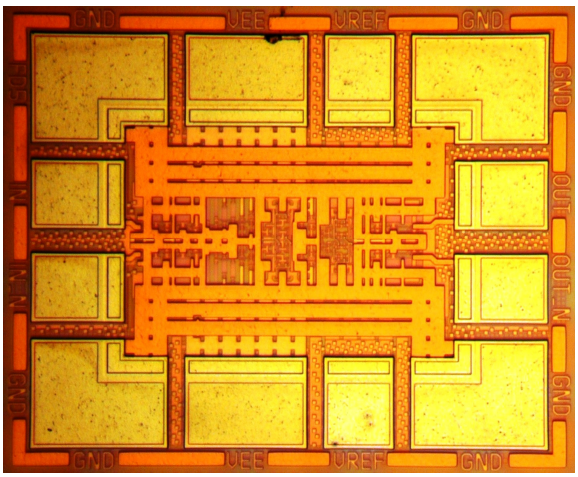

Fig. 7 Chip photograph of the static frequency divider (size 550 m x 450 m)

but then it will be no more a wide-range static frequency divider [9].

The output buffer consists of emitter followers and a differential amplifier.

Two circuits which generate the Vref have been used to drive all the current sources of the chip (current mirror with beta helper). Moreover, Vref can be also controlled externally. In this way we can adjust the current density in each current source.

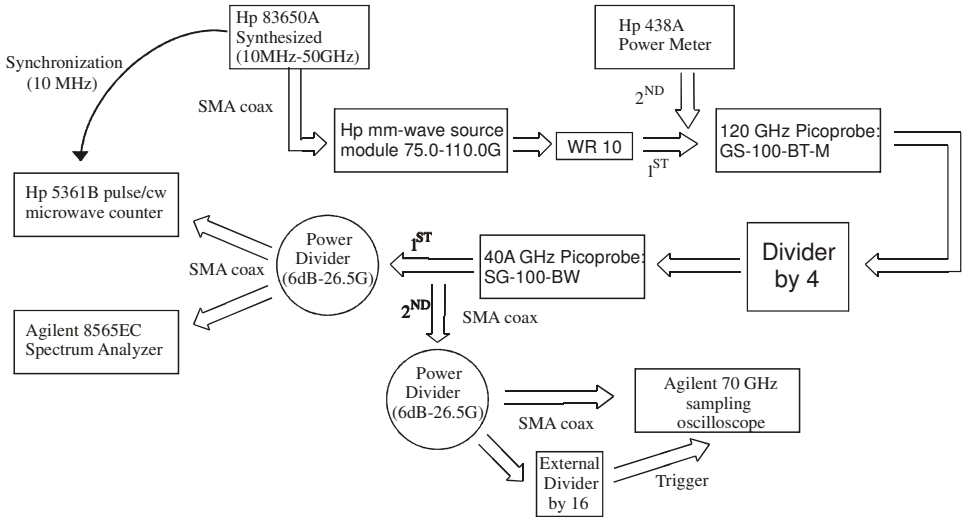

Fig. 8 Measurement setup in the 75-110 GHz frequency range

III. TECHNOLOGY

The frequency divider is manufactured in an advanced 225 GHz f_T SiGe:C bipolar process based on the technology presented in [6]. It uses shallow and deep trench isolation. The transistors have a double-polysilicon self-aligned emitter base configuration with a SiGe:C base which is integrated by selective epitaxial growth. The transistors are fabricated using 0.3 m lithography. The minimum effective emitter width is 0.14 m. All the transistors in the chip operate at a current density of 6.5 mA/ m^2. The chip photograph is presented in Fig. 7. The size of the first flip-flop is 170 m x 60 m.

IV. TEST SETUP

Measurements were performed on wafer, at room temperature. Different test setups have been used to measure the input power sensitivity of the divider from 200 MHz to 110 GHz. We have used a single-ended clock signal to drive the circuit at all frequencies. The test setups differ only at the input port of the divider. Since the divide ratio is four and the highest frequency signal provided by the signal source is 110 GHz, we have used a single-ended dc-to-40 GHz probe at the divider output in all setups. The output signal was applied via coaxial cables to a frequency counter and to a spectrum analyzer first and also to a 70 GHz sampling oscilloscope.

In the 200 MHz-50 GHz frequency range the signal source has been connected via a coaxial cable to a dc-to-67 GHz differential coaxial GSSG probe. The complementary input was terminated by using a coaxial 50 Ω load on the probe. With the same input probe, we measured also the sensitivity between 50 and 67 GHz. The input signals with frequencies from 50 to 75 GHz were generated by a millimeter-wave source module. The signal has been applied to the probe via a waveguide-to-coaxial adapter.

To test the sensitivity in the range of 60 to 75 GHz, a probe for the E-band has been used. The frequency range between 60 to 67 GHz overlaps the previous setup. The values we got for the input power from both tests in this range match well.

Another millimeter-wave source module has been used to drive the chip in the W-band. The input probe was a 120 GHz probe connected to the source module with a W-band wave guide. The complete setup for the measurement in the 75-110 GHz range is shown in Fig. 8.

After the measurement of the sensitivity in one frequency range, we have determined the effective level of the power delivered to the input probe for each measured frequency point by connecting a power meter at the end of the coaxial cable or at the end of the wave guide for the E and W band. The loss of the probes as well as the V-band to coaxial cable adapter (used in the 50-67 GHz frequency range) has not been taken into account.

V. MEASUREMENT RESULTS

Operating with a supply voltage of -5.2 V the divider consumes less than 260 mA. According to simulation, each latch in the first divider stage has a power dissipation of 170 mW. Fig. 9 shows the oscilloscope screenshot of the 27.5 GHz output of the divider, with a 110 GHz single-ended input clock signal. The spectrum of this signal is shown in Fig. 10 and its 120 MHz span zoom in Fig. 11. The measured input sensitivity curve is shown in Fig. 13. Because of the slew rate of the sinusoidal input signal, at low frequencies, the circuit needs more input power. The input sensitivity can be improved in the 200 MHz-50 GHz frequency range, if we increase the currents provided by the current sources in the circuit. The total current consumption in this case is 290 mA.

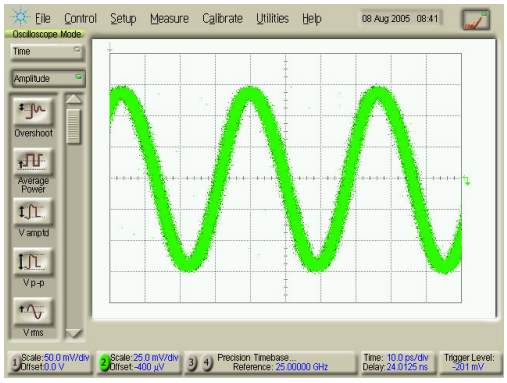

Fig. 9 Single-ended output signal (f_{in} = 110 GHz)
X-axis: 10 ps/div, y-axis: 25 mV/div.

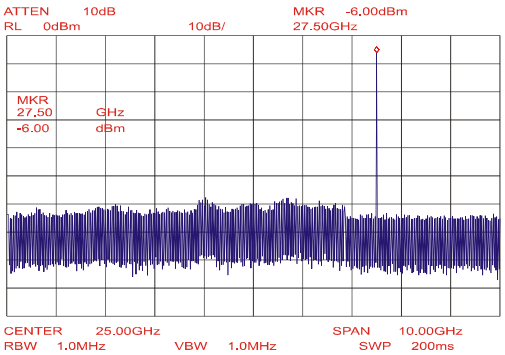

Fig. 10 Measured spectrum of the divider 27.5 GHz output signal (10 GHz span)

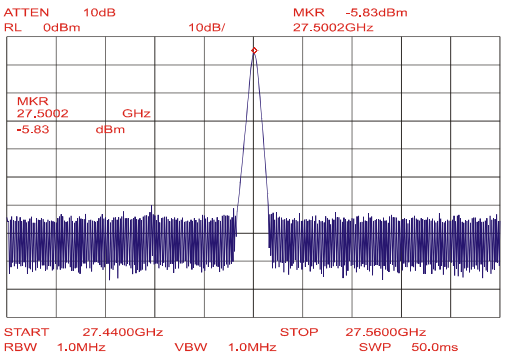

Fig. 11 Measured spectrum of the divider 27.5 GHz output signal (120 MHz span)

VI. CONCLUSION

A static frequency divider by four has been designed in a 225 GHz f_T SiGe bipolar technology. The measurements have been performed on wafer. Very high speed operation has been achieved by making the first divider stage asymmetric. At very high frequencies the reading period becomes larger than the holding period. The divider operates between 200 MHz and 110 GHz (limited by the measurement setup). To the authors knowledge this is the highest frequency of operation for a static SiGe divider reported to date.

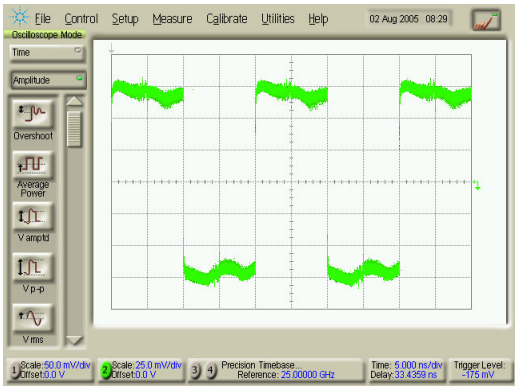

Fig. 12 Single-ended output signal (f_{in} = 200 MHz).
X-axis: 5 ns/div, y-axis: 25 mV/div.

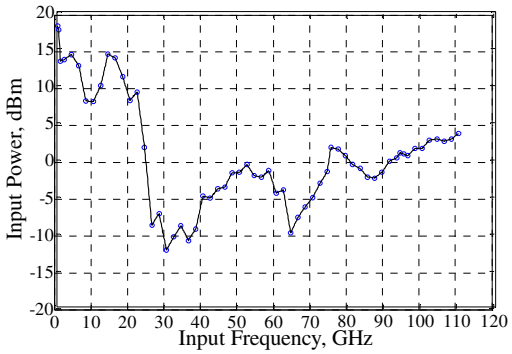

Fig. 13 Input sensitivity of the divider

REFERENCES

[1] Z. Griffith, M. Dahlstrom, M. J. W. Rodwell, M. Urteaga, R. Pierson, P. Rowell, B. Brar, S. Lee, N. Nguyen, C. Nguyen, Ultra High Frequency Static Dividers > 150 GHz in a Narrow Mesa InGaAs/InP DHBT Technology in *IEEE BCTM* 2004, pp. 176-179.

[2] D. A. Hitko, T. Hussain, J. F. Jensen, Y. Royter, S. L. Morton, D. S. Mathews, R. D. Rajavel, I. Milosavljevic, C. H. Fields, S. Thomas III, A. Kurdoghllan, Z. Lao, K. Elliott, M. Sokolich, A Low Power (45mW/latch) Static 150GHz CML Divider , in *IEEE CSICS Digest* 2004, pp. 167-170.

[3] G. He, J. Howard, M. Le, P. Partyka, B. Li, G. Kim, R. Hess, R. Bryie, R. Lee, S. Rustomji, J. Pepper, M. Kail, M. Helix, R. B. Elder, D. S. Jansen, N. E. Harff, J. F. Prairie, E. S. Daniel, B. K. Gilbert, Self-Aligned INP DHBT with f_T and f_{MAX} over 300 GHz in a new Manufactured Technology , in *IEEE Electron Device Letters*, vol. 25, NO. 8, August 2004, pp. 520-522.

[4] H. Knapp, M. Wurzer, T. F. Meister, K. Aufinger, J. B ck, S. Boguth, H. Sch fer, 86 GHz Static and 110 GHz Dynamic Frequency Dividers in SiGe Bipolar Technology , in *Microwave Symp. Dig.*, vol. 2, June 2003, pp. 1067-1070.

[5] A. Rylyakov, T. Zwick, 96 GHz Static Frequency Divider in SiGe Bipolar Technology , in *IEEE Journal of Solid-State Circuits*, vol. 39, No. 10, October 2004, pp. 1712-1715.

[6] J. B ck, H. Sch fer, H. Knapp, K. Aufinger, M. Wurzer, S. Boguth, T. B ttner, R. Stengel, W. Perndl, T. F. Meister, 3.3 ps SiGe Bipolar Technology , *IEEE IEDM* 04, pp. 255-258.

[7] Y. Suzuki, Z. Yamazaki, Y. Amamiya, S. Wada, H. Uchida, C. Kurioka, S. Tanaka, H. Hida, 120 Gb/s Multiplexing and 110 Gb/s Demultiplexing ICs , in *IEEE Journal of Solid-State Circuits*, vol. 39, No. 12, December 2004, pp. 2397-2402.

[8] S. Trotta, J. Sundermeyer, N. Weber, J. Saurer, A Novel Design of an Asymmetric D-Latch , *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Sept. 2004, pp. 261-264.

[9] B. Razavi, Design of integrated circuits for optical communications , McGraw Hill, 2003, pp. 341-349.