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Editorial

Signal Processing with High Complexity: Prototyping and Industrial Design

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Some modern applications require an extraordinary large amount of complexity in signal processing algorithms. For example, the 3rd generation of wireless cellular systems is expected to require 1000 times more complexity when compared to its 2nd generation predecessors, and future 3GPP standards will aim for even more number-crunching applications. Video and multimedia applications do not only drive the complexity to new peaks in wired and wireless systems but also in personal and home devices. Also in acoustics, modern hearing aids, or algorithms for dereverberation of rooms, blind source separation and multichannel echo cancellation are complexity hungry. At the same time the anticipated products also put on additional constraints like size and power consumption when mobile and thus battery powered. Furthermore, due to new developments in electro-acoustic transducer design, it is possible to design very small and effective loudspeakers. Unfortunately, the linearity assumption does not hold any more for this kind of loudspeakers, leading to computationally demanding nonlinear cancellation and equalization algorithms.

Since standard design techniques would either consume too much time or not result in solutions satisfying all constraints, more efficient development techniques are required to speed up this crucial phase. In general such developments are rather expensive due to the required extraordinary high complexity. Thus, de-risking of a future product based on rapid prototyping is often an alternative approach. However, since prototyping would delay the development, it often makes only sense when it is well embedded in the product design process. Rapid prototyping has thus evolved by applying new design techniques more suitable to support a quick time to market requirement.

This special issue focuses on new development methods for applications with high complexity in signal processing and on showing the improved design obtained by such methods. Examples of such methods are virtual prototyping, HW/SW partitioning, automatic design flows, float to fix conversions, and automatic testing and verification.

We received seven submissions of which only four were accepted.

In *Rapid industrial prototyping and SoC design of 3G/4G wireless systems using an HLS methodology* the authors Yuanbin Guo et al. present their industrial rapid prototyping experiences on 3G/4G wireless systems using advanced signal processing algorithms in MIMO-CDMA and MIMO-OFDM systems. Advanced receiver algorithms suitable for implementation are proposed for synchronization, MIMO equalization, and detection, VLSI-oriented complexity reduction is presented. This design experience demonstrates that it is possible to enable an extensive architectural analysis in a short time frame using HLS methodology by abstracting the hardware design iterations to an algorithmic C/C++ fixed-point design, which in turn significantly shortens the time to market for wireless systems.

In *Generation of embedded hardware/software from systemC* the authors Salim Ouadjaout and Dominique Houzet present a design flow to reduce the SoC design cost. This design flow unifies hardware and software using a single high level language and thus decreases the manual errors by rewriting design code. It integrates hardware/software (HW/SW) generation tools and an automatic interface synthesis through a custom library of adapters. The approach is validated on a hardware producer/consumer case study and on the design of a given software-radio communication application.

In *Efficient design methods for embedded communication systems* the authors Martin Holzer et al. analyze a complete design process to exhibit inefficiencies. The lack of an integrated design methodology is argued. High level characterisation, virtual prototyping, automated hardware/software partitioning, and floating-point to fixed-point data conversion are bottlenecks to solve in such a methodology. For each point, authors present and compare several tools and algorithms leading to an efficient fast prototyping framework. Examples are given in the field of high-complexity communication systems but can be extended to other complex application fields.

In *Fixed-point configurable hardware components* the authors Romuald Rocher et al. propose a flexible scheme for fixed-point optimization in order to better exploit advances in VLSI technology. After determining the dynamic range and the binary point, a data word-length optimization follows by introducing a suitable user-defined cost function. This central cost function, which, for example, depends on chip area and/or energy consumption, is to be minimized under the constraint of a pre-defined thresholded signal-to-quantization noise ratio (SQNR). Through use of analytical models the design time can be significantly reduced. A 128-tap LMS filter design exemplarily explores the fixed-point search space and demonstrates the benefits of the proposed scheme.

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Markus Rupp received his Dipl.-Ing. degree in 1988 at the University of Saarbruecken, Germany, and his Dr.-Ing. degree in 1993 at the Technische Universitaet Darmstadt, Germany. He is presently a Full Professor for digital signal processing in mobile communications at the Technical University of Vienna. He is Associate Editor of IEEE Transactions on Signal Processing, EURASIP Journal of Applied Signal Processing, EURASIP Journal on Embedded Systems and is elected AdCom Member of EURASIP. He authored and co-authored more than 200 papers and patents on adaptive filtering, wireless communications, and rapid prototyping.

Thomas Kaiser received the Ph.D. degree in 1995 with distinction and the German habilitation degree in 2000, both in electrical engineering from Gerhard-Mercator-University Duisburg. In the summer of 2005 he joined Stanford's Smart Antenna Research Group (SARG) as a Visiting Professor. Now he holds a chair on communication systems at the University of Hannover, Germany, and is a founder of the spin-off company mimoOn GmbH. He has published more than 100 papers and has co-edited four books on ultra-wideband and smart antenna systems. He is the founding Editor-in-Chief of the IEEE Signal Processing Society e-letter. His research interest focuses on applied signal processing with emphasis on multi-antenna systems, especially its applicability to ultra-wideband systems.

Jean-Francois Nezan is an Assistant Professor at National Institute of Applied Sciences of Rennes (INSA) and a member of the IETR laboratory in Rennes. He received his postgraduate certificate in signal, telecommunications, images, and radar sciences from Rennes University in 1999, and his engineering degree in electronic and computer engineering from INSA-Rennes Scientific and Technical University in 1999. He received his Ph.D. degree in electronics in 2002 from the INSA. His main research interests include image compression algorithms and multi-DSP rapid prototyping.

Gerhard Schmidt received his Dipl.-Ing. degree in 1996 and his Dr.-Ing. degree in 2001, both at Darmstadt University of Technology, Germany. Presently, he is working as a senior research engineer in the acoustic signal processing group at Harman/Becker Automotive Systems in Ulm, Germany. His main research interests include adaptive methods for speech and audio processing.

EURASIP JOURNAL ON EMBEDDED SYSTEMS

Special Issue on
Embedded Systems for Intelligent Vehicles

Call for Papers

The transport sector is seeking new technology to improve safety, driver comfort, and efficient use of infrastructures. Computer vision, range sensors, adaptive control, and networking, among the others, target problems like traffic flow control, pedestrian protection, lane-departure monitoring, smart parking facilities, and driver assistance in general. Embedded systems are sought after to implement technologically advanced solutions in smart vehicles. The automotive industry addresses mass markets in which embedded systems have a dramatic impact on the final consumer market price. From the point of view of academic research, intelligent vehicles represent a complete and sufficiently complex benchmark for integrating sensors, actuators, and control to test prototypes of autonomous systems. Additionally, intelligent vehicles are a challenging environment with a direct applicative aspect for research on autonomous systems, intended as systems reacting in a closed loop with the environment.

Topics of interest include smart sensors, sensor fusion, embedded vehicle controls, autonomous vehicles, centralized and local traffic control, GSM and ad hoc networking, Bluetooth and IEEE 802.15.4 technologies, driver-computer interface, signal processing for embedded environments, autonomous components, and intelligent control.

This special issue focuses on new results of research work in the field of embedded systems for intelligent vehicles. Several main keywords are:

- Intelligent vehicles
- Autonomous vehicles
- Embedded systems versus autonomous systems
- Computer vision in embedded systems
- Laser/radar range sensors
- Multiple sensor embedded architectures
- Sensor networks for automotive applications
- Vehicle networking
- Obstacle detection and tracking
- GPS-based navigation
- Design methodologies
- FPGA for embedded systems with application to intelligent vehicles

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Special Issue on Networks-on-Chip

Call for Papers

Single chip and embedded systems are becoming increasingly complex and heterogeneous. Such systems-on-chip (SoCs) imply the seamless integration of numerous IP cores performing different functions and operating at different clock frequencies. On one hand, this integration process requires standard interface sockets to allow for design reuse of IP components across multiple platforms. On the other hand, it is causing the scalability limitations of state-of-the-art SoC busses to emerge.

Networks-on-chip (NoCs) are generally viewed as the ultimate solution for the design of modular and scalable communication architectures, and provide inherent support to the integration of heterogeneous cores through the standardization of the network boundary. NoC architectures loosen the delay bottleneck in signal propagation across deep-submicron interconnects and are likely to improve design predictability, although their area and power overheads still remain critical issues to be addressed by research.

This special issue is dedicated to the aspects of architecture and design methodology of on-chip interconnection systems and their applications. Topics of interest include, but are not limited to:

- Design flows for NoCs and MP-SoC platforms.
- Modeling, simulation, and test of NoC systems.
- On-chip network monitoring and management.
- Architectures and topologies.
- Performance and trade-off analysis.
- Mapping and scheduling applications/communication.
- Energy efficiency and power management.
- Fault tolerance and reliability issues.
- Routing and addressing issues.
- QoS in NoC systems.
- Reconfigurability issues.
- Industrial case studies of SoC designs using the NoC paradigm.

Authors are encouraged to submit high-quality research contributions that will not require major revisions.

Authors should follow the VLSI Design manuscript format at http://www.hindawi.com/GetJournal.aspx?journal=VLSI. Prospective authors should submit an electronic copy of their complete manuscript through the VLSI Design manuscript tracking system at http://www.hindawi.com/mts/, according to the following timetable:

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