Transmitter and Receiver Circuits for Serial Data Transmission over Lossy Copper Channels for 10 Gb/s in 0.13 μm CMOS

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***Abstract*— This paper presents a transmitter and receiver for high speed serial data links including pre-distortion and equalization circuits. The circuits allow data transmission over lossy copper channels up to 10 Gb/s and beyond. The transmitter uses a three tap FIR-filter for pre-distortion. A full rate FIR design allows a low latency and provides a smooth filter characteristic. An analog equalizer in the receiver with high-pass filter characteristic is implemented. Transmitter and receiver use high speed differential current mode logic without using passive inductors. Measurements over legacy channels show error free transmission (BER $< 10^{-12}$) of 11 Gb/s for a 5 meter long RG58 cable and 9 Gb/s over a state of the art 22 cm long dual inline memory module (DIMM)- motherboard channel.**

I. Introduction

Data communications in the 10 Gb/s range was reserved for fiber-optics systems in the past. Increasing demand of data bandwidth and a trend towards serial inter-chip communications in computer systems creates a new field for gigabit communications. System vendors want to avoid to deploy new backplanes because of high development and production costs. Increased bandwidth over legacy copper channels requires new transmitter and receiver circuit technology.

Channel distortion results in inter-symbol interference (ISI). Pre-distortion techniques using symbol-spaced FIR-filters are widely used to reduce signal parts from precursor and post-cursor bits at the receiver [1] [2] [3]. Heavy channel distortion and high data rates require a large number of taps. In latency critical systems as memory-busses time consuming pre-distortion techniques are not practical. Pulse shaping techniques presented in [4] and single tap pre-emphasis using digital differentiators [5] suffer from their analog implemented delay circuits.

To minimize latency while using clock-defined delay cells the number of taps used in this work is limited to three. Furthermore D-Latches are used instead of master-slave D-FF resulting in a further reduction of latency and stronger emphasis of high frequency signal parts.

In the receiver an analog equalizer is implemented allowing a further amplification of high frequency signal parts. Equalizers with adjustable filter characteristics for 10 Gb/s are already presented in [6] using BiCMOS technology and inductors, [7] using 0.13 μm CMOS and inductors and [8] using 0.11 μm CMOS. In this work all circuits are designed in 0.13 μm CMOS and no inductors are used to achieve minimum chip area.

II. Transmitter Circuit Design

Figure 1 shows the block diagram of the implemented transmitter. The transmitter is fully designed in CML logic and applies a 3-tap FIR pre-emphasis.

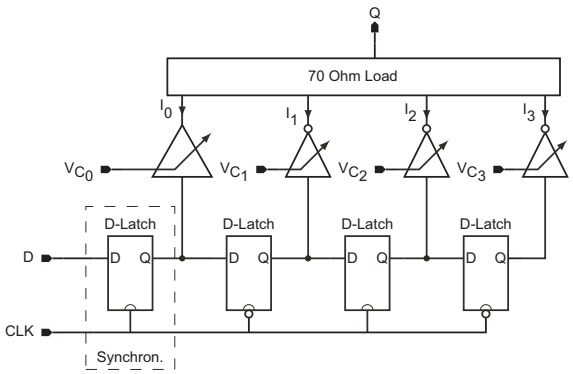

Fig. 1. Transmitter block diagram. Time shift is realized with D-Latches instead of conventional D-FF design. First D-Latch synchronizes clock and data signals and is not element of the FIR-filter.

The transmitter is designed as a full rate system. The time shifted data signals are realized by D-type latches whereas following latches are feed with inverted clock signals. Each latch adds a time delay T_D of $1/(2 \cdot f_C)$ where f_C is the clock frequency. The first D-Latch at the data input D was introduced to give a clock synchronous data pattern at the main driver. This latch is needed because the transmitter is feeded with not synchronous clock and data signals in the test environment. It has no influence on the FIR-filter characteristics.

Figure 2 shows the simulated frequency response of the idealized FIR-filter illustrating the benefits of using D-Latches instead of D-FF. The clock frequency is set to 10 GHz and

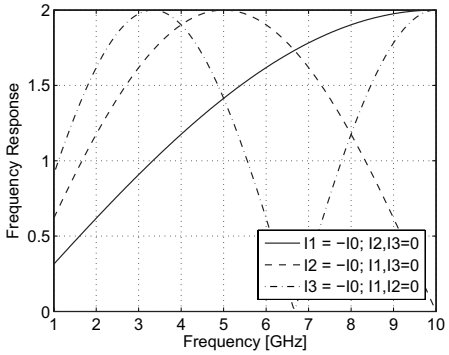

Fig. 2. Simulated frequency response of the idealized FIR-filter applying a clock-frequency of 10 GHz and setting the tap-currents $I_{\{1,2,3\}}$ to the negative of I_0.

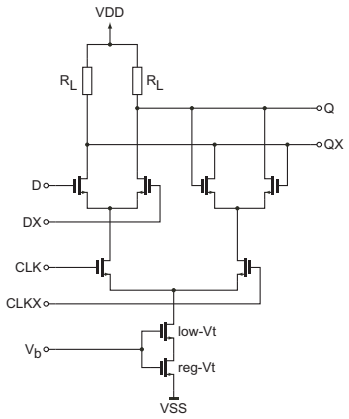

Fig. 3. State of the art D-Latch. All transistors in the core are low-V_t NMOS devices. The stacked current source consists of a low-V_t and a regular-V_t transistor [9].

tap-currents $I_{\{1,2,3\}}$ are set to $-I_0$. Full-rate design gives a data-rate of 10 Gb/s for 10 GHz clock with corresponding high spectral density at 5 GHz. First graph with $I_1 = -I_0$ gives a differentiator behavior over the whole signal spectrum with a very good emphasis of high-frequency parts. Setting $I_2 = -I_0$ gives the frequency response of a single tap, symbol spaced FIR-filter with a peak at 5 GHz. The last tap is introduced to compensate losses at lower frequencies.

The transmitter uses differential pair drivers with open drain output for summation. All drivers are working on the same 70 Ohm load. A 70 Ohm load is chosen as a trade off between matching and output voltage swing in a 50 Ohm system. First tap driver (see Fig. 1) is designed for a maximum current I_0 of 15 mA. This results in a maximum output voltage swing of 450 mV_{pp} single ended on an external 50 Ohm load. Remaining tap-drivers are designed for a maximum current $I_{\{1,2,3\}}$ of 8 mA. All driver currents are defined by their current source bias voltage V_{Ci} and can be externally adjusted. The FIR tap coefficients C_i are obtained by normalizing currents I_i with respect to the current of the main driver I_0 by $C_i = -I_i/I_0$. Negative tap coefficients are realized by inverting buffers.

In figure 3 the D-type latch is shown. All transistors used in the core are low-V_t NMOS devices with minimal gate length. Differential pairs in the data path have 3/5 the width of the clock transistors. These larger clock devices increase input sensitivity and help to manage the available voltage budget [9]. The simulated internal voltage swing is typically two times 600 mV_{pp}.

The current source in figure 3 consists of two stacked NMOS devices. The transistor on top of the stack is a low-V_t type, the other on the bottom a regular-V_t. This stacked configuration results in high output resistance and consequently in a flat current source characteristic above 300 mV drain voltage. The stacked design is preferred, because of the bad DC-characteristic of short channel devices.

III. Receiver Circuit Design

Figure 4 shows the block diagram of the receiver. The input signal is terminated by on chip resistors with 50 Ohm and split up into two paths.

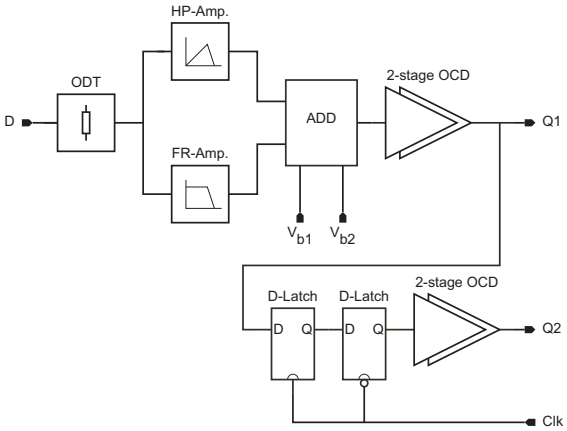

Fig. 4. Receiver block diagram. High-pass amplifier, flat-response amplifier and adder build the adjustable equalizer. D-Latches are used as differential slicers.

A high frequency path to emphasize high frequency parts of the signal spectrum and a flat-response path for the entire signal spectrum. Both signals are recombined at the adder and weighted according V_{b1} and V_{b2}.

A two stage off chip buffer drives the first output Q1. This output is implemented for equalizer characterization. The output signal also feeds the differential slicer built by a master-slave flip-flop. Feeding the signal from the output driver to the slicer is not the optimum solution. Nevertheless this configuration is chosen to characterize the slicer on the same chip as well.

The circuit of the high-frequency path is shown in figure 5. The first stage uses capacitive source degeneration to achieve high-pass characteristics.

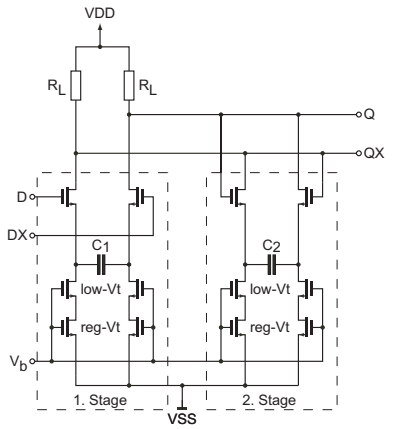

Fig. 5. High-pass amplifier circuit. The first stage uses capacitive source degeneration to achieve high-pass characteristics. The second is an active peaking circuit.

The second stage is an active peaking circuit. The cross coupled differential pair and the capacitance provide an inductive behavior. This peaked amplifier is designed without using passive inductors consuming a lot of chip area.

The flat-response amplifier in figure 4 is designed for a maximum cut-off frequency and provides a gain of 10 dB to increase sensitivity. The adder consists of two CML-pairs working on the same load. The current of each pair is defined by external bias-voltages. The used D-Latches are already described in the previous section (see figure. 3).

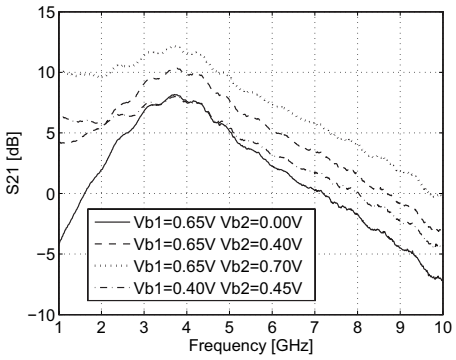

Fig. 6. Measured small-signal frequency response of the equalizer circuit. V_{b1} controls the high-frequency path and V_{b2} the flat-response path.

The measured small-signal frequency response is shown in figure 6. V_{b1} controls the high-frequency path and V_{b2} the flat-response path. Measurements show a peak at 3.8 GHz. Presented bias-voltage configurations show good emphasis of high-frequency parts. The ripple in the measurements are introduced by the bias-tees in the measurement setup.

IV. Experimental Results

Figure 7 shows the chip micrograph of the transmitter a) and receiver b). Both have a chip area of 470 x 640 μm^2.

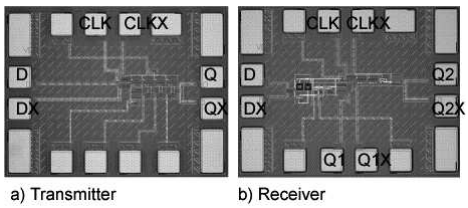

Fig. 7. Chip Micrograph of the transmitter a) and the receiver b).

To evaluate the circuit performance the chips are bonded on 30x30 mm^2 0.51 mm RO4003 microwave substrate (ε_r = 3.38) with SMA connectors for input and output signals.

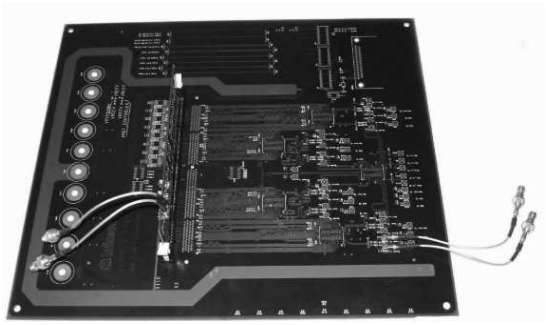

Fig. 8. Motherboard test channel including the motherboard, a DIMM-Connector and a DIMM.

Measurements are performed with two different channels, two five meter long RG58 cables connected to the test fixtures with BNC-SMA connectors and a conventional designed, differential motherboard channel. Figure 8 shows the motherboard test assembling. The channel consists of a 18 cm long differential line, a DIMM-connector and a DIMM with an additional 4 cm line. All lines are designed like state of the art memory interconnects with a line width of 127 μm. MMCX-connectors are used for data input and output. SMA-MMCX connectors and 10 cm long MMCX-cables allow connecting the test fixtures.

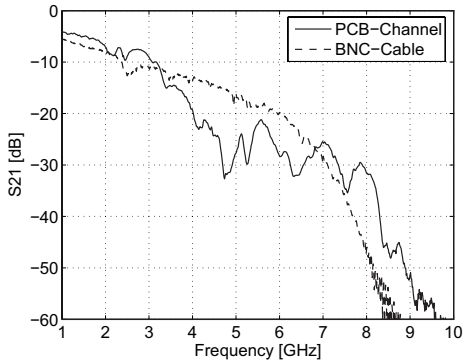

Fig. 9. Measured frequency response of the test channels. Each channel show high damping. Additionally the PCB-channel suffers from strong non-linear phase-distortion.

Figure 9 shows the test channels frequency response. Each of them show high damping and the PCB-channel suffers from strong non-linear phase-distortion.

BER-measurements are performed with a PRBS-11 generator and the Anritsu MP1764A error detector. Signal shapes are measured with Agilents sampling scope Infiniium DCA 86100B with the 83484A two channel module.

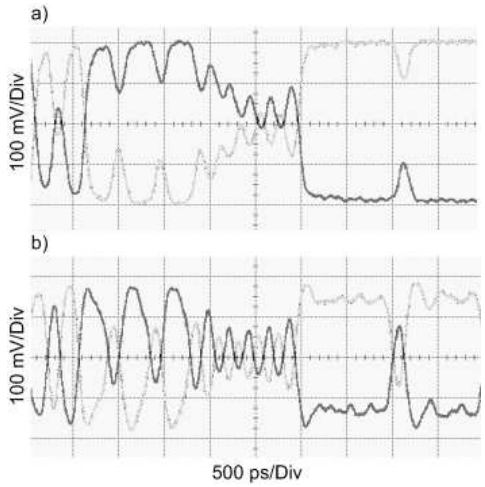

Fig. 10. Measured equalizer output Q1 with a 9 Gb/s data pattern over the motherboard channel a) without and b) with pre-distortion and equalization.

Figure 10 shows a 9 Gb/s data pattern at the equalizer output Q1 for the motherboard channel. Fig. 10(b) shows the data pattern with pre-distortion and equalization and Fig. 10(a) without both. This signal is applied to the slicer and gives a BER $< 10^{-12}$. Note that the damping at the corresponding Nyquist-frequency is 24.3 dB (4.5 GHz). Error free transmission of higher data rates is not possible for this channel because of strong phase-distortion above 4.5 GHz (see Fig. 9).

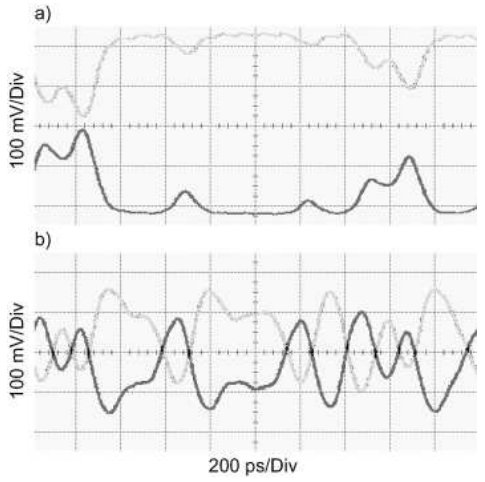

Fig. 11. Measured equalizer output Q1 with a 11 Gb/s data pattern over 5m RG58 cable a) without and b) with pre-distortion and equalization

Figure 11 shows a 11 Gb/s data pattern for the 5 m long BNC-cable channel, with pre-distortion and equalization (b) and without both (a). This signal is applied to the slicer and gives a BER $< 10^{-12}$. Damping at corresponding Nyquist-frequency is 18.8 dB (5.5 GHz).

At both measurements the tail current of the last tap of the FIR-filter was set to zero. This enables a reduction of total FIR tap-size to 2 resulting in a total delay time of 1 UI.

Data rates	10 Gb/s
Supply voltage	1.5 V
Supply current	120 mA
Chip size	2 x 470 x 640 μm^2
Technology	0.13 μm Bulk CMOS

TABLE I
TECHNICAL DATA

V. CONCLUSION

A transmitter and receiver circuit in 0.13 μm CMOS is presented allowing 10 Gb/s error-free data transmission over legacy copper channels without using inductors. An unconventional FIR-filter design allows to compensate channel losses with only two taps and a total delay of 1 UI. Measurements are presented with BER $< 10^{-12}$ at 9 Gb/s over a conventional motherboard channel with 24.3 dB damping at 4.5 GHz and 11 Gb/s over a 5 m long RG58 cable with 18.8 dB damping at 5.5 GHz.

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