A 24-Gb/s $2^7 - 1$ Pseudo Random Bit Sequence Generator IC in 0.13 μm Bulk CMOS

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***Abstract*— This work presents a 24 Gb/s pseudo random bit sequence (PRBS) generator with a sequence length of $2^7 - 1$. The circuit uses an interleaved linear feedback shift register and multiplexing architecture. An output voltage swing of 280 mVpp is achieved for 24 Gb/s data rate and 390 mVpp for 10 Gb/s. The circuit features a trigger output which allows to trigger the eye or the sequence pattern. The circuit is manufactured in 0.13 μm bulk CMOS technology and draws 183 mA at 1.5 V supply voltage.**

I. Introduction

Pseudo random bit sequences (PRBS) are needed as test signals for all kinds of digital circuits and systems in the field of digital data communication. Testing of fundamental building blocks such as multiplexers, de-multiplexers, flip-flops or digital broadband amplifiers as well as whole communication systems from fibre optics to backplane communication depends on suitable test signal sources.

PRBS generators are mostly based on linear feedback shift registers. The length of the shift register defines the maximum length of the generated sequence. A shift register of the length L has a maximum sequence length of $2^L - 1$. PRBS generators of different length are used for different requirements whereas short sequences as $2^7 - 1$ are typically used for basic tests and longer sequences for bit error tests. The feedback path of the shift register is the second part defining sequence characteristics. Sequences with maximum length are denoted maximum length sequences (m-sequences) and have balanced amplitude characteristic. There is only one 1 more than 0s in a sequence. An additional useful property of a m-sequence is its autocorrelation function approximating the dirac impulse which results in a flat power density spectrum and make m-sequences to an important part in spread spectrum systems.

Fast pseudo random sequences are obtained by multiplexing slower pseudo random data patterns using special multiplexing techniques [1] [2] [3]. In this work a 2:1 multiplexer architecture is used to reduce the bit rate of the shift-register core to the half of the output bit rate. The multiplexer is feed with two appropriate time shifted bit sequences tapped from the shift-register core. PRBS generators using this architecture have been presented in 0.18 μm SiGe technology using 2:1 multiplexing techniques for bit rates from 40 Gb/s up to 100 Gb/s in [4] [5] and in BiCMOS technology using a 4:1 multiplexing technique for 80 Gb/s [6]. The PRBS architecture used in this work is based on an interleaved linear feedback registers presented in a 40 GHz AlGaAs/GaAs technology for bit rates up to 21 Gb/s [7].

In the past multi-gigabit data communication IO-circuits had to be designed in bipolar technology. Recent works [8] [9] demonstrate digital CMOS receiver and transmitter circuits working at data rates in the 10 Gb/s range and above. Integrated testing routines show the need of fast PRBS generators realized in CMOS technology.

A full rate $2^7 - 1$ PRBS generator for bit rates up to 13 Gb/s in 0.13 μm CMOS technology was recently presented in [10]. Maximum bit rates achievable in CMOS are by a factor of 4 lower than in state of the art bipolar technologies nevertheless a CMOS implementation has a very important benefit and that is its integration ability into existing CMOS data communication circuits.

II. PRBS Architecture

To achieve maximum data rates a multiplexing PRBS generator architecture was chosen allowing the shift register core to work at half the frequency compared to full rate PRBS generators.

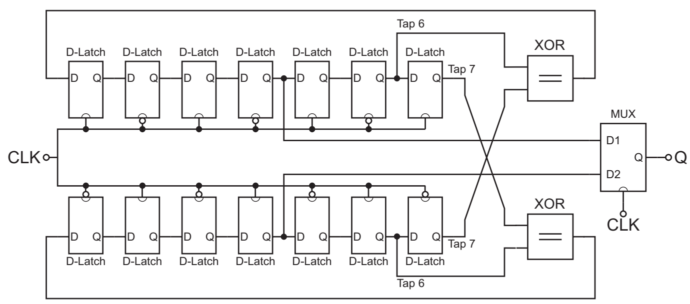

Fig. 1. Block diagram of the PRBS core realized with interleaved shift registers. The multiplexing architecture reduces the shift register data rate to the half of the output data rate.

Figure 1 shows the block diagram of the PRBS generator core. For a PRBS of length $2^7 - 1$ seven shift registers are needed. One shift register is realized as D-type flip flop consisting of two D-type latches. Here the shift registers are split into two groups containing seven D-type latches. The two opposite shift register groups have to be clocked with inverted clock signals. The feedback is realized by an XOR-gate working as modulus 2 adder. The inputs of the XOR-gate are taken from tap 6 and tap 7. Unlike conventional shift register design, feedback taps are defined between D-latches and not between D-flip flops. Second difference is the interleaved structure. The feedback signal is build from tap 6 of one shift register and tap 7 of the opposite shift register. The output sequence is build by the multiplexer feeded with two opposite signals. This allows the shift register core to work at half the bit rate of the output pattern. This architecture produces a m-sequence of length $2^7 - 1$ according to the characteristic polynomial $x^7 + x^6 + 1$.

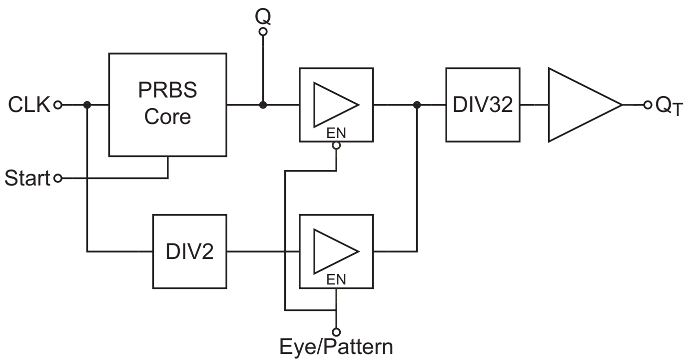

Fig. 2. Block diagram of the full PRBS generator including the eye/pattern trigger output.

Figure 2 shows the block diagram of the full PRBS-generator implementation including the eye/pattern trigger output. The PRBS-core shown in figure 1 has an external start-input to reset the shift register in the all zero case. An external eye/pattern input signal switches the trigger output between eye and pattern mode. Trigger signals in both cases are generated by a 32:1 frequency divider. Switching between the two modes is done by enabling or disabling the buffers feeding the divider. A $2^7 - 1$ m-sequence has 32 transition from 1 to 0 and vice versa. Dividing the sequence through 32 leads to a trigger signal with the same period as the sequence. The 32:1 frequency divider is realized with five, sequential 2:1 frequency dividers realized with feed back D-flip flops [11]. An additional 2:1 frequency divider is introduced in the eye path to achieve a further decrease of the trigger output frequency in eye mode.

III. Circuit Design

All high speed circuits in this work are designed in current mode logic (CML) allowing fully differential design, faster switching and higher supply noise suppression.

All cells (D-Latch, MUX, DIV2) driven from the external clock signal contain a source follower which is shown in the latch circuit diagram in figure 3. The source follower is introduced to reduce capacitive load at the clock input and provides appropriate clock DC values.

The used current source consists of two stacked NMOS devices (see figure 3). The transistor on top of the stack is a low-V_t type, the other on the bottom a regular-V_t. This stacked configuration results in high output resistance and consequently in a flat current source characteristic above 300 mV drain voltage. The stacked design is preferred, because of the high slope in short channel devices DC-output characteristics.

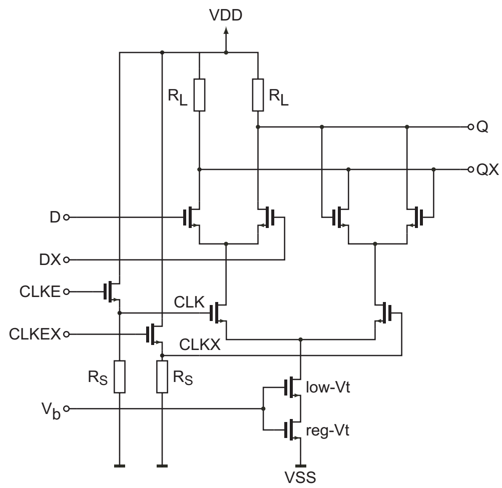

Fig. 3. State of the art D-Latch. All transistors in the core are low-V_t NMOS devices. The stacked current source consists of a low-V_t and a regular-V_t transistor.

In figure 3 the D-type latch is shown. All transistors used in the core are low-V_t NMOS devices with minimal gate length. Differential pairs in the data path have 3/5 the width of the clock transistors. These larger clock devices increase input sensitivity and help to manage the available voltage budget. The simulated internal voltage swing is typically two times $600\,\text{mV}_{pp}$.

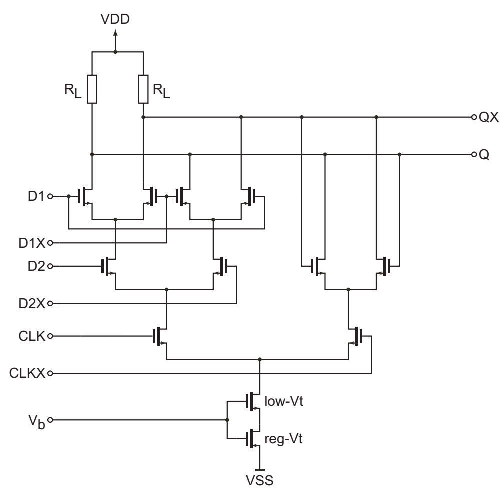

Fig. 4. CML XOR gate including a D-Latch. All transistors in the core are low-V_t NMOS devices.

Figure 4 shows the XOR gate for linear feedback of the shift register which is included in the first latch of the shift register. Instead of a differential pair the XOR gate is introduced at the transparent side of the latch. This design allows to save one cell. Five stacked transistors at low CMOS supply voltage results in a very low voltage headroom for each transistor and a slower cell. Nevertheless this design is much faster than a design with separated XOR and latch circuits. The XOR gate in figure 4 is realized with minimum gate length, low-V_t transistors. It draws current from the left load resistor R_L and sets the output low if the input signal D1 and D2 are equal and high if they are different.

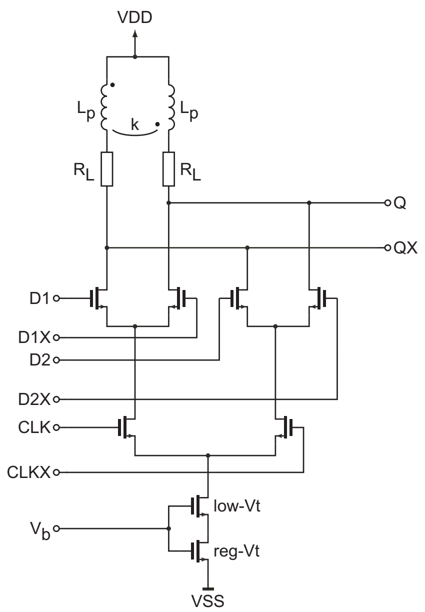

Fig. 5. Schematic diagram of the 2:1 multiplexer with inductive peaking applied to increase bandwidth[12].

Figure 5 shows the schematic diagram of the multiplexer. Transistors in the core are realized as low-V_t transistors with minimum gate length. The multiplexer load consists of $70\,\Omega$ resistors and coupled peaking coils. The multiplexer output directly feeds the chip output and the external load to avoid additional band limiting output buffers. The $70\,\Omega$ load resistors result in a good trade off between output voltage swing and matching of a $50\,\Omega$ external load. The multiplexer current source draws 8 mA which results in a differential output swing of 470 mVpp.

A. Shunt Peaking Design

To increase the multiplexer bandwidth inductive shunt peaking is applied. A symmetrical inductance is introduced in the drain path. The center tap of the symmetrical inductance is connected to VDD and the inductance is connected to the differential load resistors. This results in two coupled inductances connected to the multiplexer drain paths with an inductance of $L_p = 0.26\,nH$ and a coupling coefficient $k = 0.67$. Differential design leads to an effective inductance seen at each side of $L_{eff} = L_p(1 + k)$.

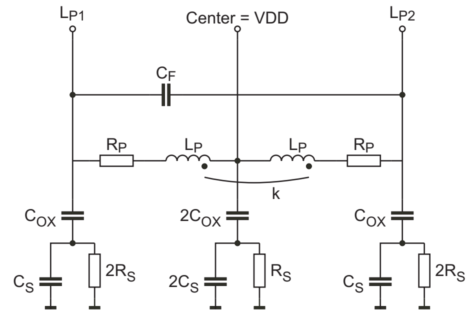

Fig. 6. Equivalent circuit of the shunt peaking inductances. This inductance model including parasitics [13] is used for circuit simulation.

Figure 6 shows the equivalent circuit [13] of the symmetric shunt peaking inductor used in circuit simulation. The series resistance is denoted by R_p, the interwinding capacitance is modeled by C_F. The capacitance from the inductance to the substrate is denoted by C_{OX} and the substrate itself is modeled by C_S and R_S.

IV. Measurement Results

Figure 7 shows the chip micrograph of the PRBS generator. The three boxes are showing the PRBS-core (a), the peaked MUX (b) and the frequency dividers for the trigger output (c). The PRBS generator has a total chip area of $630 \times 470\,\mu\text{m}^2$.

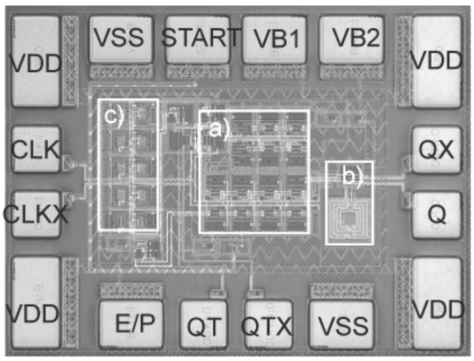

Fig. 7. Chip micrograph of the PRBS generator showing the PRBS-core (a), the peaked MUX (b) and the frequency dividers for the trigger output (c).

The PRBS generator is design for negative supply voltage and draws 183 mA from a -1.5 V voltage source. To evaluate the circuit performance the chip is bonded on a 30x30 mm^2 0.51 mm RO4003 microwave substrate ($\varepsilon_r = 3.38$) which is connected with SMA connectors for input and output signals. Measurement results show the performance of the PRBS generator circuit including the loss caused by the bond wires, microstrip lines and SMA connectors on the test board. The differential clock signal was generated by a 180 hybrid coupler. Output signals are measured with Agilents sampling scope Infiniium DCA 86100B using the 83484A two channel module.

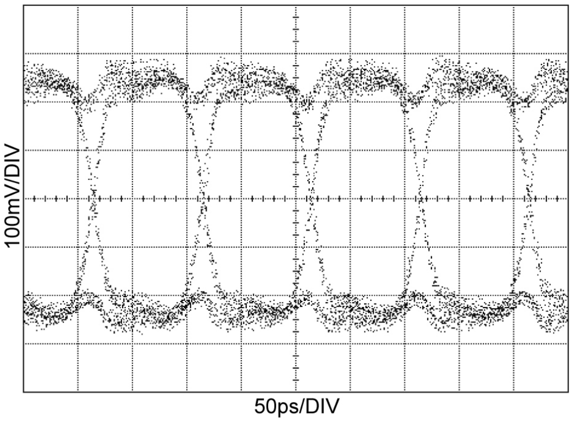

Fig. 8. Measured differential eye diagram of the PRBS-output at a data rate of 10 Gb/s.

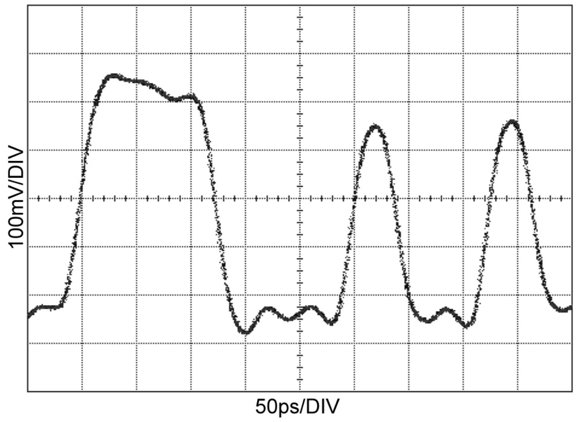

Fig. 10. Measured differential PRBS-output pattern at a data rate of 24 Gb/s.

Figure 8 shows the differential eye diagram of the sequence output signal at a data rate of 10 Gb/s. At this output data rate the input clock frequency is 5 GHz. The minimum vertical eye opening is 390 mVpp.

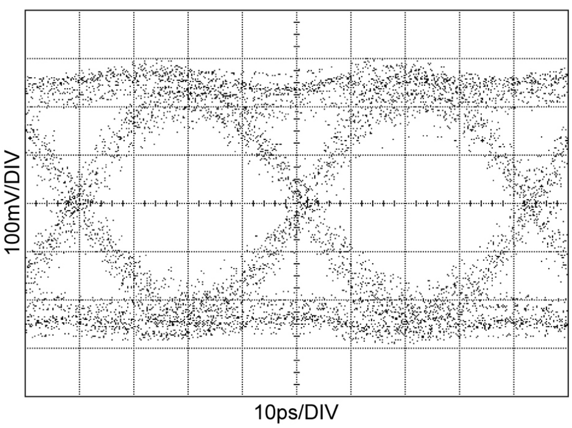

Fig. 9. Measured differential PRBS-output at a data rate of 24 Gb/s.

The PRBS generator works up to a clock frequency of 12 GHz resulting in a data rate of 24 Gb/s. Figure 9 shows the differential eye diagram and figure 10 the sequence pattern. The minimum vertical eye opening at a data rate of 24 Gb/s is 280 mVpp. Eye diagram and sequence patterns are measured using the build in trigger output.

V. Conclusion

In this work a $2^7 - 1$ PRBS generator IC, working at data rates up to 24 Gb/s in standard 0.13 μm bulk CMOS is presented. High output voltage swings of 390 mVpp and 280 mVpp are achieved at date rates of 10 Gb/s and 24 Gb/s respectively. The circuit also features a trigger output for eye and sequence triggering. The integrate circuits draws 183 mA from a negative 1.5 V power supply.

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