



The simulated noise figure of the LNA is 6.5 dB in the frequency range from 75 GHz to 86 GHz. Interstage matching is accomplished by an LC matching network ( $T_2$ ,  $C_3$ ). Here, the inductance is replaced by a transmission line that is shorted for high frequencies. The transformed input impedance of the following stage determines the load impedance (the gain) of the CE transistor  $Q_1$ . The output of the LNA is matched with transmission lines to a  $50\ \Omega$  interface, including the parasitic pad capacitance. The simulated gain of the LNA at 79 GHz is 16 dB. The LNA consumes 32 mA.

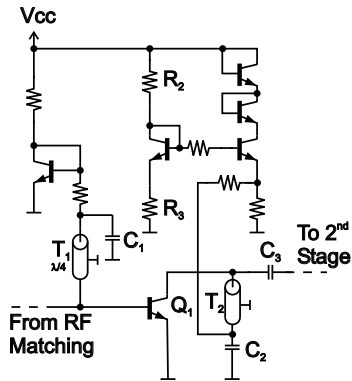


Fig. 2. One stage of the low-noise amplifier.

The power splitting of the RF signal is done as follows: Two transmission lines of  $220\ \mu\text{m}$  length transform the input impedance of both RF baluns to a low impedance. This value is transformed to the  $50\ \Omega$  interface by a serial transmission line and a shunt capacitor.

The RF and the LO baluns are LC-baluns where the inductors are replaced with transmission lines [7]. With this type of balun, a single-ended to differential conversion and impedance matching is achieved simultaneously. The insertion loss of one balun is 1.6 dB.

The direct conversion mixers are based on the high level mixer presented in [8], but without any degeneration at the lower differential pair. The switching behavior of the four upper transistors in the Gilbert cell has a large influence on the noise figure of the mixer. Thus, the current density in the switching quad is chosen to result in maximum  $f_T$ , i.e.,  $5\ \text{mA}/\mu\text{m}^2$ . The amplified thermal noise of the base resistances in the lower differential pair degrades the overall noise figure. Therefore transistors with bases consisting of two fingers and large emitter sizes are chosen. Current mirrors provide the bias current for the mixers. The bias networks at the LO port as well as at the RF port consist of level shifting diodes and resistors.  $500\ \Omega$  resistors decouple the biasing from the signal path. The mixer is designed for high impedance external loads, so the internal load of  $2 \times 400\ \Omega$  and the bias current of 6 mA determine the conversion gain. The simulated noise figure of one mixer is 12 dB, and the conversion gain is 24 dB. The current consumption of one mixer, including biasing, is 11 mA.

To maintain a high voltage swing at the LO port of the mixer, which is essential for good noise performance, the LO signal is applied to the four switching transistors via an LO

buffer. This buffer is depicted in Figure 3. The load of the differential pair  $Q_{1,2}$  is formed by an LC circuit in a parallel resonator configuration. The shorted transmission lines  $T_{1,2}$  replace the inductors, and the capacitors are the transformed ( $T_{3,4}$ ) input impedances of the emitter followers  $Q_{3-6}$  and the parasitic capacitances at the collectors of the differential pair  $Q_{1,2}$ . The simulated gain of the buffer as shown in Figure 3 is 10 dB in the frequency range around 80 GHz. The buffers consume 60 mA each.

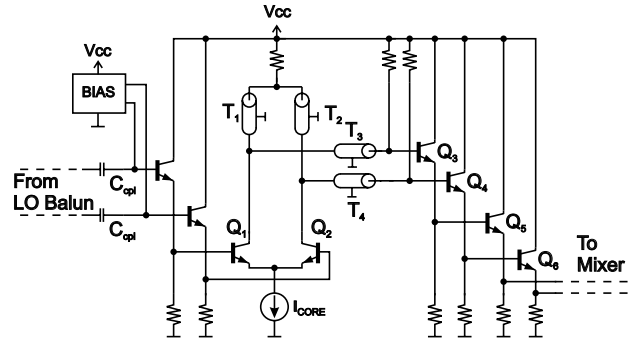


Fig. 3. LO buffer amplifier.

The  $0^\circ/90^\circ$  phase shift between the two IF output ports is achieved by the use of a branchline coupler at the LO port of the mixer. The coupler is designed using an electrical model, consisting of the damping factor and the effective permittivity of the transmission lines at the operation frequency. The isolated port is terminated with  $50\ \Omega$ . Transmission lines match the input impedance of the coupler to  $50\ \Omega$  parallel to the parasitic pad capacitance. Effects of corners and tee-junctions are neglected. The four branches have a length of  $480\ \mu\text{m}$  each, which equals  $\lambda/4$  at 80 GHz.

### III. TECHNOLOGY

The frontend was implemented in an advanced 200 GHz  $f_T$  SiGe:C bipolar technology, based on the technology presented in [2]. The maximum oscillation frequency  $f_{\text{max}}$  of the transistors is 275 GHz. Shallow and deep trench isolation are used. The transistors are fabricated with a double-polysilicon self-aligned emitter base configuration with a SiGe:C base. This base is integrated by selective epitaxial growth. The transistors have a minimum emitter mask width of  $0.35\ \mu\text{m}$ , resulting in an effective emitter width of  $0.18\ \mu\text{m}$ . The technology additionally features high-voltage transistors with a  $BV_{CEO}$  of 5.0 V [9]. Four metal layers, MIM-capacitors, varactors, and different types of resistors are also included.

Transmission lines are essential components in millimeter wave circuits, making their accurate modeling mandatory. A 2D field simulator is used to model the transmission lines, as described in [10]. The transmission lines are implemented with metal layer M4 over metal layer M2. A  $5\ \mu\text{m}$  wide metal M4 signal path over a metal M2 ground path yields a  $50\ \Omega$  transmission line. The maximum width of metal M2 is limited to  $15\ \mu\text{m}$ . Therefore, a cheesed structure is used to expand the ground plane. Simulations show that the transmission lines have a loss of 1 dB per millimeter and an effective dielectric

constant of 3.83 at 80 GHz. The  $35\ \Omega$  transmission lines of the branchline coupler exhibit a loss of 0.86 dB per millimeter at the same frequency.

#### IV. EXPERIMENTAL RESULTS

A die photograph of the fabricated I/Q frontend is shown in Figure 4. The left hand side of the chip is occupied by the I/Q mixer, while the LNA covers the right hand side.

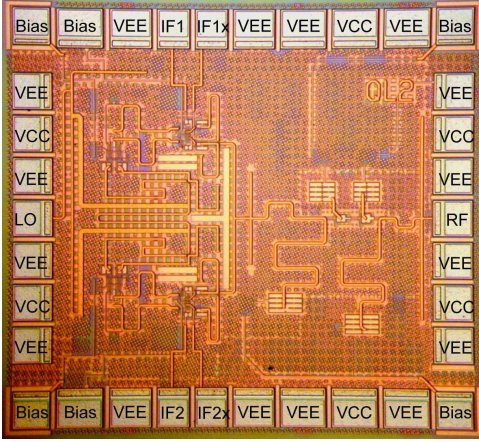


Fig. 4. Die photograph of the frontend. Die size is  $1100\ \mu\text{m} \times 1000\ \mu\text{m}$ .

All measurements were done on-wafer with probes. The temperature was kept at a constant level of  $25^\circ\text{C}$ . The LO power level was set to +1 dBm on-chip. The mixers are designed for high impedance external loads, thus external voltage followers with an input impedance of 100 k $\Omega$  were attached to the output of the mixers. This provides matching to the  $50\ \Omega$  measurement environment. The differential IF signal was combined with a  $180^\circ$  low-frequency hybrid. The voltage followers limit the IF measurement range to an upper frequency of 30 MHz. All off-chip losses from the test setup were de-embedded from the measurement results.

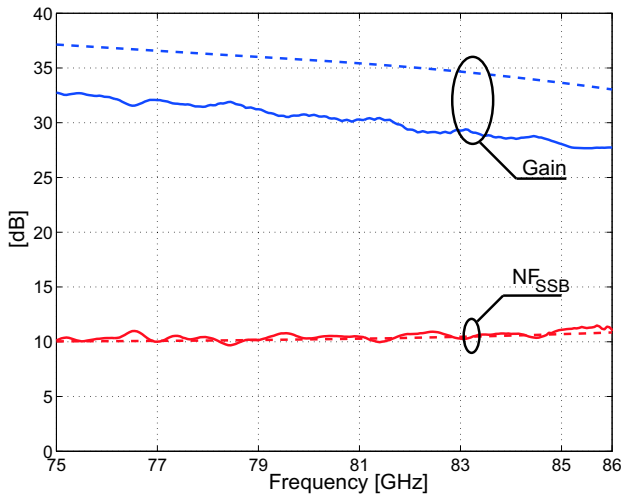


Fig. 5. Measured (solid lines) and simulated (dashed lines) single sideband noise figure and conversion gain of the frontend (IF = 10 MHz).

The noise figure was measured using HP's 8970B noise figure meter, which limits the lower IF range to 10 MHz. The

single sideband (SSB) noise figure and the conversion gain are depicted in Figure 5. This plot also shows a comparison with the simulated results. While the noise figure matches simulations (11 dB), the gain deviates by 5 dB over the whole frequency range. Additional measurements show that the gain of the LNA differs from the simulation by 4 dB.

The  $90^\circ$  phase shift of the in phase and the quadrature output is a crucial parameter for the performance of communication as well as precision sensor systems. This parameter was measured using a frequency counter with phase measurement capability (HP 53132A). The result is shown in Figure 6, along with the simulated phase difference. The measured results are in good agreement with the simulations.

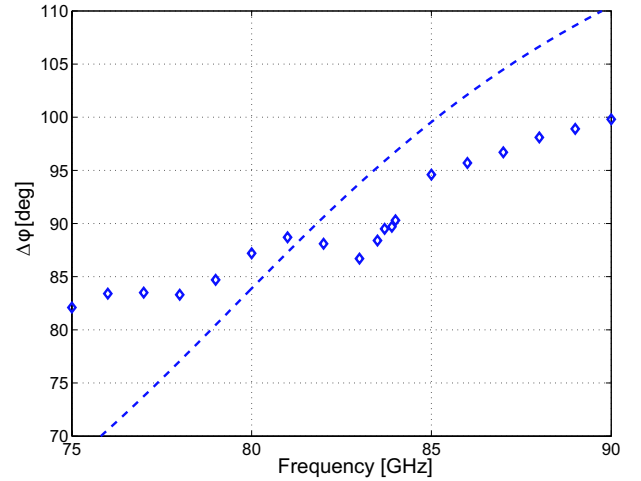


Fig. 6. Measured mean phase difference and simulated (dashed lines) phase difference of the IF outputs (IF = 10 MHz, 500 averages).

The relative phase difference from  $90^\circ$  is within  $\pm 8^\circ$  from 75 GHz to 88 GHz. Figure 7 shows the conversion gain and noise figure imbalance of the two mixer outputs. The gain differs by less than 0.7 dB. The difference in noise figure is negligible.

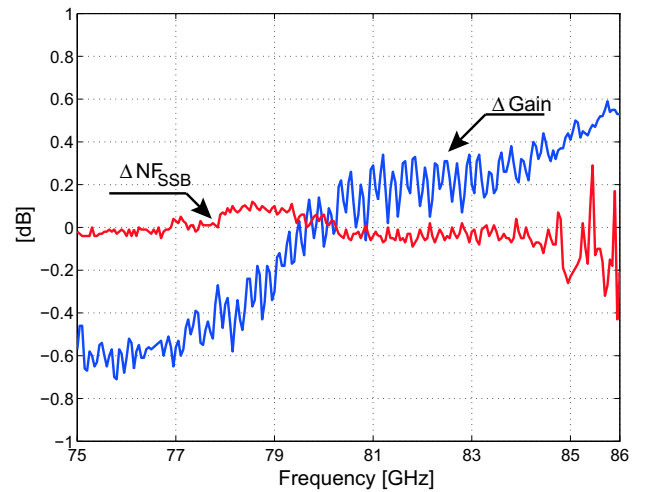


Fig. 7. Measured gain and noise figure imbalance of the two output ports (IF = 10 MHz).

The plot of the differential IF output voltage versus RF input power is shown in Figure 8. Due to the external high impedance load of the mixer, the output voltage is depicted instead of the output power. The input-referred 1 dB compression point is -16 dBm. The differential saturated output voltage is  $13 \text{ dBV}_{\text{pp}}$ , which is equal to a linear differential output voltage of  $4.47 \text{ V}_{\text{pp}}$ . The 1 dB compression point instead of the third-order intercept point is taken as a figure of merit for the usability of this frontend in data communication systems due to the lack of a third RF source for the two tone measurement setup.

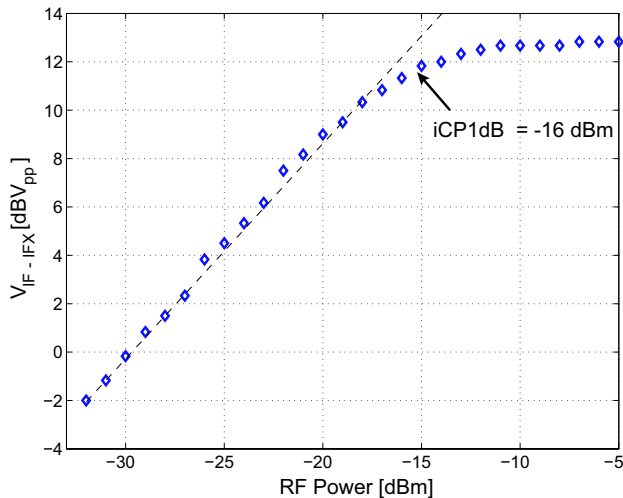


Fig. 8. Differential IF output voltage versus input power at 79 GHz (IF = 10 MHz).

The RF and LO port matching were measured using millimeter-wave probes and a 110 GHz network analyzer from Agilent. The results are shown in Figure 9. The RF port has a return loss larger than 10 dB in the frequency range from 75 GHz to 89 GHz. The return loss of the LO port is larger than 10 dB in the frequency range from 50 GHz to 90 GHz. These results show very good agreement with the simulations, as indicated in Figure 9. The measured LO to RF isolation is better than 35 dB from DC to 110 GHz.

## V. CONCLUSION

An I/Q receiver frontend for sensing and communication purposes was designed, fabricated in a SiGe:C bipolar technology, and characterized. The frontend features a conversion gain of more than 28 dB and a noise figure of 11 dB over a frequency range from 75 GHz to 86 GHz. The two IF outputs are in quadrature at a frequency of 84 GHz, and they are within  $8^\circ$  out of quadrature from 75 GHz to 88 GHz. The gain imbalance between these outputs is smaller than 0.7 dB, and the imbalance in noise figure is smaller than 0.4 dB. The input-referred 1 dB compression point is -16 dBm.

The performance of this frontend indicates its suitability for communication systems in the frequency range from 81 GHz to 86 GHz, or for precision sensing applications around 79 GHz. From the technology point of view, the obtained

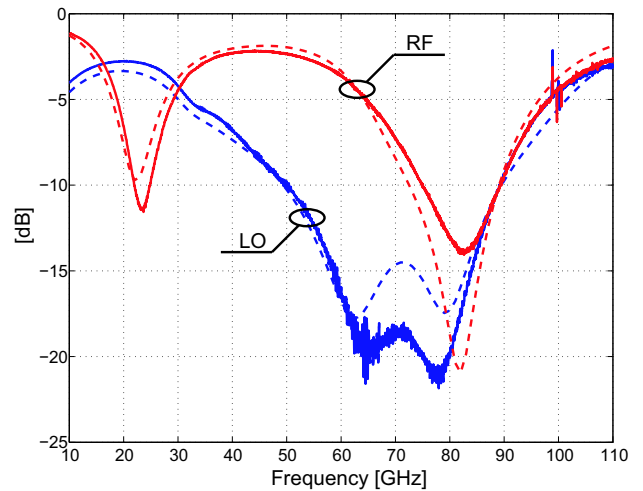


Fig. 9. Measured (solid lines) and simulated (dashed lines) LO and RF port matching of the frontend.

results show that very high integration levels in millimeter-wave frequency ranges are feasible in SiGe.

## VI. ACKNOWLEDGEMENT

The authors thank Infineon's technology team for the chip fabrication. This work was partly supported by the German Bundesministerium für Bildung und Forschung (BMBF) under contract 10 M3161A (KOKON).

## REFERENCES

- [1] K. Strohm et al., "Development of Future Short Range Radar Technology," in *European Microwave Week, EUMA*. EUMW Technical Digest, October 2005, pp. 165 – 168.
- [2] J. Böck et al., "SiGe Bipolar Technology for Automotive Radar Applications," in *Bipolar/BiCMOS Circuits and Technology, 2004. Proceedings of the 2004 Meeting*. IEEE, December 2004, pp. 84–87.
- [3] H. Rücker et al., "SiGe:C BiCMOS technology with 3.6 ps gate delay," in *Electron Devices Meeting, IEEE*. IEDM Technical Digest, December 2003, pp. 5.3.1– 5.3.4.
- [4] B. Floyd et al., "SiGe bipolar transceiver circuits operating at 60 GHz," *Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 156 – 167, January 2005.
- [5] M. Kaleja et al., "An I-Q Mixer at 76.5 GHz using flip-chip mounted silicon Schottky Diodes," in *Microwave Symposium Digest*, vol. 3. IEEE, 2001, pp. 1653–1656.
- [6] B. Dehlink et al., "A low-noise amplifier at 77 GHz in SiGe:C bipolar technology," in *Compound Semiconductor Integrated Circuit (CSIC) Symposium*. Palm Springs, USA: IEEE, Oct – Nov 2005, pp. 287–290.
- [7] W. Bakalski et al., "Lumped and distributed lattice-type LC-baluns," *Microwave Symposium Digest*, vol. 1, pp. 209–212, 2002.
- [8] H. Wohlmut and W. Simbürger, "A high IP3 RF Receiver Chip Set for Mobile Radio Base Stations up to 2 GHz," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 7, pp. 1132–7, July 2001.
- [9] R. Vytla et al., "Simultaneous Integration of SiGe High Speed Transistors and High Voltage Transistors," in *Accepted for Presentation at Bipolar / BiCMOS Circuits and Technology Meeting*. IEEE, October 2006.
- [10] D. Kehrer et al., "Prospects of Microstrip Waveguides in Aluminum and Copper Metallization for High-Frequency Applications," *Journal of the Brazilian Telecommunications Society*, vol. 18, no. 1, pp. 1–9, August 2003.