A Fundamental VCO with Integrated Output Buffer beyond 120 GHz in SiGe Bipolar Technology

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***Abstract* — A fundamental voltage controlled oscillator (VCO) beyond 120 GHz is presented. The VCO has been extended by a cascode amplifier as an output buffer. The chip is fabricated in a 200 GHz f_T SiGe bipolar technology. The VCO shows a tuning range from 117.5 to 121.5 GHz. A phase noise of -93.3 dBc/Hz at 1 MHz offset frequency was measured. The circuit consumes 310 mA from a -6 V supply. The high oscillation frequency with low phase noise performance, to the best authors' knowledge, are record values for fully integrated fundamental voltage controlled oscillators in SiGe technology.**

***Index Terms* — SiGe, voltage controlled oscillator, VCO, millimeter-wave circuits, heterojunction bipolar transistor.**

I. Introduction

Millimeter-wave voltage controlled oscillators (VCOs) play an important role in advanced communication systems and radar sensors. Recently different circuits in SiGe technology targeting the 122 GHz ISM frequency band have been presented. In [1] a fundamental VCO up to 112 GHz and a 122 GHz mixer have been reported. A static divider up to 110 GHz and a dynamic divider by four up to 160 GHz have been demonstrated in [2] and [3], respectively. Moreover, it has been shown that VCOs can be used to test and compare technologies in terms of speed and noise performance [4].

In this paper we present a fully differential fundamental voltage controlled oscillator beyond 120 GHz. The oscillator core is of the negative-resistance type. The circuit includes also an output buffer to achieve high output power.

II. Circuit Design

A fully differential configuration has been chosen due to the advantages compared to single-ended operation, as presented in [5]. The circuit consists of a VCO-core, an emitter follower pair and an output buffer stage. The VCO-core is based on the topology presented in [5], a common collector Colpitts, with some modifications.

According to the Leeson's formula, in order to reduce the phase noise in the VCO an increase of the voltage swing in the resonator is needed. This effect can be achieved by increasing the collector current and, thus, using larger transistors which lower the maximum oscillation frequency due to the larger parasitic capacitances. In our design the resonator has been designed to reduce this drawback. L_1 is used to allow to feed the bias current of transistor into a virtual ground node. The differential varactor is connected to the emitter of the transistors T_1 via the transmission lines L_2, as shown in Fig. 1 (due to the symmetry of the circuit only one label is used). The varactor has been chosen very large in order to set the resonance frequency for the varactor-L_2 network in the range of 50 GHz showing an inductive behavior in the frequency range of interest. L_2 reduces the phase noise contribution of the varactor increasing the loaded quality factor. The overall impedance seen by T_1 at its emitter is: $Z_{eq}=j\omega L_1//(j\omega L_2-j/\omega C_{var})$ and its overall inductive behavior is shown in Fig. 2. The effective inductance of Z_{eq} is increased by the increasing of the capacitance of the varactor: Z_{eq} is working like a tuneable inductor. The input impedance, $Z_{in,T1}$, of the large transistor T_1 depends on the load Z_{eq}. The imaginary part $Z_{in,T1}$ is negative and increases with the frequency. The real part of $Z_{in,T1}$ is positive at very low frequency and than becomes negative at higher frequency: the cross point zero can be moved to higher frequency, enabling higher operation frequencies, by increasing the reactance of the load Z_{eq} as demonstrated in [6].

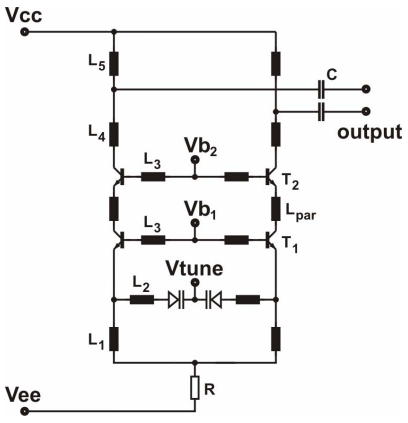

Fig. 1 VCO-core schematic without the output buffer stage. $L_{1\text{-}5}$ are implemented as microstrip-lines, all with inductive behavior. L_{par} models the parasitics of the interconnection line between T_1 and T_2.

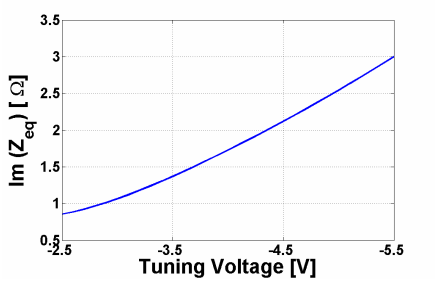

Fig. 2 Simulated behavior of Z_{eq} (the supply voltage is -6 V).

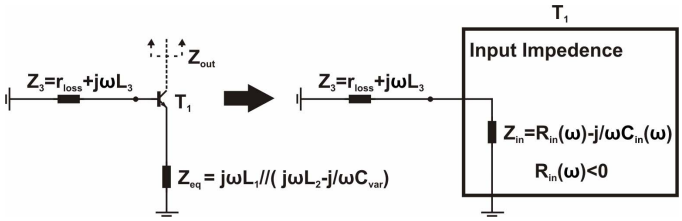

Fig. 3 Simplified one-port model of the oscillator. In the analysis half of the circuit has been considered for symmetry reasons.

Fig. 3 shows the simplified one-port model for the negative resistance oscillator sketched in Fig. 1. The losses in the transmission line L_3 have been taken into account by r_{loss}. The condition for oscillation, at the start-up, is that the negative resistance of the active device compensates for the losses at the oscillation frequency: $r_{loss}+R_{in,T1}(\omega_{osc})<0$. When steady-state oscillation has built up, large-signal effects cause an increase of the negative resistance and the active device exactly compensates the resonator losses, $r_{loss}+R_{in,T1}(\omega_{osc})=0$. The oscillation frequency can be estimated by using the model in Fig. 3:

$$\omega_{osc} \approx \sqrt{\frac{1}{L_3 C_{in}}},$$

where C_{in} is tuned by Z_{eq}. The increase of Z_{eq} results in a lower C_{in} which tunes the VCO to higher frequency. In Fig. 4, the simulated real and imaginary part of $Z_{in,T1}+Z_3$ are plotted. The oscillation conditions for the start-up are satisfied by the zero crossing of the imaginary part $Im(Z_{in,T1}+Z_3)$.

In order to fully characterize the oscillator, we can use also the two-port model [7]. The VCO can be viewed as feedback circuits and it needs to satisfy the well-known criteria of Barkhausen [7]. The loop gain, $H_1(j\omega)$, as been evaluated by using the Return Ratio method. A simulated example of the magnitude and phase of $H_1(j\omega)$ is given in Fig. 5: where the phase is zero the magnitude of the loop gain is still above 10 dB and, thus, high enough for the start-up of the oscillator. The slight difference for f_{osc} between Fig. 4 and Fig. 5 is due to the Return Ratio method which only gives an approximation for the loop gain.

The common base stage, consisting of T_2 stacked to T_1, was intended to improve the decoupling between the VCO-core

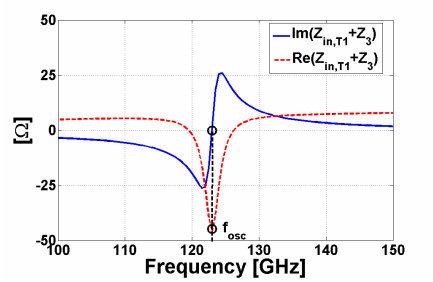

Fig. 4 Simulated impedance of $Z_{in,T1}+Z_3$.

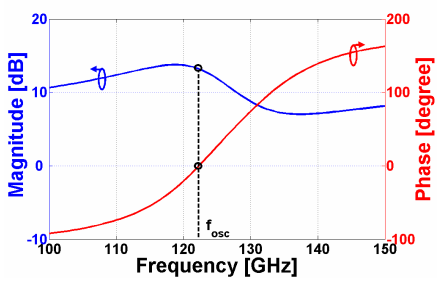

Fig. 5 Simulated magnitude and phase for the loop gain $H_1(j\omega)$.

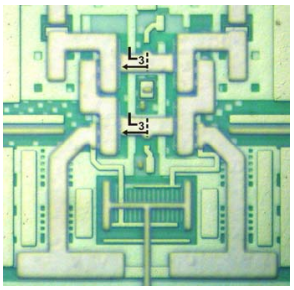

Fig. 6 Detail of the layout of the VCO-core. The transmission lines L_3 are identical and very short. They show a length of 10 µm.

and the output buffer stage at the cost of increased phase noise [5,7]. In order to avoid instability issues at the common base stage (cascode), it must be layouted with the two bases very close to each other. Since the target frequency for this VCO is 122 GHz, the transmission lines L_3, which are part of the resonator, are very short. They have a length of 10 µm, as shown in Fig. 6. In the layout, for placement reasons, the minimum possible distance between the transistors T_2 in the common base stage was comparable with 10 µm. Therefore we designed the cascode similar to the stage consisting of T_1 and L_3. In this configuration this stage becomes part of the VCO-core and its behavior is set by L_3, L_{par} and L_4-L_5. L_4 and L_5, with the output impedance of T_1, transform the input impedance of T_2 which will also oscillate at f_{osc}. In fact, also in this case the network consisting of the input impedance of T_2 and Z_3 satisfies the one-port conditions for oscillation. Moreover, also the second loop gain including T_2 satisfies the two-port conditions. The results of a simulation example are plotted in Fig. 7 and 8. The loaded Q_L given by [7] has been also evaluated for the two cases and the results are shown in

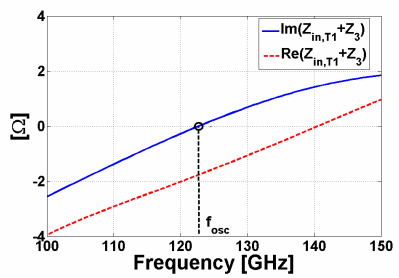

Fig. 7 Simulated impedance of $Z_{in,T2}+Z_3$.

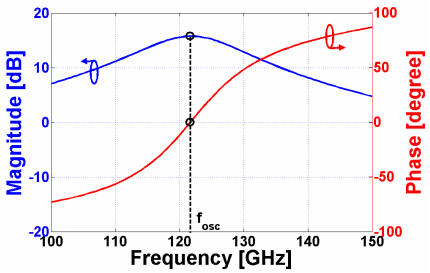

Fig. 8 Simulated magnitude and phase for the loop gain $H_2(j\omega)$.

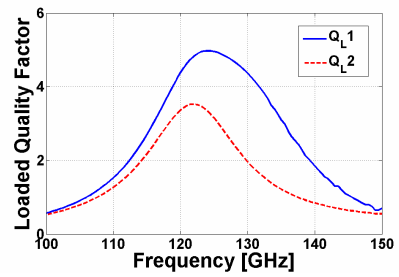

Fig. 9 Simulated loaded Q_L.

Fig. 9. The common base stage, T_2, is efficiently decoupling the VCO stage consisting of T_1 from the buffer which load the VCO-core. L_4 and L_5 are also used to achieve the maximum output swing, which improves the output power. Moreover, they act as an inductive voltage divider to still reduce the load of the buffer input [8]. Because of the large signal swing in the oscillator, there was not enough headroom left to use a current mirror. A resistor has been implemented as current source. The current in the VCO-core is 100 mA.

Fig. 10 shows the schematic diagram of the output buffer. The differential output signal from the VCO-core is applied via AC-coupling capacitances and the short transmission line L_6 to the emitter follower (EF) pair. The emitter followers have been used mainly for their impedance transformation property and to improve the decoupling between the output and the VCO. The transistors in the emitter follower configuration show an input impedance with negative real part that combined with some parasitics can cause parasitic oscillations [6]. In order to prevent these oscillations and improve the stability of the EFs, damping resistors R_{damp} have been used at the cost of a reduced output power. The

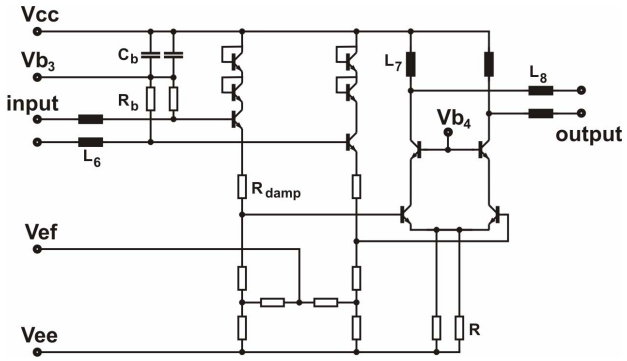

Fig. 10 Output buffer schematic: a cascode stage driven by emitter followers.

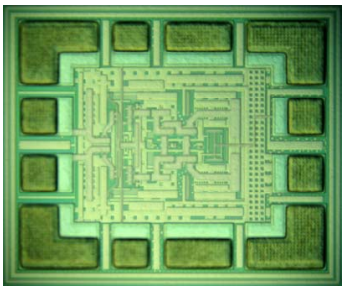

Fig. 11 Chip photograph of the fundamental VCO.

capacitances C_b provide a path to ground to avoid potential parasitic oscillations. The emitter followers drive the output buffer which consists of a cascode stage. The output buffer is needed in order to improve the output power and reduce the load-pulling effect. The transmission lines L_7 and L_8 are used as load in the cascode and also for on-chip matching of the external 50 Ω load. The gain of this cascode is quite small, due to the limited transistor current gain $\beta \approx 1.6$ at 122 GHz. For this reason the VCO-core must provide a large signal power to the output buffer in order to achieve the desired output power. The bias voltages $Vb_{1\text{-}4}$ are generated on chip.

III. EXPERIMENTAL RESULTS

The chip is manufactured in an advanced 200 GHz f_T SiGe:C bipolar process based on the technology presented in [9]. The transistors in the chip operate at a current density of 6.5 mA/μm^2. The chip photograph is presented in Fig. 11. The size of the chip is 478 x 578 μm^2.

Measurements were performed on wafer. The supply voltage was -6 V (losses in the voltage supply filter not deembedded) while the current consumption 310 mA. The output spectrum of the oscillator has been measured with a 50 GHz spectrum analyzer (Agilent 8565E), using an Agilent external harmonic mixer 11970W. This mixer is specified for the W-band but is still capable to down-convert signals beyond 110 GHz at the cost of high conversion loss. The output power was measured by using an Agilent W8486A waveguide power sensor connected to a HP 438A power

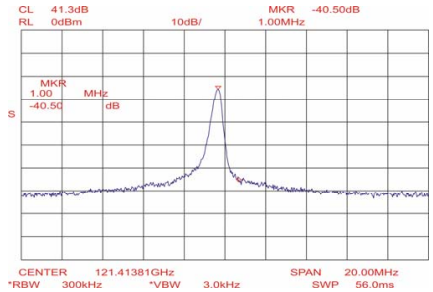

Fig. 12 Single-ended output power spectrum of the VCO at a center frequency of about 121.4 GHz.

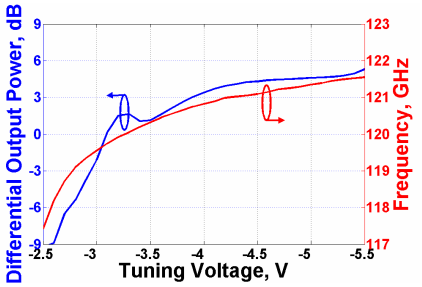

Fig. 13 Oscillation frequency and differential output power vs. tuning voltage. Since the power sensor is specified up to 110 GHz, the measured values represent an estimation of the real power.

meter. Since the power sensor is specified up to 110 GHz, we have to consider the values for the output power just as an indication of the real maximum output power delivered by the VCO. For this estimation the losses by the measurement setup have been deembedded.

From Fig. 12 the phase noise of the VCO, which includes an output buffer stage, can be obtained at a carrier frequency of 121.4 GHz. But this value for the phase noise is too optimistic. As explained in [10], the measured values must be corrected due to the voltage envelope detector and due to the ratio of the equivalent noise bandwidth to the -3 dB bandwidth. By including these factors, the phase noise at 1 MHz results to be -93.3 dBc/Hz, which is an excellent value in this frequency range for a fundamental SiGe VCO. This measured phase noise is 2 dB worse than the simulated value. Because of the emitter followers and the output buffer stage, for the VCO presented in this paper the influence from the external waveguides used in the measurement setup, which usually act as a resonator improving the phase noise as explained in [11,12], is strongly reduced.

In Fig. 13 the dependence of the oscillation frequency on the tuning voltage V_{TUNE} is shown. The VCO displays 4 GHz of tuning range. According to simulations, the differential output power should be above 4 dBm.

For measuring the temperature dependence of the VCO, the chuck temperature was increased from 10 °C to 125 °C. Within this range, the oscillation frequency decreases by about 2.3 GHz, caused mainly by the decrease of f_T. The VCO can easily achieve the target frequency of 122 GHz by slightly

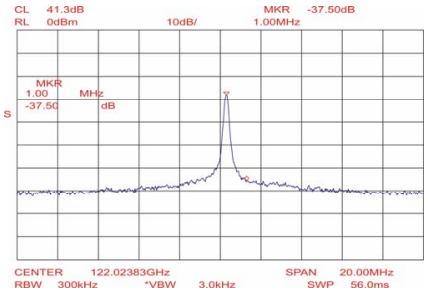

Fig. 14 Single-ended output power spectrum of the VCO at a center frequency of approximately 122 GHz.

increasing the supply voltage. As shown in Fig. 14, at this frequency the phase noise is -90.3dBc/Hz at 1 MHz offset.

IV. Conclusion

A fundamental VCO and an output buffer have been integrated on a single chip. Operation of the VCO beyond 120 GHz has been demonstrated with very good value of phase noise. To the authors' knowledge, this is the highest oscillation frequency reported to date for a fundamental voltage controlled oscillator with integrated output buffer in SiGe bipolar technology.

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