Thermal Simulations of III/V HEMTs

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Abstract

Thermal management is a key problem for semiconductor RF-components due to the reduction of chip and device performance by thermal effects. The simulation of devices at various operating temperatures and the inclusion of self-heating effects in the simulation are therefore crucial for the optimization of devices with respect to chip and system performance as well as for reliability concerns. We present investigations of GaAs based High Electron Mobility Transistors (HEMTs) using the two-dimensional device simulator MINIMOS-NT. This includes the critical influence of the contact modeling and findings for realistic thermal boundary conditions. Temperature dependent DC transfer characteristics, RF-simulation results, and comparisons to measurements of state of the art HEMTs are given.

1. INTRODUCTION

Our work demonstrates electrical and electro-thermal investigations of GaAs-based High Electron Mobility Transistors (HEMTs) using the two-dimensional device simulator MINIMOS-NT [1]. E.g., automotive applications such as the W-band collison avoidance radar demand environmental temperatures of operation between 230 K and 400 K. Heat conduction in III/V-based semiconductors is generally lower than in silicon. The evaluation of sophisticated packaging techniques, e.g. for high-power devices on semi-insulating GaAs substrates [2], becomes crucial. As lattice temperature dependent device simulations including mounting aspects in silicon devices have been demonstrated, cf. [3], this work addresses III/V HEMTs with gate-lengths l_g down to 140 nm. In this way the changes in the device performance with temperature can be linked to the effects setting thermal boundaries by packaging. The general thermal modeling within MINIMOS-NT is described in [4]. Further modeling has been demonstrated in [5, 6]. In addition, new insulator materials have been implemented into MINIMOS-NT such as AlN and Al_2O_3 which allows advanced modeling of thermal boundaries. Critical areas of the heat generation and lattice temperature distribution depending on the boundary conditions can be quantitatively evaluated. This is useful to optimize the devices not only towards electrical, but also towards thermal criteria.

2. DEVICE SIMULATIONS

The most general approach to account for electro-thermal problems in HEMT devices is a three-dimensional device simulator to account for all possible effects in devices, especially for the heat spreading. This work on HEMTs is based on the assumption that a large number of investigations of practical interest can and have to be performed using a two-dimensional approach for the following reason: Fig. 1 shows the extended two-dimensional cross section of a realistic device which to our finding is the least complex structure to account for heat spreading in a device. The area normally accounted for in an electrical two-dimensional HEMT simulation extents up to some 5 μm^2, given by the dashed box in Fig. 1. Yet, the minimum distances to heat sinks on a RF-chip, as shown in Fig. 1, can extent up to 50 μm, if thinned chips are mounted. The lateral extension for the simulation has to be at least 50 μm. We find it very desirable for electro-thermal RF device simulation to find ways to simulate realistic

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thermal boundary conditions for the two-dimensional problem for the HEMT for the reason of efficiency. This argument shall not question the need for further development of three-dimensional tools. For device simulation a hydrodynamic transport model has been used to account for hot electron effects. A two step approach is chosen. First, lattice temperature dependent models are used without solving the heat flow equation to evaluate the thermal model as a function of constant lattice temperature in a device. With this model e.g. transfer curve measurements of industrial devices can be simulated. Second the heat flow equation is included allowing the evaluation of packaging and thermal optimization.

3. HEAT GENERATION

The heat generation in a device or in analytical description is based on four terms according to [7]. They can be written as:

$$H = H(\text{joule heating}) + H(\text{generation/recombination}) + H(\text{Thomson}) + H(\text{radiation}) \quad (1)$$

When evaluating the heat generation for HEMT devices quantitatively we confirmed the common assumption [8] that unipolar devices are governed by the joule dissipation term. By adding recombination models to the simulation it is found that given low natural p-doping concentration in the AlGaAs spacer, recombination heat can be neglected in HEMTs. The ohmic contacts are modeled in a more macroscopic approach, so any recombination at the contacts is included in the approach given below. Impact ionization is neglected in these examples given due to the limited V_{DS} bias applied. Thomson effects are neglegible according to [4, 7]. The electromagnetic interaction with radiation is not included in this approach.

4. BOUNDARIES

Contact conditions can be realized thermally only and electrically/thermally combined. The realized thermal boundary conditions at the contacts in MINIMOS-NT can be Dirichlet conditions setting the lattice temperature at the contact to a given value or Neumann conditions defining a thermal resistor towards an imaginary heat sink at a given temperature. In a HEMT the minimum distance of an area with maximum thermal activity towards the Schottky contact boundary can be as short as a few nm, so a very careful usage of these boundaries, as stated by e.g. [9], is necessary.

The generally assumed thermal blocking of the gate reflects the fact that in a HEMT the gate contact temperature itself is strongly determined by heat generation of the gate area. The gate can only be set to a constant temperature or being used as a heat sink, if and only if elaborate cooling measures are provided, which is usually not the case on RF-chips since the gate connection to the environment is rather thin.

The thermal conductivity of the passivation films is comparably low as given in [10], so the heat transfer out of the device passivation in the surrounding air was neglected, whereas the passivating layers themselves were fully accounted for both electrically and thermally. Regarding the thermal boundary condition of the ohmic contacts the following approach was used: The contact modeling consists of two parts: the first part is the contact model itself, which is described e.g. in [4], the second the understanding of the underlying effective conduction band edge in the caps as a results of the alloying process, see e.g. [11]. To account for the effective temperature dependence of the ohmic contacts and the caps the following approach is used. For the HEMT technology given the temperature dependence of the ohmic contacts is evaluated regarding typically extracted parasitic elements R_S and R_D: They are modeled to consist of two contributions:

$$R_s(T) = R_{s\,metal}(T) + R_{s\,thermionic}(T) \quad (2)$$

The first so called metal part of R_S shows a metal like rise in the electrical resistance with rising temperature. The second contribution at the source side accounts for a step in the effective conduction band edge found even for the alloyed contact and the cap. The ohmic contacts given are governed by the first contribution resulting in a general increase of the electrical resistance with rising temperature. Yet R_S and R_D show different temperature coefficients. The second thermionic contribution will lead to a decrease with rising temperature due to the thermionic effect especially on the source side.
The temperature dependence of this contribution from the additional step is modeled by applying a thermionic emission model at in the GaAs/AlGaAs interface between the caps and the spacer. The AlGaAs/InGaAs interfaces are modeled by a thermionic field emission interface model, see [1]. By further applying the temperature dependence of the metal part using a temperature dependent series line resistor at the contact it was found that realistic simulation results could be obtained as presented in the following chapter.

5. RESULTS

Fig. 2 shows the lattice temperature dependence of the transfer characteristics for lattice temperatures of 298 K and 373 K and a comparison to measurements taken at the same temperatures at $V_{DS} = 1.5$ V without the inclusion of self-heating.
Generally a rise of the pinch off current, a drop in the DC-g_m, and a decrease in saturation current can be observed as a function of rising temperature. The drop of the drain current I_D and the drop in DC-g_m can be understood as follows: On the one hand the carrier mobility, especially the zero field mobility, is a decreasing function of temperature. Further the saturation velocity is a function of T_L [6]. We again emphasize the influence of the cap geometry and the ohmic contacts for a realistic simulation. The simulations agree well with the measurements in the given V_{GS} range for both temperatures. Despite of the good agreement slight differences were observed in the lower part of the curves when simulation overestimates the measured currents.
Fig. 3 shows the heat generation distribution when including the solution of the heat flow equation in a HEMT. The contact configuration is given in Fig. 1. Trying different thermal boundary conditions it is found that the heat generation in the bias and temperature ranges given is fairly independent of the thermal boundaries set at the contacts, which is typical for the joule heat generation. Maximum self-heating occurs at the drain end of the gate due to the maximum electrical fields, yet, also typical for joule heating, the sum of the heat generation integrating over the caps cannot be neglected. The current distribution is determined by the real space transfer modeled by the thermionic field emission interface model at the channel to spacer interface. The field distribution leads to the temperature distribution given in Fig. 4 assuming a temperature of $T_L = 330$ K set at both ohmic contacts. This simulation assumes a substrate contact 50 µm from the gate in the configuration of Fig. 1 with an ideal heat sink at the thermal substrate contact. The maximum local temperature in the channel amounts to 348 K in the high field region given no heat transition over spacer to gate transition at the Schottky contakt. Assuming a thermal resistor at the ohmic contacts can lead to significant artefacts if the resistor is directly included in the contact model itself since the thermal resistor is typically distributed over the distance to the heat sink.
Next we analyze the influence of the sub mount on the lattice temperature distribution in the channel for an active bias. The three electrical contacts do not allow any heatflow, whereas the substrate contact at a distance of 50 µm from the gate is kept at a temperature of 330 K. Fig. 5 shows the difference of an ideal heat sink attached to the substrate and an additional heatspreader using Al_2O_3 between the substrate and an ideal heatsink. The local temperature in the channel changes from a maximum local temperature of about 360 K in the ideal case to a maximum local temperature of 375 K. These values have to be taken within the limits of the two-dimensional approximation and the lateral heat spreading assumed.
Fig. 6 shows the comparison of the simulated [12] and measured drop of the current gain cut-off frequency f_T with lattice temperature for a gate-length of $l_g = 140$ nm and an extraction taken

from a device with a gate-width of 4x40 μm. The drop in f_T is caused by the drop in g_m whereas the capacitances C_{gs} and C_{gd} are found to remain constant in the temperature range given. The important influence of the source resistor was modeled as given above. Thereby it is possible to compare the results obtained by MINIMOS-NT to extrinsic S-parameters and f_T values.
To demonstrate the impact of a geometrical variation on thermal aspects Fig. 7 shows the results of a simple experiment. By shortening the distance d of both the ohmic contacts to the gate without changing the given recess geometry it can be show that the local temperature distribution within the device can be relaxed. Since for high speed devices with gate-lengths l_g = 150 nm and shorter the number of available parameters is restricted by electrical demands, simulation can support device optimization by evaluating the trade-off between electrical and thermal demands. The obvious advantage of a combined electro-thermal simulation is that the impact of the changes on the decisive small signal elements C_{gs}, C_{gd}, and g_m can be evaluated in the same device simulation. For rough operating conditions of high speed devices with high ambient temperatures such measures on the device level can help to control local overheating, if and only if it is possible to mount efficient heat sinks nearby. Though lowering the effective temperature in the simulation by this measure practical concerns of placing heat sinks will decide on the possibilities of the metalization in general for realistic cooling purposes.

6. CONCLUSION

Our work demonstrates temperature dependent electrical and electro-thermal device simulations of GaAs-based HEMTs. We show the general models in MINIMOS-NT are capable of simulating transfer characteristics at different lattice temperatures. The temperature dependence of the current gain cut-off frequency f_T can be realistically reproduced. A better understanding of the ohmic contact behavior was obtained regarding the temperature dependence of the equivalent circuit parasitic elements. Using further arguments from mounting techniques the maximum local temperature distribution in a HEMT can be estimated as a function of the boundary conditions.

Acknowledgments

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Figures

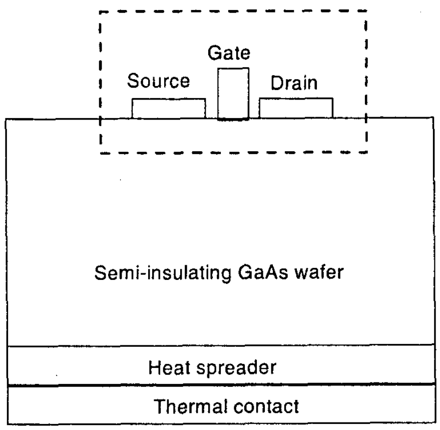

Fig. 1 Heat spreading in an extended device (non to scale)

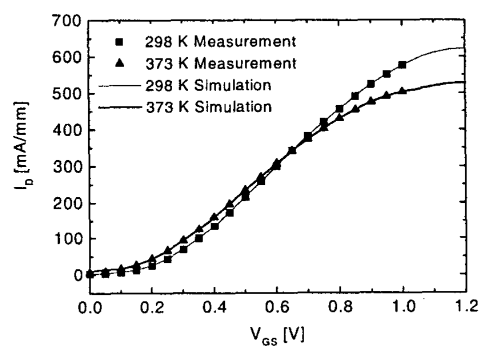

Fig. 2 Impact of the homogenous temperature change on the transfer curves at $V_{DS} = 1.5$ V.

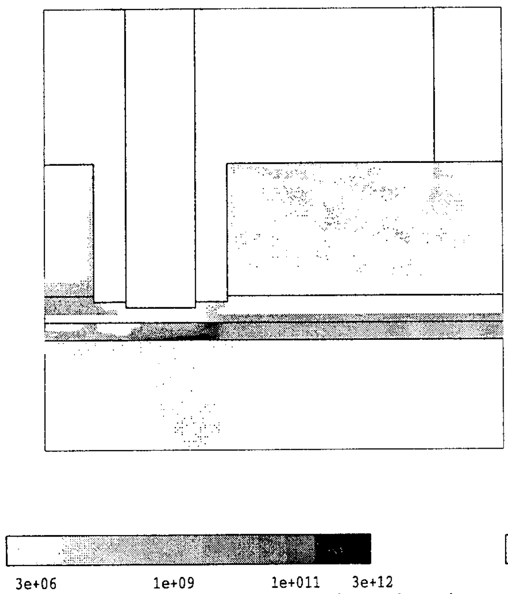

Fig. 3 Heat generation distribution, given in a.u..

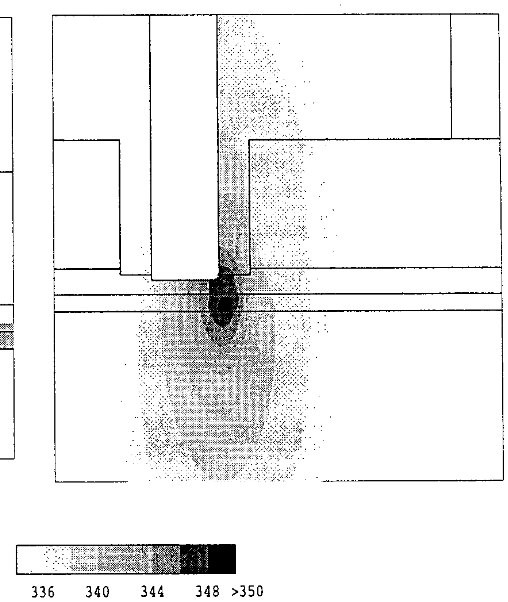

Fig. 4 Equivalent temperature distribution given in K.

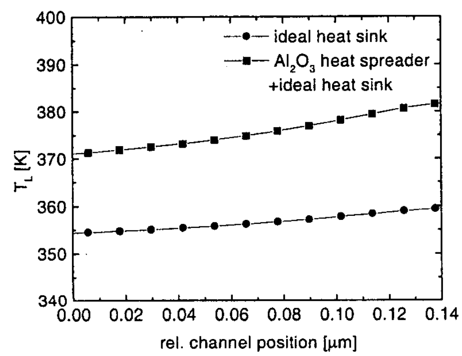

Fig. 5 Influence of the sub mount on the lattice temperature T_L in the channel under the gate of l_g = 140 nm.

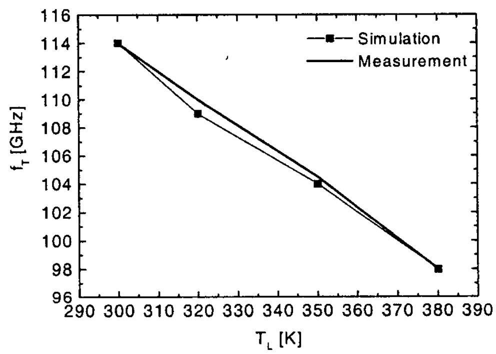

Fig. 6 f_T as a function of the lattice temperature and comparison to measurements for l_g= 140 nm at g_{mmax}.

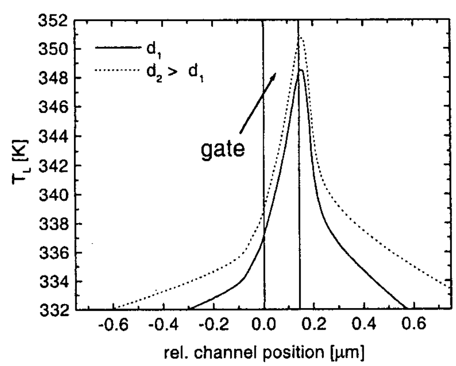

Fig. 7 Lattice temperature distribution along the channel when varying the distance d between the ohmic contacts without other changes in the device structure or boundaries.