A LOW-POWER LOW-VOLTAGE NMOS BULK-MIXER WITH 20 GHZ BANDWIDTH IN 90 NM CMOS

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Student Paper

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ABSTRACT

A fully differential low-voltage mixer topology is presented. The problem of stacking input-, cascode- and switching-transistors within 1.2 V supply voltage is solved by the use of a bulk driven mixer core. In order to demonstrate the feasibility a testchip was manufactured in INFINEON triple well 90 nm standard CMOS process. The differential mixer includes an on-chip resistive 50 Ω termination and an operational amplifier for measurements. The chip features a gain of 3.2 dB, a DSB noise figure of 17.4 dB, an input IP3 of -2.1 dBm, an input 1dB compression point of -13.3 dBm and consumes 1.8 mW at a power supply voltage of 1.2 V. The mixer has a 3 dB low-pass bandwidth of 20 GHz.

1. INTRODUCTION

The ongoing technology down-scaling increases continuously the attractiveness of RFCMOS transceivers as the high frequency capability meanwhile largely exceeds the frequency of popular GSM, UMTS or WLAN applications [1, 2]. E.g. a modern 0.13 μm standard CMOS process [3] features an f_T of about 100 GHz enabling highly integrated transceivers as demonstrated e.g. for UMTS-applications in [4, 5]. However the decreasing power supply voltages with the technology downscaling leads to severe circuit design problems [6, 7]. The nominal power supply voltage of e.g. 1.2 V of 90 nm CMOS severely limits the possibility of transistor stacking. Common designers practice of using cascode structures becomes nearly impossible. Especially mixers are an important component in wireless transceiver designs which often involves trade-offs between conversion gain, bandwidth, noise figure, supply voltage and power consumption. This paper investigates a classical Gilbert mixer which is used as a four terminal device for low supply voltage capability at ultra low power consumption [8].

2. DESIGN

Fig. 1 shows the circuit diagram of the NMOS bulk-mixer. The circuit consists of four NMOS-transistors wired to a double-balanced Gilbert mixer. The specific idea is to use the bulk contact of the MOSFETs as a second input. Therefore

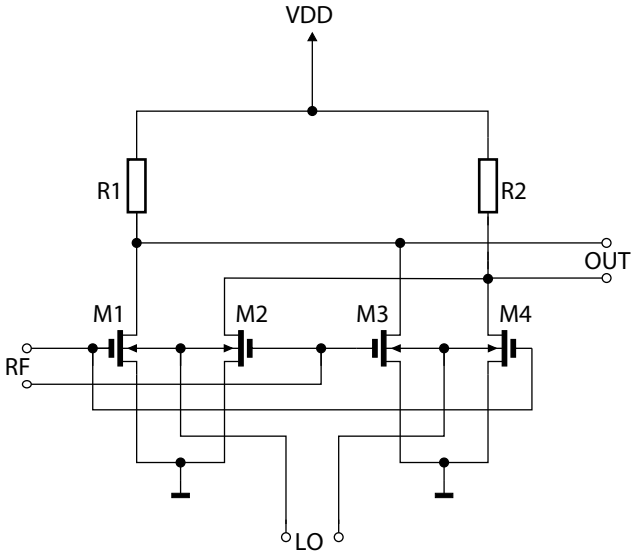

Figure 1: Mixer schematic.

a triple well process is used to implement an NMOS bulk driven mixer. This results in two advantages for the mixer design. First NMOS transistors have a much higher transconductance than PMOS transistors. Secondly the 90 nm process features also a higher transconductance than a 130 nm process and enables a higher bandwidth. In this circuit the gate transconductance is used for the radio frequency input, while the switching of the signal is provided by the local

oscillator frequency through the bulk transconductance.

The simplified small-signal high-frequency model of one transistor is shown in Fig. 2. As shown in [8] the small signal gain can be calculated as:

$$G = -g_m(R_o||R_L). \quad (1)$$

The downconverted signal $\omega_{LO} - \omega_{RF}$ is the mix product of the RF input ω_{RF} and the square wave LO signal ω_{LO}. This results in the conversion gain of the mixer:

$$CG = -\frac{2}{\pi} g_m(R_o||R_L). \quad (2)$$

In this equation R_o represents the output resistance of the transistor while R_L is the load resistor of the mixer. The

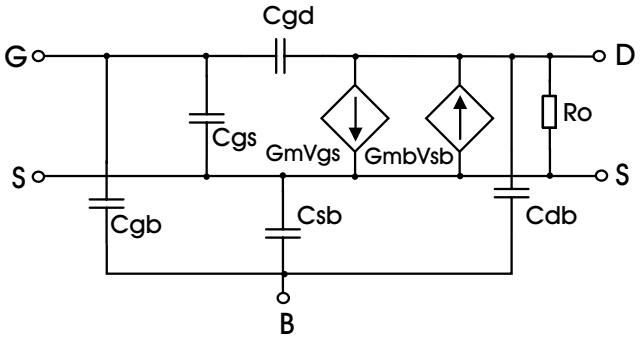

Figure 2: Small-signal high-frequency MOS model.

schematic of the test chip including the resistive 50 Ω termination and an operational amplifier both on-chip and the measurement setup is shown in Fig. 3. The optimum bias points for the RF and the LO inputs are chosen to maximize the conversion gain.

In the circuit illustrated in [6] a transformer is inserted into the mixer design to extend its operation down to very low supply voltages. The obvious disadvantages of this design are the smaller bandwidth because it is limited by the transformer and the resulting high area demand. In comparison with [7], the folded-mirror mixer design has more active transistors which result in additionally noise. The introduced NMOS bulk mixer requires only four transistors and allocates an active area of about 40 μm x 90 μm.

3. MEASUREMENT RESULTS

The measurements were performed with the chip directly mounted on a 30x30 mm^2 0.51 mm RO4003 microwave substrate ($\varepsilon_r = 3.38$) with SMA connectors. Fig. 4 shows the evaluation board mounted on a high frequency test fixture. The chip photograph is shown in Fig. 5. The die size is 490μm by 470μm. All measurements were done at

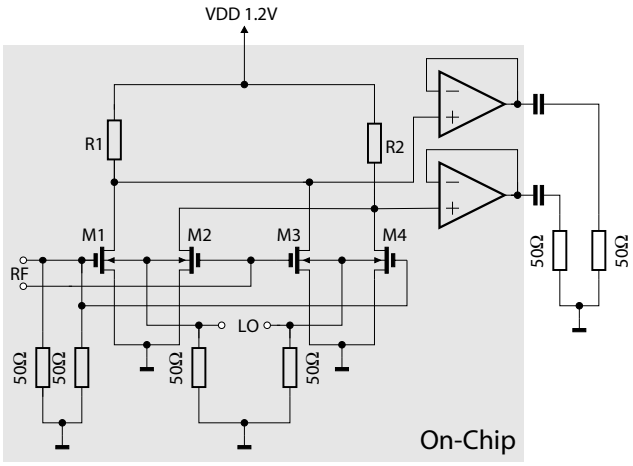

Figure 3: Mixer testchip schematic and measurement setup.

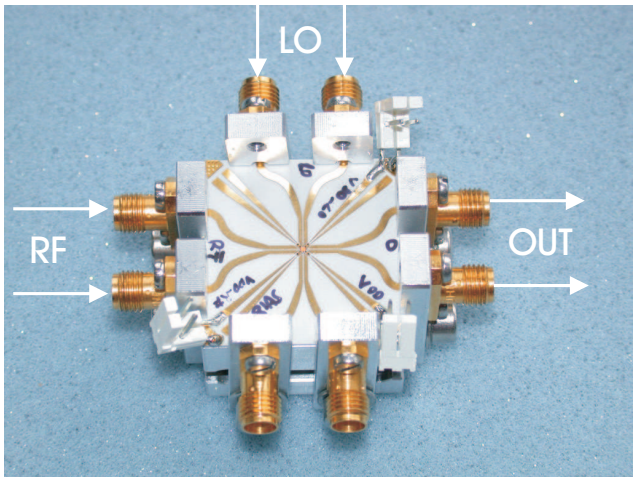

Figure 4: Photograph of the mixer test-board.

1.2 V supply voltage and the power consumption was 1.8 mW. The mixer linearity was measured for an LO input frequency of 12.05 GHz and an RF input frequency of 12 GHz. The one-tone compression measurement is presented in Fig. 6. A measured 1-dB input compression point of -13.3 dBm was found. Also noticeable is the strong reduction of the gain in the region beyond the 1-dB compression point. This effect was also seen in simulations. It is probably due to the high RF and LO amplitudes shifting the operating point of the mixer transistors. The two-tone intermodulation measurements are presented in Fig. 7 and 8. The distance between the tones of 1 MHz is deviated from typical wireless applications. The 1.2 V mixer features a measured input IP3 point of -2.1 dBm.

Also the noise figure was measured at 12 GHz LO fre-

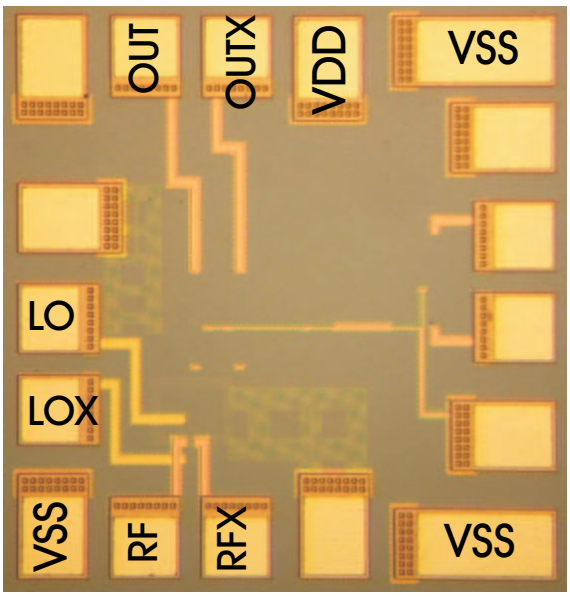

Figure 5: Mixer testchip photograph.

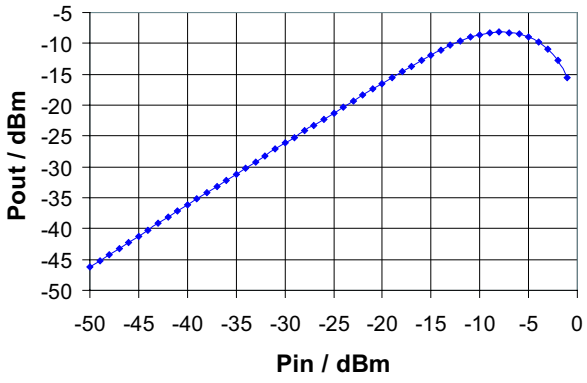

Figure 6: Mixer 1dB-compression, LO 12.05 GHz 9 dBm, RF 12 GHz.

quency using hp 8970B noise figure meter. The measured DSB noise figure is 17.4 dB. The frequency range of operation of the mixer was measured by sweeping the RF- and the LO-input frequency with a constant offset of 50 MHz. The result is presented in Fig. 9. The NMOS bulk-mixer achieves a high 3 dB low-pass bandwidth of about 20 GHz. This limitation is the result of the mentioned evaluation board and its SMA connectors, which have a cut-off frequency of about 18 GHz. The mixer characteristics are summarized in Table 1.

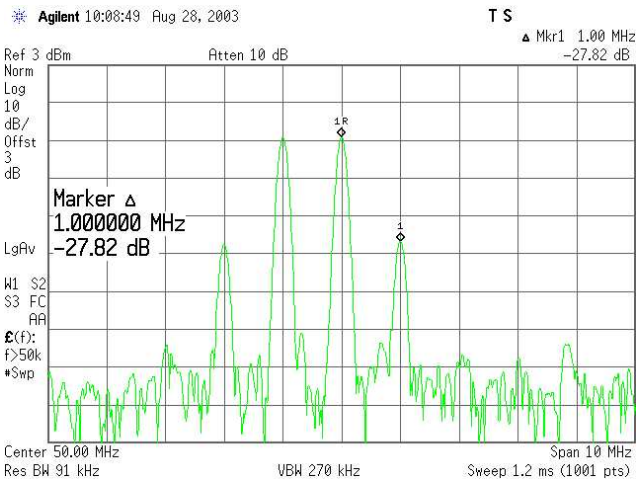

Figure 7: Mixer two tone test output spectrum for LO 12.05 GHz 9 dBm and RF 12 GHz & 12.001 GHz both -17dBm.

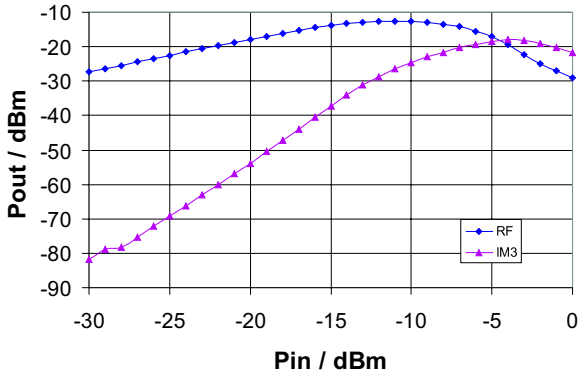

Figure 8: Mixer two tone test, LO 12.05 GHz 9 dBm, RF 12 GHz & 12.001 GHz.

4. SUMMARY

A broadband mixer design is proposed to extend the use of classical Gilbert mixers to very low supply voltages. Due to the exploitation of both a 90 nm CMOS process and NMOS transistors instead of PMOS transistors the bulk driven mixer core consumes low power and features a high bandwidth. The differential mixer includes the on-chip resistive 50 Ω termination and an operational amplifier for measurements. The circuit features a gain of 3.2 dB, a DSB noise figure of 17.4 dB, an input IP3 of -2.1 dBm, an input 1 dB compression point of -13.3 dBm and consumes 1.8 mW at a power supply voltage of 1.2 V. The mixer has a 3 dB-bandwidth of 20 GHz.

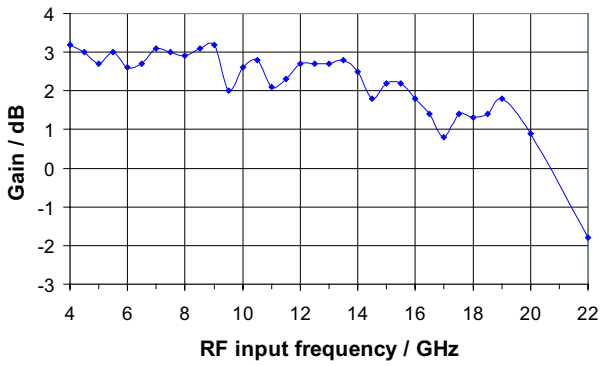

Figure 9: Mixer gain over frequency, LO power 9 dBm, fixed output frequency of 50 MHz.

Power supply	1.2 V
Power consumption	1.8 mW
Gain	3.2 dB
DSB Noise Figure	17.4 dB
Input compression point	-13.3 dBm
Input IP3	-2.1 dBm
3 dB Low Pass Bandwidth	20 GHz
Active Area	40 μm x 90 μm
Technology	90 nm standard CMOS

Table 1: Mixer summary, nominal operation at 2 GHz LO frequency and 2.15 GHz RF frequency

5. REFERENCES

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