A low-noise and high-gain double-balanced mixer for 77 GHz automotive radar front-ends in SiGe bipolar technology

W. Perndl [1,2], H. Knapp [2], M. Wurzer [2], K. Aufinger [2],
T. F. Meister [2], J. Böck [2], W. Simbürger [2], A. L. Scholtz [1]

Student Paper

[1] Institute of Communications and Radio-Frequency Engineering
Technical University of Vienna
Gusshausstrasse 25/389, A-1040 Vienna, Austria

[2] Infineon Technologies AG, Corporate Research,
Otto-Hahn-Ring 6, D-81739 Munich, Germany
E-Mail: Werner.Perndl@Infineon.com

***Abstract* — An active down-conversion mixer for automotive radar applications at 76 GHz to 81 GHz was realized in a 200 GHz f_T SiGe bipolar technology. A conversion gain of more than 24 dB and a single-sideband noise figure of less than 14 dB is achieved. The 1 dB output compression point is -4 dBm. The power consumption is 300 mW at -5 V supply voltage.**

***Index Terms* — Mixer, SiGe, double-balanced, low-noise, high-gain, Gilbert mixer, 77 GHz, automotive radar.**

I. Introduction

Recent advances in SiGe bipolar technology and improvements in the circuit design enable the use of silicon-based circuits for new emerging applications, like automotive radar sensors at frequencies from 76 GHz to 81 GHz. Up to now, this field was dominated by III-V semiconductors ([1], [2], [3]).

In this work, an active mixer in SiGe bipolar technology for down-conversion with a conversion gain of more than 24 dB and single-sideband (SSB) noise figure of less than 14 dB in the frequency range from 76 GHz to 81 GHz is presented. An active down-conversion mixer up to 40 GHz in a silicon-based technology is presented in [4] with a gain of 25 dB and a double-sideband (DSB) noise figure of 15 dB. A 60 GHz transceiver in SiGe bipolar technology is presented in [5]. The mixer of this transceiver shows a gain of 18.6 dB and a noise figure of 13.3 dB at 60 GHz.

Mixers in the mm-wave frequency range have been realized as passive diode ring-mixers with Si-Schottky diodes to obtain low 1/f-noise, for example. A diode mixer in [6] exhibits a conversion loss of 10 dB and a SSB noise figure of 18 dB at an IF frequency of 100 kHz. A state of the art GaAs HEMT mixer is presented in [1] which exhibits a conversion loss below 11 dB and SSB noise figure of 20 dB at 1 MHz intermediate frequency (IF) frequency.

II. Circuit Design

The mixer presented in this work consists of a mixer core, an LO buffer, a balun at the RF input and an IF buffer. A simplified circuit diagram of the mixer is shown in Fig. 1.

The mixer core is based on the Gilbert-mixer [7]. It has a double-balanced structure and utilizes differential LO and RF signals. Transistor sizes and bias currents are optimized in order to obtain a good compromise between gain, linearity and low noise figure. The size of the switching transistors is designed at the current density for maximum f_T, whereas the RF transistors are designed for minimum noise contribution. In order to improve LO-IF isolation and RF-IF isolation an on-chip low-pass filter is used in front of the IF buffer. DC levels are set by the emitter-followers of the LO buffer and the diode bias circuit at the RF input.

The IF buffer provides impedance matching at the IF output. The IF buffer increases the conversion gain but slightly reduces noise performance. Emitter degeneration is used for linearity improvement.

The differential signals required for LO and RF inputs of the mixer core are generated by the LO buffer and the LC balun, respectively. The LO buffer (Fig. 2) consists of a differential amplifier which provides a differential output signal from the single-ended input. Due to the reduced common mode rejection ratio (CMRR) of the differential

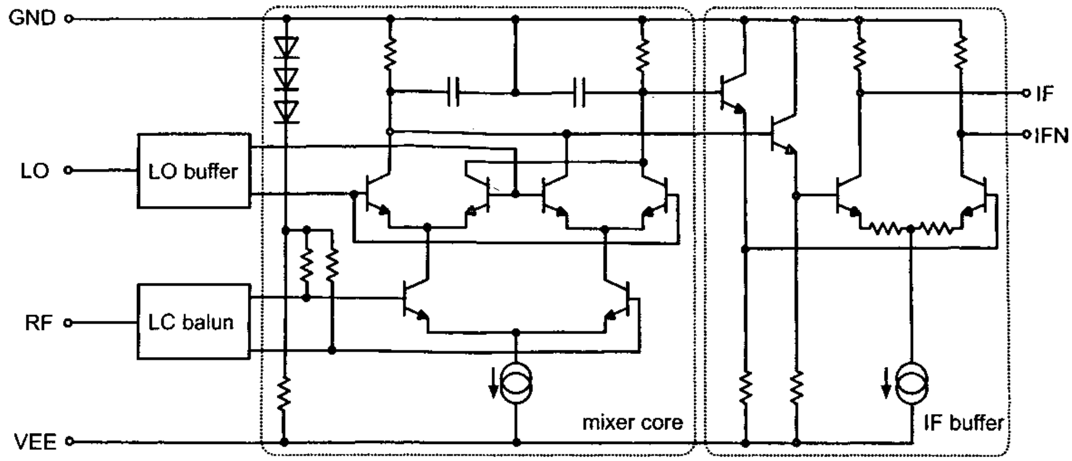

Fig. 1. Simplified circuit diagram of the mixer (GND = 0 V, VEE = -5 V)

amplifier and the low output resistance of the tail current source at the target frequency range, AC coupling is used in order to prevent a DC offset at the LO input of the mixer core. Emitter-followers provide a low impedance interface to the switching mixer circuit. Additionally the LO buffer acts as a limiting amplifier to provide a constant LO signal amplitude for the mixer core. A 50 Ω on-chip resistor is used in order to provide matching at the LO input.

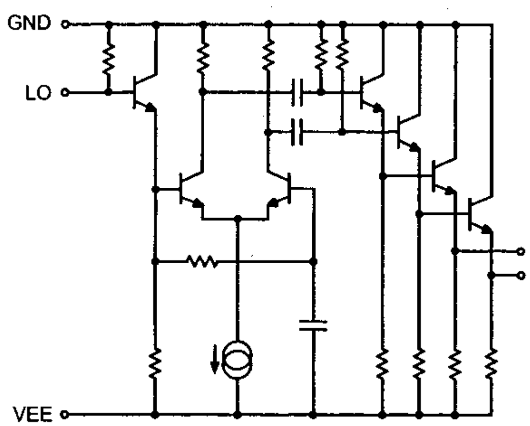

Fig. 2. Circuit diagram of the LO buffer

The circuit diagram of the LC balun at the RF input is shown in Fig. 3. In Fig. 4 the corresponding photograph of the chip is depicted. The inductive elements of the balun are realized as microstrip lines with the signal line in the fourth and the ground plane in the second metal layer. Capacitances are realized with MIM-capacitors. The transmission lines TRL_3 and TRL_4 transform the impedance of the RF input transistors into a real-valued resistance.

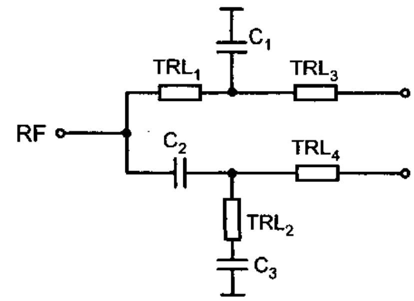

Fig. 3. Circuit diagram of the LC balun. Transmission lines are drawn as rectangles. TRL_1 and TRL_2 represent inductances, TRL_3 and TRL_4 are used for impedance transformation.

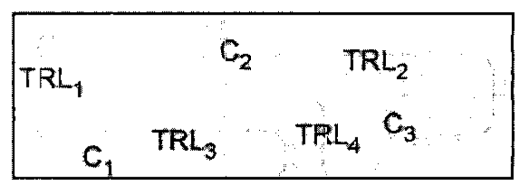

Fig. 4. Detailed view of the LC balun

The LC balun consisting of the transmission lines TRL_1 and TRL_2 and the MIM-capacitors C_1 and C_2 converts the balanced to an unbalanced signal and provides an impedance transformation for 50 Ω matching at the RF input. Capacitor C_3 is required to achieve an RF ground at TRL_2. The LC balun was designed based on the calculation of a lumped element balun [8]. Then the inductances were substituted with transmission line TRL_1 and TRL_2 [9]. Further optimization was done using a field simulatior.

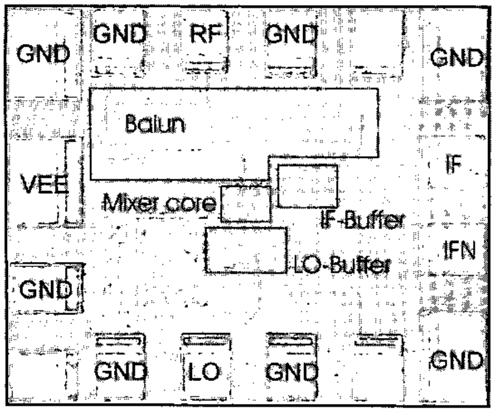

Fig. 5. Chip photograph of the mixer (chip size: 550 μm × 450 μm)

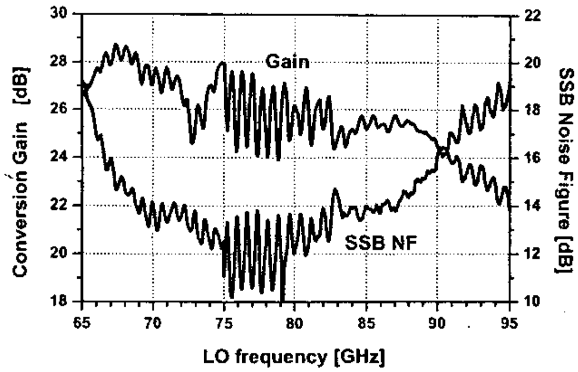

Fig. 6. Measured conversion gain and SSB noise figure versus LO frequency. IF frequency is 500 MHz, LO power is 2 dBm.

III. TECHNOLOGY

The mixer is fabricated in a SiGe bipolar technology which is based on the process technology presented in [10]. The transistors have a double-polysilicon self-aligned emitter-base configuration with an effective emitter width of 0.18 μm. The SiGe:C base of the transistors has been integrated by selective epitaxial growth and the transistors exhibit a monocrystalline emitter contact.

The transistors manufactured in this technology offer a transit frequency f_T and a maximum oscillation frequency f_{max} of more than 200 GHz and a ring-oscillator gate delay of 3.7 ps.

The technology provides four copper metallization layers, two different types of polysilicon resistors and a TaN thin film resistor.

IV. EXPERIMENTAL RESULTS

Fig. 5 shows the chip photograph of the mixer. The chip size is 550 μm × 450 μm. Building blocks and important pads are indicated in the photograph. The LC balun is placed directly at the RF input, followed by the mixer core.

All measurements have been performed on-wafer with an Agilent HP8970 noise figure meter, Agilent mm-wave source modules HP83557A for 50-75 GHz (V-band) and HP83558A for 75-110 GHz (W-band), GGB GS and SG probes for E-band and noise sources from Noisecom for V- and W-band. At the IF output a GGB GSSG probe and a Mini-Circuits power combiner have been used in order to combine the 0°/180° mixer IF outputs to a single unbalanced signal.

The mixer operates at a supply voltage of -5 V with a total current consumption of 60 mA. The mixer core requires only 6 mA.

In Fig. 6 the measured conversion gain and SSB noise figure versus LO frequency of the mixer at a constant IF frequency of 500 MHz are shown. The LO input power is set to 2 dBm at the center frequency. The center frequency of 78.5 GHz is met at the first design. The measured conversion gain is higher than 24 dB and the SSB noise figure is lower than 14 dB at the frequency range from 72.3 GHz to 82.5 GHz. The mismatch of the mixer RF input and the noise source output result in a ripple seen in the measurement plot. The V-band noise source (frequencies below 75 GHz) exhibits a better match than the W-band noise source (frequencies above 75 GHz).

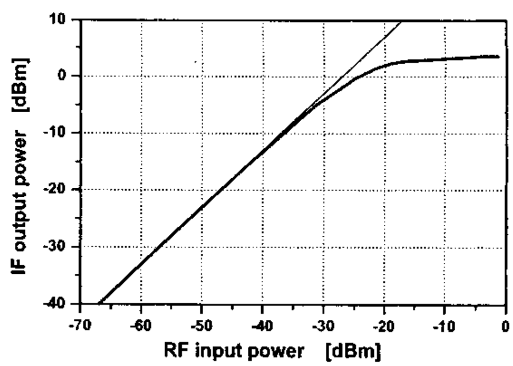

Fig. 7. Measured IF output power versus RF input power. LO frequency is 78.5 GHz, RF frequency is 79 GHz, IF frequency is 500 MHz, LO power is 2 dBm.

In Fig. 7 the measured output power versus input power is shown. The IF frequency is 500 MHz, the LO frequency is 78.5 GHz and the LO power is 2 dBm. The 1 dB compression point is -30 dBm referred to the input and -4 dBm referred to the output. The compression point is dominated by the IF buffer. The IF buffer is included in order to provide a matched intermediate frequency output and it

TABLE I

SUMMARY OF TECHNICAL DATA

Supply voltage	-5.0 V
Supply current	60 mA
Conversion gain	>24 dB (65.0 GHz - 90.8 GHz) >22 dB (65.0 GHz - 94.9 GHz)
SSB noise figure	<14 dB (72.3 GHz - 82.5 GHz) <16 dB (66.5 GHz - 90.0 GHz)
1 dB compression point referred to input / output	-30 dBm / -4 dBm
Technology	0.18 μm / 200 GHz f_T SiGe bipolar
Chip size	550 μm × 450 μm

exhibits a simulated gain of 1.7 dB. So the gain of the complete mixer is dominated by the gain of the mixer core.

Fig. 8 shows the measured conversion gain and SSB noise figure at a fixed IF frequency of 500 MHz and a constant LO frequency of 78.5 GHz as a function of LO power. At lower LO level (<0 dBm), conversion gain and SSB noise figure degrade with decreasing LO power.

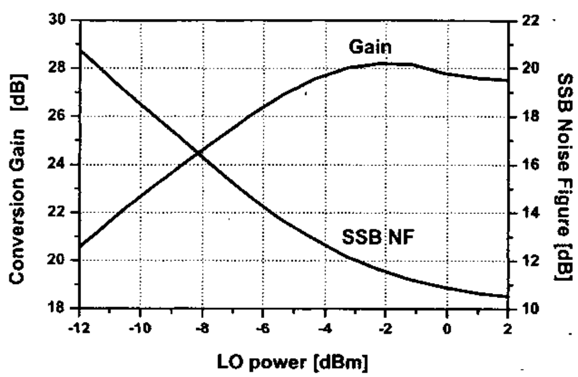

Fig. 8. Measured conversion gain and SSB noise figure versus LO power. IF frequency is 500 MHz, LO frequency is 78.5 GHz.

V. SUMMARY

In this paper an active down-conversion mixer in SiGe bipolar technology has been presented. This mixer exhibits a high gain of more than 24 dB and a low SSB noise figure of less than 14 dB at the highest RF frequencies reported so far for Si-bipolar technologies. So it is demonstrated that SiGe bipolar technology is suited for receiver building blocks of automotive radar systems in the frequency range from 76 GHz to 81 GHz. Tab. I summarizes the technical data of the circuit.

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