An Integrated 17 GHz Front-End for ISM/WLAN Applications in 0.13 μm CMOS

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Student Paper

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Abstract

This paper presents an integrated front-end for ISM/WLAN applications at 17.3 GHz in 0.13 μm standard CMOS. The front-end chip includes an inductive source-degenerated low noise amplifier (LNA), a transformer-based Gilbert-mixer, an intermediate frequency (IF) amplifier and a buffer for the local oscillator (LO) input. The integrated receiver front-end achieves a gain of 34.7 dB, a SSB noise figure of 6.6 dB, an input IP3 of -34.4 dBm and an input 1dB compression point of -39 dBm and consumes only 70 mW at a power supply voltage of 1.5 V.

Introduction

The trend in the world of the wireless communications is going up to research in faster and high-performance radio frequency (RF) circuits. Sub-micron CMOS is particularly attractive for its low power consumption and high degree of integration. An integrated CMOS chip which combines elementary RF building blocks, such as the RF LNA and a down-conversion mixer, is called the front-end for an RF receiver. The front-end of a wireless receiver must observe the standard for the sensitivity. The input noise of the front-end must be sufficiently low to enable it to detect weak input signals. Also the gain of the receiver must be high enough to fulfill the requirements of wide input dynamic range. The purpose of this work is to develop a high gain CMOS receiver front-end operating at frequencies above 5 GHz such as 17.1-17.3 GHz industrial, scientific and medical (ISM) band.

The lower frequency bands (e.g. 2.4 and 5 GHz bands) are being extensively explored for various applications, there are several potentially significant advantages to operation at much higher frequency. One obvious advantage is the larger available bandwidth at high frequencies that is extremely important for wideband wireless communications [1].

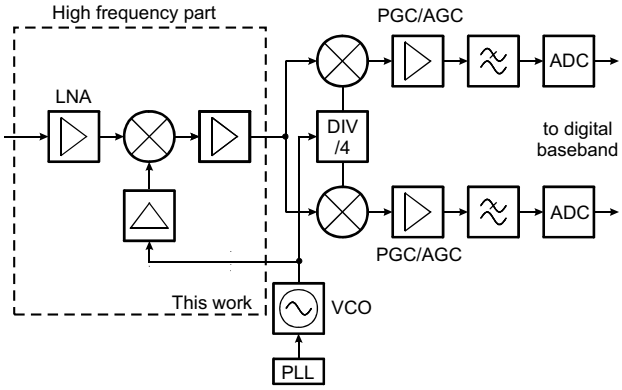

Fig. 1. Block diagram of the presented front-end.

Front-End Architecture

A block diagram of the proposed CMOS front-end is shown in Fig. 1. It consists of a LNA, a transformer-based Gilbert-mixer and an IF amplifier. The concept of the dual conversion shown in the block diagram results in a large frequency separation between the RF and LO frequencies [2] and avoids the generation of I/Q signals at the first LO frequency. This receiver architecture avoids additionally IF filters by using high IF. Also the simple L-C tank from the mixer output is used for IF filtering.

The complete receive chain is fully differential and provides an IF-interface at a much more easy to handle frequency in the range of 3.5 GHz. The LNA and mixer together determine the performance of the front-end. For instance, although a large LNA gain is desirable, too large gain may overload the mixer and compromise dynamic range. On the other hand, the gain must be large enough to overcome the fundamentally higher mixer noise. It is also preferable to connect the LNA in some simple way to the mixer input, without a high power consuming RF buffer circuit.

Circuit Implementation

A. LNA Design

A fully differential common-source type LNA with on-chip inductive degeneration is chosen. LNA-design is one of the main challenges in the front-end design, since this circuit determines the total noise figure of a receiver. The LNA core in Fig. 2 consists of a cascoded, inductively degenerated common source input stage that converts the available power into a current. This topology allows reasonable input matching with a low noise figure at a low power consumption. The inductive degeneration is employed at the common source node of the LNA to achieve a real valued input impedance. The LNA-output is loaded by an integrated LC-tank to improve the gain. In order to get a high quality factor in the LC-tank it is necessary to minimize the total capacitance and maximize the inductance. Therefore the total capacitance seen by the inductor in the circuit is realized by the parasitic capacitance. Furthermore this tank provides a bandpass filter at 17.3 GHz. The integrated series inductors at the input of the LNA improve the input matching and the high-frequency gain in a more robust way compared to external or bond wire matchings. Due to the high frequency of 17 GHz all inductors can nicely be integrated without significant area penalty (see chip photograph Fig. 5).

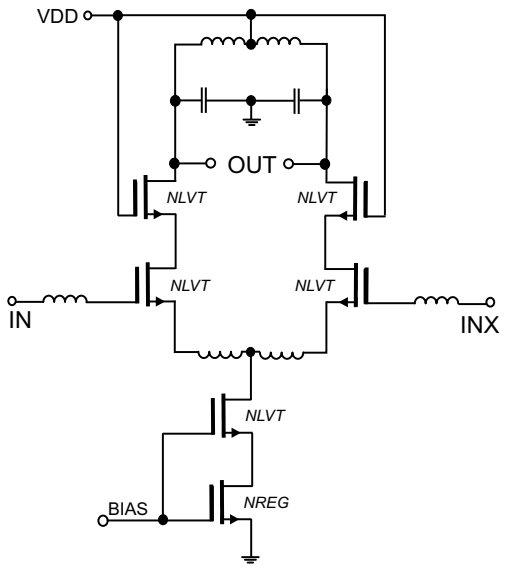

Fig. 2. Simplified schematic diagram of the LNA.

B. Mixer Design

The amplified signal at the LNA output is down-converted to a intermediate frequency of 3.5 GHz for further amplification, filtering and detection. The down-conversion mixer is an integral part of the RF front-end. In Fig. 3 the mixer schematic diagram is presented. The classical Gilbert type mixer [3] was preferred as the best solution to combine acceptable gain, noise figure and linearity. To overcome the problems caused by the low supply voltage of 1.5 V for the 0.13 μm CMOS process, a fully differential integrated transformer [4] was inserted between the input transconductance stage and the switching pairs. Power supply is connected to the center taps of the transformer. This topology effectively doubles the voltage headroom available for the circuit design and enables the insertion of cascode transistors to improve the linearity and to control the current in the mixer switching stage. To achieve the highest coupling between the two stages the transformer should work in resosance. This was realized by inserting two NMOS-capacitancies connected to the primary winding. Due this capacitancies the transformer is tuned to the desired center frequency of 17.3 GHz. Further the mixer is loaded by an integrated LC-tank at 3.5 GHz to enhance the gain and to provide second order bandpass filtering. In order to achieve the maximal inductance the inductor is realized as cross-coupled fully differentail inductor which exploits the coupling factor to increase the inductance per chip area. The total capactinance seen by the the inductor in the circuit is realized with the inherent capacitance of the inductor (inner winding and to substrate) and the capacitance of the connected transistors (drain, gate). Also the parasitics of the interconnections must be considered, especially between two stages. The inductor of the tank circuit consists of a fully

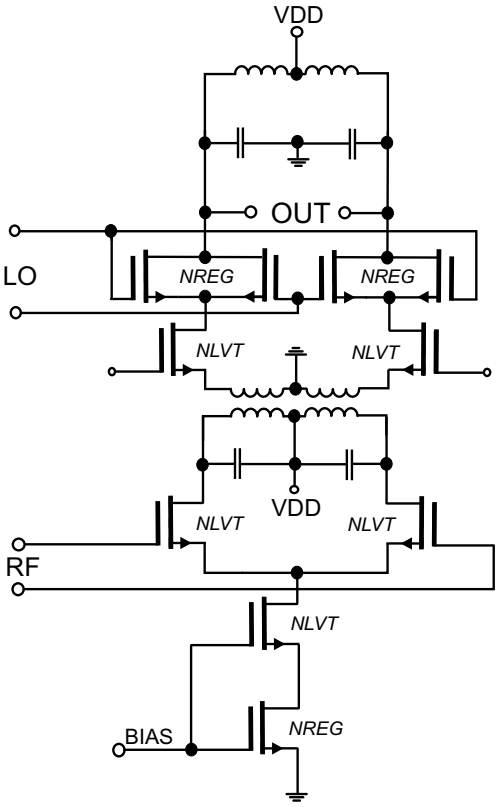

Fig. 3. Simplified schematic diagram of the Mixer.

TABLE I
Receiver front-end performance summary @ 17.35 GHz RF frequency, 13.95 GHz LO frequency and 2 dBm LO input power.

Power supply	1.5 V
Total power consumption	70 mW
LNA power consumption	5.2 mW
Mixer power consumption	27 mW
LO-Driver power consumption	12 mW
IF-Amplifier power consumption	25.8 mW
IF frequency	3.4 GHz
Power Gain	34.7 dB
Noise Figure SSB	6.6 dB
Input compression point	-39 dBm
Input IP3	-34.4 dBm
3 dB Bandwidth	200 MHz
Die Area	0.88mm^2
Technology	0.13 μm standard CMOS

differential integrated 6.6 nH inductor. Fig. 4 shows the lumped double π-model of the used inductor.

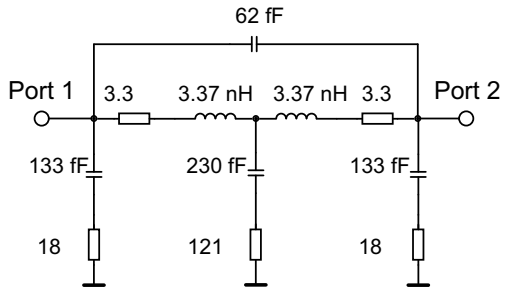

Fig. 4. Schematic of the 6.6 nH inductor.

Experimental Results

The front-end is realized in a standard 0.13 μm six-metal-copper CMOS process of INFINEON [5]. Fig. 5 shows the chip photograph. The die area is 0.88mm^2. The front-end is characterized using chip-on-board mounting. The measurement results, including the parasitics of the bondwires, are summarized in Table I.

All measurements were performed at 1.5 V supply voltage and the total power consumption was 70 mW. The 1dB input compression point was measured for a LO input frequency of 13.95 GHz and a RF input frequency of 17.35 GHz. The single-tone compression measurement result is presented in Fig. 6. The 1 dB input compression point is -39 dBm.

The two-tone intermodulation measurement results are presented in Fig. 7. The distance between the tones of

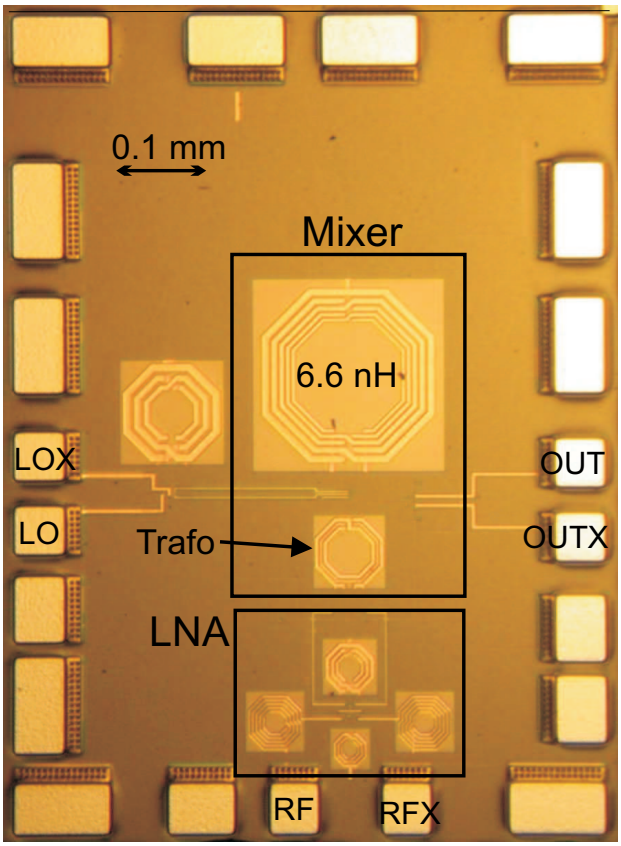

Fig. 5. Receiver front-end chip photograph (Die size 800 μm x 1100 μm)

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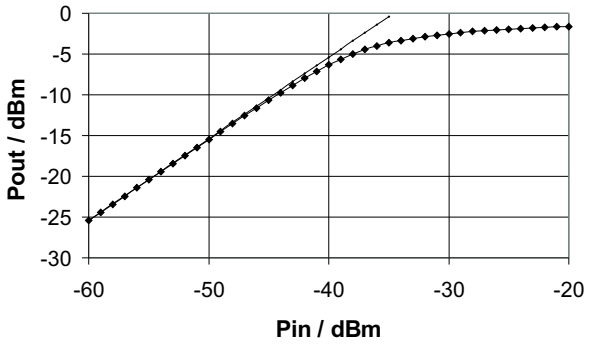

Fig. 6. Measured power transfer characteristic of the receiver front-end.

1 MHz is according to typical wireless LAN applications (IEEE 802.11). The front-end features a measured input IP3 point of -34.4 dBm. Fig. 8 presents the gain measured as a function of the RF input frequency with a LO frequency 3.4 GHz apart. The external LO power is 2

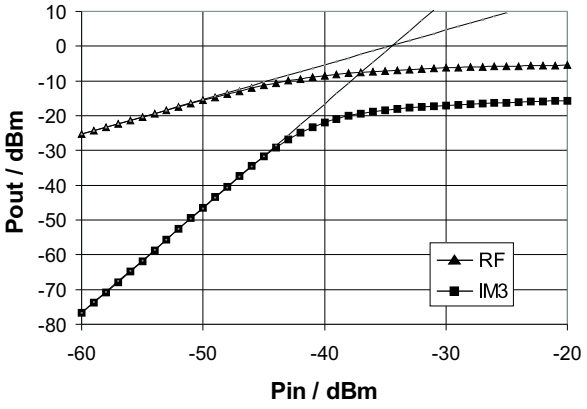

Fig. 7. Measured front-end two tone test, LO 13.95 GHz 2 dBm, RF 17.35 GHz & 17.351 GHz.

dBm. The voltage swing can be easily provided from an integrated VCO [6]. The measurement shows that the maximum power gain of 34.7 dB appears for an RF input frequency of 17.35 GHz and an IF of 3.4 GHz. The measured noise figure is also shown in Fig. 8. The receiver front-end achieves a minimum noise figure of about 6.6 dB at 17.34 GHz.

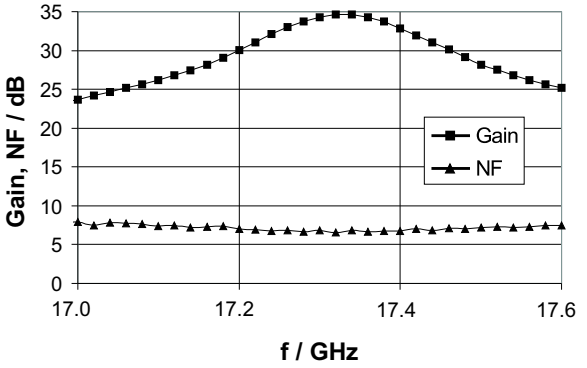

Fig. 8. Gain and noise figure over frequency at a fixed IF frequency of 3.4 GHz.

Conclusions

An integrated high gain CMOS receiver front-end for wireless applications at 17 GHz is presented. The front-end aims at a fully integrated dual-conversion quasi-homodyne receiver. The presented front-end features a gain of 34.7 dB, a SSB noise figure of 6.6 dB, an input IP3 of -34.4 dBm and an input 1 dB compression point of -39 dBm at a power consumption of only 70 mW from a 1.5 V supply voltage. The 3 dB-bandwidth is 200 MHz at a center frequency of 17.34 GHz.

TABLE II
Overview of recently published front-ends.

	[1]	[7]	This work
Total Power consumption	64.5 mW	62.5 mW	70 mW
Power Gain	27.5 dB	17.3 dB	34.7 dB
Noise Figure	7.7 dB	6.5 dB (SSB)	6.6 dB (SSB)
Frequency	24 GHz	17 GHz	17 GHz
Technology	0.18 μm CMOS	100 GHz-f_T BiCMOS	0.13 μm CMOS

Table II shows an overview of recently published integrated front-ends. This work in standard 0.13 μm CMOS features a similar performance as the circuit in 100 GHz-f_T SiGe BiCMOS technology.

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