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TIME-RESOLVED ANALYSIS OF SELF-HEATING IN POWER VDMOSFETs USING BACKSIDE LASERPROBING

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Abstract A laserprobe technique for characterization of transient self-heating in power devices is proposed and its applicability is demonstrated on VDMOSFETs. The change in the silicon lattice temperature in the device active region under pulsed operation is sensed by an infrared laser beam focused on a single VDMOS cell from the substrate side. The temperature-induced change in the silicon refractive index causes an optical phase change which is detected interferometrically. The transient phase measurements are carried out under various VDMOSFET bias conditions and for heating pulse widths in the μs range. The laser beam modulation is numerically modeled using a solution of the transient heat transport equation and a transmission line approach to model the beam propagation. Calculated optical phase signals show a very good agreement with the experiments. The phase change calculated by using a simple geometric optic approximation was compared with the phase variation obtained by the rigorous transmission line approach. The results show that the geometric optic approach can accurately be used in the analysis of transient self-heating of VDMOSFETs. © 1997 Elsevier Science Ltd.

1. INTRODUCTION

The steady increase in the switching frequency of power devices under high voltage and current conditions causes transient thermal effects to become a more severe and critical issue[1]. Typically, if the chip temperature exceeds a critical value, thermal runaway may cause destruction of the device. These thermal effects occur in the ms-to-second time scale involving package and heat sink conditions[2,3]. However, critical operation conditions like switching, commutation, suddenly shorted load or turn-off of inductive loads may cause destructive thermal effects in the μs range. A local temperature increase in the device can trigger a second breakdown, latch-up and turn-on of parasitic thyristors and transistors in power MOSFETs[4,5], bipolar transistors and insulated gate bipolar transistors[6,7]. These effects are studied widely but yet not fully understood, not least because appropriate temperature measurement techniques are not available.

Various experimental techniques for thermal analysis of semiconductor devices, such as infrared emission spectroscopy[8,9], liquid crystal mapping[10] and fluorescent microthermal imaging[11] were introduced. These methods suffer, however, from insufficient time resolution and some of them are invasive. In contrast, novel techniques based on infrared laser probing provide a large dynamic range and a spatial resolution limited by the laser wavelength[12]. Time resolved reflectivity[13] and laser deflection spectroscopy[14] were used to characterize temperature changes in devices. The backside laserprobing introduced by Heinrich *et al.*[12] senses the modulation of a laser beam focused on the device active area from the substrate side caused by changes in the refractive index of the semiconductor resulting from plasmaoptical, thermooptical and electrooptical effects. This technique was applied to study the free-carrier modulation in devices[12,15,16] and ICs operating up to GHz frequencies[17].

In this contribution we report on a study of transient self-heating in VDMOSFETs using a backside laserprobe technique introduced in Ref. [18]. After the sample and method description, measurements of the time evolution of the optical phase signal and the electrical characterization are presented in Section 2. Numerical modeling of the temperature distribution and optical phase signal is given in Section 3, where also results of simulation and experiment are compared. Finally, these results are summarized.

2. EXPERIMENTS

2.1. Sample description

Commercially available VDMOSFETs with 150 V and 200 V voltage rating[19] are studied. The devices consist of several hundred hexagonal VDMOS cells (Fig. 1) arranged in a hexagonal geometry and are packaged in a standard TO-126 package. In order to access optically the substrate of the device, the package was opened and the drain contact removed mechanically by grinding, followed by substrate polishing. A new electrical drain contact was evaporated (Ti–Au) leaving a small optical window

($100\,\mu m \times 100\mu m$) opened in the center of the chip. The electrical characteristics of the devices were not influenced by this procedure, except for an increase in the series drain contact resistance (of about 0.5Ω), which was taken into account in numerical modeling. As will be shown later, the thermal properties of the device in the μs time scale were not changed by sample preparation.

2.2. Basic principles

The measurement of the transient temperature changes is based on detecting the changes in the complex refractive index of silicon $\bar{n} = n - ik$ with the temperature, where n and k are the real and imaginary part of the refractive index, respectively. An increase in the lattice temperature of ΔT induced by power dissipation in the device increases the real part n of the refractive index by Δn;

$$\Delta n(\Delta T) = \frac{dn}{dT} \cdot \Delta T, \tag{1}$$

where dn/dT is the temperature coefficient of the refractive index ($dn/dT \simeq 1.5 \times 10^{-4}K^{-1}$ for silicon at room temperature[20]). This refractive index change modulates the phase of an infrared laser beam propagating through the active region of the device, which is interferometrically detected. The photon energy of the laser beam ($\lambda = 1.31\,\mu m$) is well below the band gap of silicon, thus the optical measurements are noninvasive. In our heterodyne interferometer set-up[18] the laser beam is split into two beams where a probe beam is focused on a single MOSFET cell through the window in the drain contact (Fig. 1) and a reference beam is placed on the drain metallization about $70\,\mu m$ apart from the probing beam. As the reflectivity of the drain metallization does not change during the measurement, this provides a good interferometric reference. The diameter of the focused laser beam used in this study is approximately $8\,\mu m$, which gives sufficient spatial resolution for this study (see Section 3.1). The theoretical limit for the spatial resolution, however, would be 0.4λ ($\approx 0.5\,\mu m$) in silicon, if a microscope objective with high numerical aperture (NA = 1.3) is used[21]. The probing and the reference beams reflected from the polysilicon gate and the evaporated drain contact, respectively, interfere in the photodetector. The noisy detector output signal is filtered, averaged and displayed on a digital oscilloscope. The temporal resolution of the present experimental set-up is $0.8\,\mu s$, as determined by the bandwidth of the detection unit but not by the method itself.

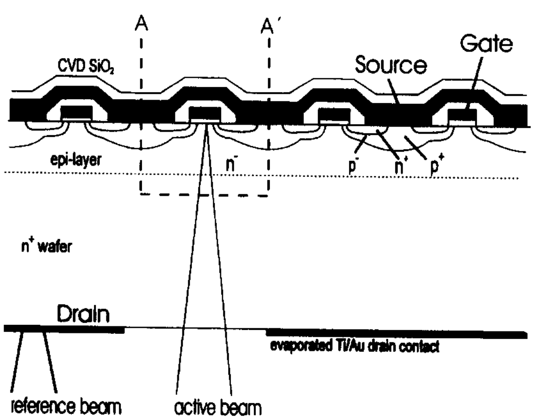

Fig. 1. Schematic view of the cell-like structure of VDMOSFET with the probing laser beam and the reference beam. Device electrical modeling was carried out in the two half-cells area between the lines A–A'.

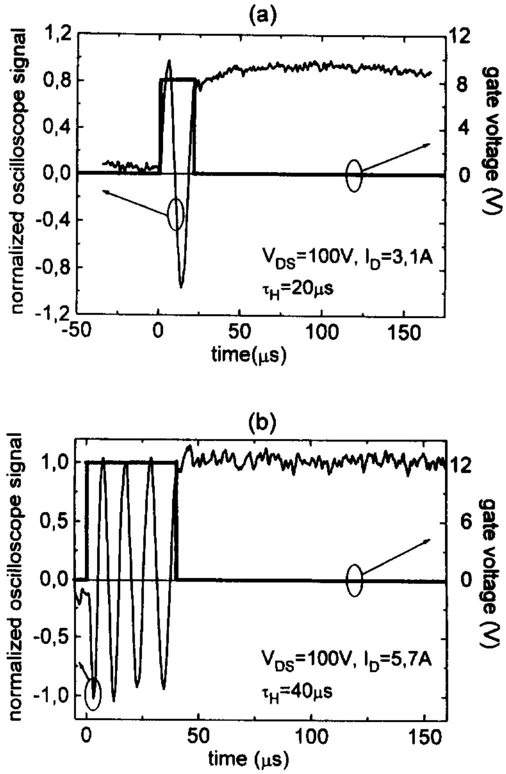

Fig. 2. Oscilloscope signal obtained from a laserprobe experiment on VDMOSFET. The device is biased at constant $V_{DS} = 100$ V, gate pulses are applied of width (a) $\tau_H = 20\,\mu s$ ($V_{GS} = 0$ to 8 V) and (b) $\tau_H = 40\,\mu s$ ($V_{GS} = 0$ to 12 V).

The oscilloscope signal $y(t)$ holds information on the phase change $\Delta\phi(t)$ and can be expressed as[18];

$$y(t) = A \sin[\Delta\phi(t)], \tag{2}$$

with A being the amplitude of the signal. For small $\Delta\phi$ the approximation $\Delta\phi(t) \approx y(t)/A$ may be used as usually assumed[12,18], while for large $\Delta\phi$ as in this study $\Delta\phi(t) = \arcsin(y(t)/A)$ has to be used. A typical oscilloscope signal obtained from laserprobing of a VDMOSFET biased under two different conditions is shown in Fig. 2. This example manifests a large temperature measurement range of the laserprobe technique: For large values of $\Delta\phi$ multiple transitions in the sinusoidal signal are resolved. To obtain the time dependent phase change from the measured signal, eqn (2) has to be used.

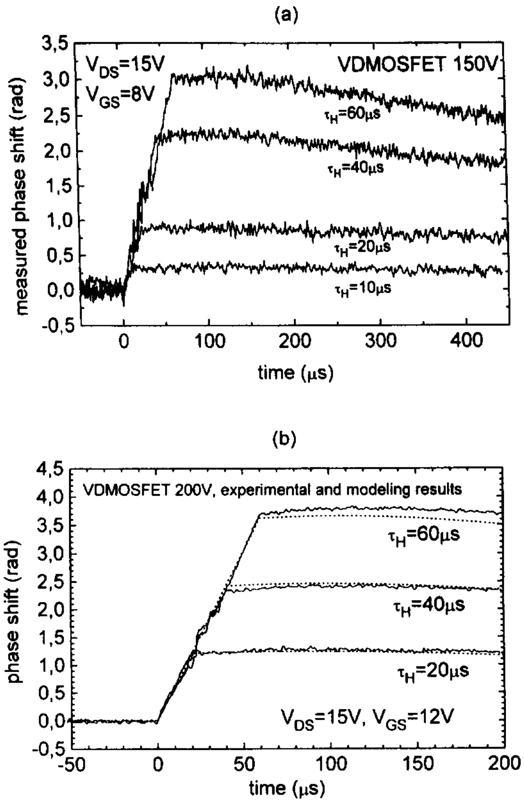

Fig. 3. Time dependence of the optical phase change with the pulse width τ_H as parameter for two device types; (a) 150 V, (b) 200 V (solid lines, experiment; dotted lines, modeling result with $dn/dT = 1.6 \times 10^{-4}\ K^{-1}$). The calculation results are only shown for the 200 V device.

The phase change can be estimated assuming a homogeneous temperature increase $\Delta T(t)$ over the modulation region of depth L (a region where the temperature increase is significant)[12];

$$\Delta\phi(t) = 2\frac{2\pi L}{\lambda}\frac{dn}{dT}\Delta T(t), \tag{3}$$

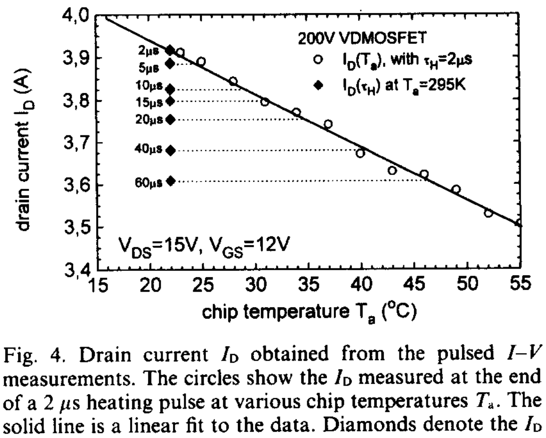

Fig. 4. Drain current I_D obtained from the pulsed I–V measurements. The circles show the I_D measured at the end of a 2 μs heating pulse at various chip temperatures T_a. The solid line is a linear fit to the data. Diamonds denote the I_D measured at chip room temperature for varying pulse widths. The intersections of the dotted lines and the solid line determine the channel temperature increase.

where the factor 2 on the right hand side arises from the two-way passage of the probe beam through the modulated region. Note that in the case of an inhomogeneous temperature distribution over the modulation region ($\Delta T(t)$ is a function of the depth), the $\Delta T(t)$ function has to be integrated over the beam path;

$$\Delta\phi(t) = 2\frac{2\pi}{\lambda}\int_L \frac{dn}{dT}\Delta T(t)\,dl. \tag{4}$$

The latter approximation is referred in the following as the geometric optic approach.

It should be noted that the change in the temperature also causes a change in the imaginary part k of the refractive index, as given by Kramers–Kronig relations[22]. Since the absorption in this spectral region is very small ($k \approx 10^{-7}$)[23–25], this effect on the measured signal (amplitude A in eqn (2)) is negligible. Besides lattice temperature changes in the refractive index, the laser beam is additionally modulated by the free carrier (plasma optical)[22] and electric field effects[26]. These effects are also negligible in our measurements. This was verified experimentally by biasing VDMOSFET in such a way that heating vanishes; the gate-to-source bias is varied, while the drain-to-source bias is set to $V_{DS} = 0$ V. The electron and hole concentrations in a VDMOS cell are modelled using MINIMOS 6[19]. The obtained carrier concentrations are used to calculate the free-carrier induced phase change (see Appendix). For bias conditions $0 \leqslant V_{GS} \leqslant 14$ V and $0 \leqslant V_{DS} \leqslant 15$ V the calculated phase change is less than 4×10^{-4} rad. Further, laser beam modulation caused by the thermal expansion of the silicon lattice was neglected in this study, since this effect is small with respect to the effect of the temperature change in the refractive index. Accounting for the thermal expansion, the total phase change becomes;

$$\Delta\phi = 2\frac{2\pi}{\lambda}\left[L\frac{dn}{dT}\Delta T + n\frac{dL}{dT}\Delta T\right]. \tag{5}$$

Taking literature values for the thermal expansion coefficient $dL/(L\,dT)$[27] and the temperature coefficient of the refractive index of silicon[20] the error induced by neglecting the thermal expansion is about $[n\,dL/dT]/[L\,dn/dT] \approx 6\%$.

The amount of dissipated heat in VDMOSFET chip was varied by changing the width τ_H of the gate pulses. We applied gate pulses V_{GS} from 0 V to 8 V (saturation) and from 0 V to 12 V (quasi-saturation device operation), with constant $V_{DS} = 15$ V. The pulse period was long enough ~100 ms) to ascertain total cooling of the device between succeeding pulses. This was verified by monitoring the steady-state temperature of the VDMOSFET package by a sensor. For pulsed I–V measurements, the chip temperature was controlled by a thermochuck in the 22 to 55°C range. The drain current variation was obtained by monitoring the voltage drop across a drain shunt resistor.

2.3. Experimental results

All the optical experiments were carried out at room temperature. Figure 3(a) shows a time dependence of the optical phase of a 150 V device with the gate pulse width τ_H as parameter. A comparable result obtained on a 200 V VDMOSFET is shown in Fig. 3(b). Two regions in the phase signal can be found; (1) a nearly linear increase during the heating and (2) a region with an almost constant signal followed by a slow decrease after the gate pulse turn-off. The nearly constant signal can be explained by considering the detected phase shift is proportional to the integral of the temperature difference $\Delta T(t)$ over the length of the modulation region. Although the lattice temperature gradually decreases after the heating turn-off, the length of the modulation region further increases due to heat conduction into the bulk. Therefore, the integral over the modulation region is roughly constant. A detailed analysis of the experimental signal shows that it slightly increases, reaches a maximum and then slowly decreases. This effect will be explained in Section 3. Finally, at longer times the signal decrease is caused by heat removal through the bottom drain contact due to heat propagation and cooling.

In order to confirm the temperature values resulting from numerical modeling, pulsed I–V measurements were performed to extract the channel temperature at various pulse widths (Fig. 4). The channel temperature is obtained from a comparison of two types of pulsed I–V measurements;

(i) The chip temperature T_a is externally varied and the gate pulse width is maintained short (2 μs). Under these conditions the self-heating is small and the drain current I_D is fully determined by the known chip temperature T_a.

(ii) The chip is kept constant at room temperature and the drain current at the end of the heating pulse is measured as a function of the pulse width. The drain current change is used for the estimation of the lattice temperature near the Si/SiO_2-interface using the I_D–T curve obtained in measurements (i), as shown in Fig. 4.

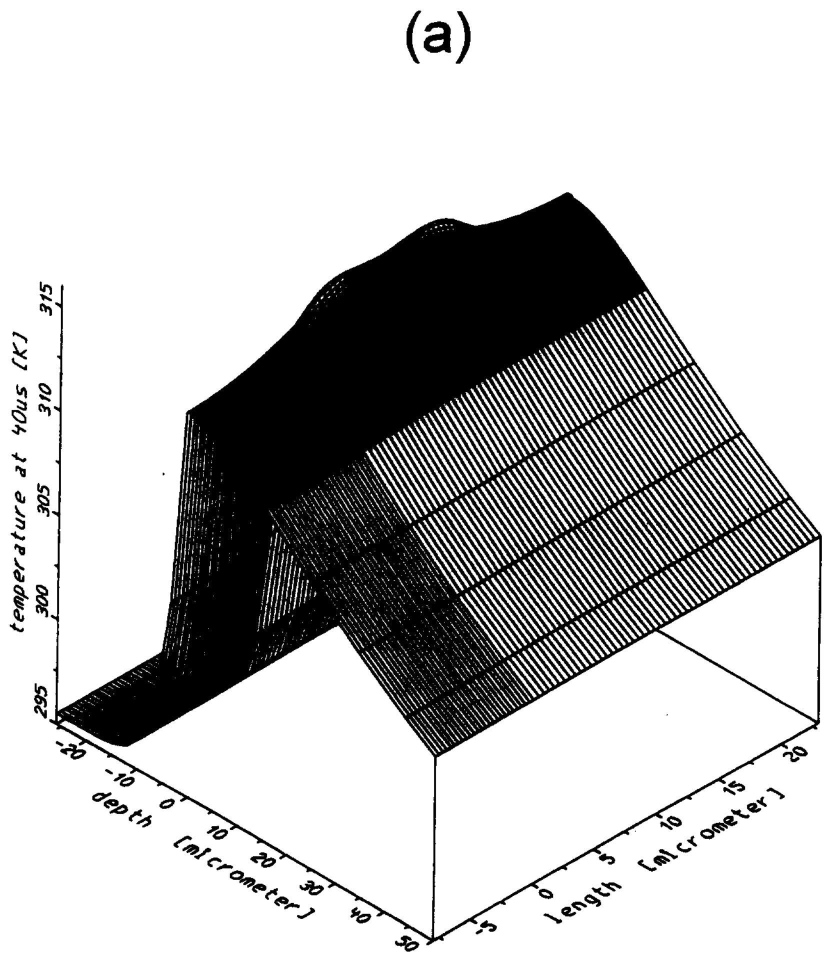

Fig. 5a.

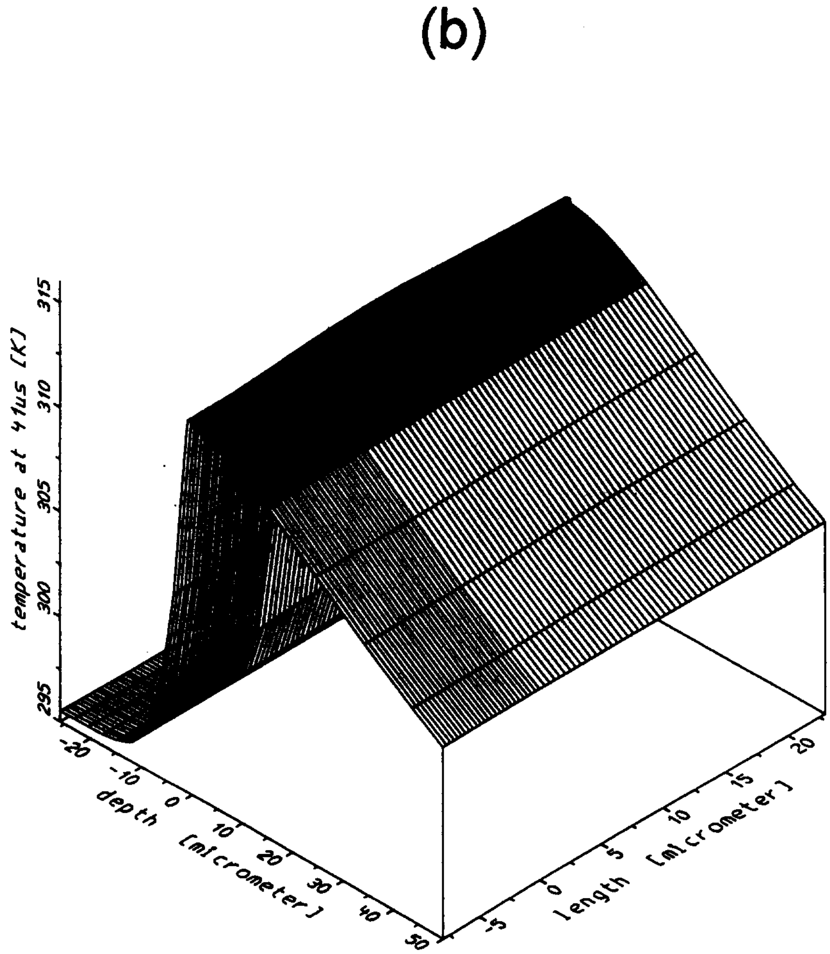

Fig. 5. Numerical modeling result for the temperature distribution across two half VDMOSFET cells (the A–A′ area in Fig. 1): (a) at the end of the heating interval τ_H, and (b) 1 μs after the gate turn-off. Pulse width $\tau_H = 40$ μs, $V_{GS} = 8$ V, $V_{DS} = 15$ V, 150 V device. The polysilicon gate edges are placed at 0 and 15 μm. The p^-/n^--junction at the Si/SiO$_2$ interface (depth = 0) is located at 2.5 and 12.5 μm. The epitaxial layer thickness is 15 μm.

3. NUMERICAL MODELING

3.1. *Modeling of heat conduction*

The study of time dependence of the temperature in VDMOSFET requires modeling of the total chip consisting of several hundred cells including the chip package. To reduce the complexity of the model, we first analysed the temperature distribution in a single VDMOSFET cell. The electrical characteristics of a single cell are calculated by a modified version of MINIMOS 6[28] using the simulated doping profile from[19]. A 2-D numerical simulator is then used to solve the transient heat conduction equation considering Joule heat as the dominant term for heat dissipation[29]. The voltage drop across and the power dissipated in the n^+-substrate are neglected because of high substrate doping. As a result of the symmetry in the thermal modeling of a single cell in the chip center, we assume no heat flow across neighbouring cells. Figure 5(a) shows results for the temperature distribution in the two half cell area A–A′ (Fig. 1) at the end of the heating pulse τ_H. A small temperature increase in the channel region with respect to the epi-region can be seen for the analysed operation point in the saturation. This inhomogeneity vanishes immediately (1 μs) after turn off (Fig. 5(b)) because of the high thermal conductivity of silicon[30]. For the purpose of modeling the phase modulation, this temperature inhomogeneity within the cell can be neglected. As the channel depth is small compared to the depth of the epitaxial layer the additional temperature-induced phase change arising from the channel region is very small. Therefore, the heat generation in the cell structure of the VDMOS chip may be replaced by a homogeneous heat generation within the epitaxial layer (Fig. 6). Under these conditions, lateral temperature variations in the cell cannot be resolved allowing us to use a microscope objective with relatively small spatial resolution. The total heat generation $H(t)$ within the epitaxial layer is calculated from

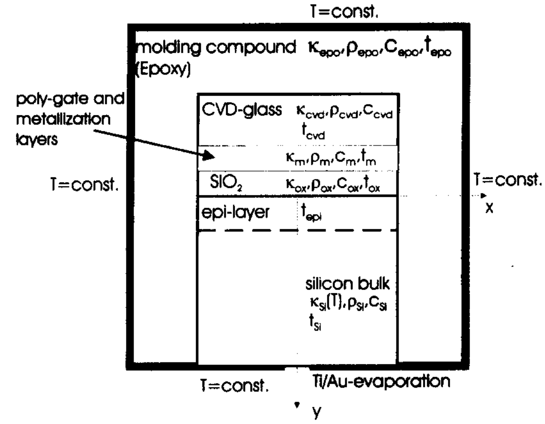

Fig. 6. Simplified structure of the VDMOSFET chip including the package used for 2-D numerical thermal modeling; $\kappa(T)$, ρ, c and t are the thermal conductivity, the mass density, the specific heat and the layer thickness, respectively. The origin of y-coordinate is at SiO_2-interface.

$H(t) = [V_{DS} - R_D I_D(t)] \cdot I_D(t)$, where R_D being the series drain contact resistance and $I_D(t)$ is the measured current. The 2-D heat conduction equation is then solved over the whole chip area including the package. The temperature is considered to be constant at the package-air interfaces and at the drain contact-air interface (Fig. 6). The latter approximation is valid as long as the heat front does not reach the bottom contact (this holds for times less than about 150 μs). Consequently, for the heating intervals applied ($\tau_H \leqslant 60\ \mu$s) the boundary conditions at the drain contact altered by the preparation have no influence on the temperature increase in the device active region. From the calculated 2-D temperature profiles within the VDMOSFET chip we have found that the temperature in silicon along the length (x-axis in Fig. 6) is nearly uniform which allows the reduction of the 2-D heat conduction problem to an 1-D model. A set of typical transient temperature profiles across the chip center at various time instants is shown in Fig. 7. The calculated temperature near the Si/SiO_2-interface is close to the values obtained by pulsed I–V measurements (Fig. 4). For example, for a heating pulse width of $\tau_H = 60\ \mu$s

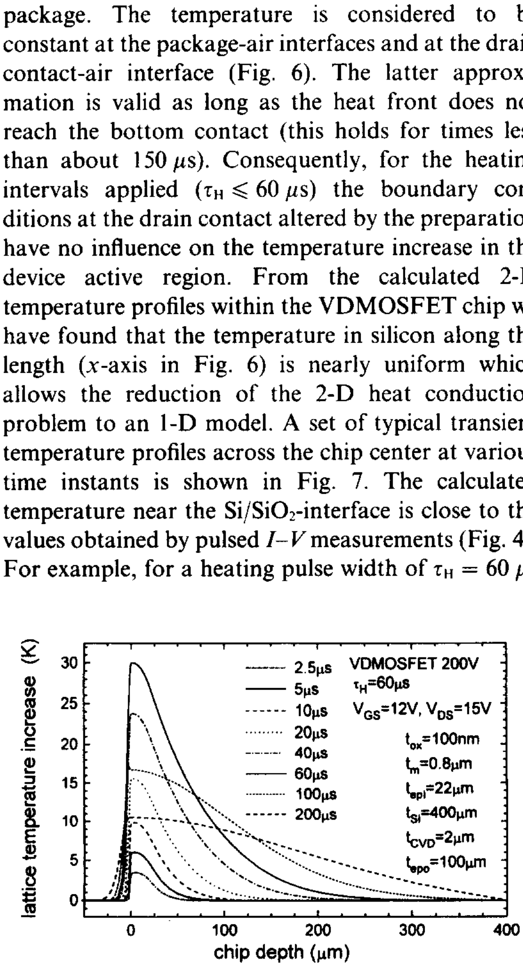

Fig. 7. Calculated 1-D temperature profile across the chip center at different time instants for a heating pulse of 60 μs.

in Fig. 7, the temperature increase in the channel after 20 μs is about $\Delta T = 12$ K, which is in agreement with 12.5 K extracted from the pulsed I–V measurement (Fig. 4). The 1-D temperature profiles are further used as input for the calculation of the laser beam modulation.

3.2. Modeling of laser beam modulation

To calculate the phase change in the laser beam a transmission line approach is applied[31]; computation details can be found in Appendix. The refractive index profile used in modeling was calculated from the 1-D temperature profile by using eqn (1). The coefficient dn/dT was taken as a fitting parameter so that the experimental and calculated phase match at the end of the heating pulse. The values of dn/dT obtained from altogether 32 measurements on different devices under different pulse widths (from 5 to 60 μs) and biasing conditions are grouped around the mean value of $1.6 \times 10^{-4}\ K^{-1}$ with a standard deviation of $1.4 \times 10^{-5}\ K^{-1}$. This result is very consistent with the literature values of $1.5 \times 10^{-4}\ K^{-1}$[20], $1.9 \times 10^{-4}\ K^{-1}$[32], $1.8 \times 10^{-4}\ K^{-1}$[33] and $1.4 \times 10^{-4}\ K^{-1}$[34]. The measured and calculated phase signals show a good quantitative agreement in the first 150 μs (Fig. 3(b)). The difference in the slope of the calculated phase signal for larger times is most likely caused by a drain contact thermal resistance which was neglected in modeling. The small increase in the phase signal immediately after pulse turn-off originates from the heat stored in the gate and passivation CVD-glass layers and the subsequent heat back-transfer into the silicon.

It was found that the phase change obtained from the rigorous numerical transmission line model is very close to that calculated from the temperature profile using the geometric optic approach (Section 2.2). This can be explained by the fact that the modulation region is of the order of several wavelengths ($L \gg \lambda/n$) and accordingly, the wave nature of the laser beam has a minor influence on the modulation signal. The wave nature is, however, important in cases of a modulation layer depth of few nm (like the inversion and accumulation layer in conventional MOSFETs[35]), where the transmission line model must be applied. The geometric optic approach can additionally be used for estimation of the temperature in the device active area during the heating pulse. Provided that the effective thickness of the modulation region is known, the temperature change can directly be calculated from the measured phase change using eqn (3).

4. CONCLUSION

The backside laserprobing technique was used successfully to characterize transient self-heating in power VDMOSFETs. The thermooptical effect is found to be dominant over the plasmaoptical and electrooptical effects. If the probing beam is positioned in a VDMOSFET cell located in the center of the chip, the thermal analysis for thermooptical modeling can be reduced from 3-D to 1-D case. Moreover, the geometric optic approach is found to be sufficiently accurate, resulting in beam modulation signals which agree well with the transient phase signals obtained from experiments. As the backside laserprobing technique provides a large temperature range and a high temporal resolution of measurements, we propose that this method can be used for the study of critical thermal phenomena in power devices in the μs time scale.

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APPENDIX

The laser beam modulation is calculated by a model derived from the transmission line theory[36]. Starting from the Si/SiO_2-interface the silicon is divided along the chip depth (perpendicular to the beam propagation) into $n_y - 1$ segments of widths Δy_j, $j = 1, \ldots, n_y$. A constant complex refractive index $\bar{n}_j$ is assumed in a particular segment. The thermooptical effect, the free-carrier (plasma-optic) effect and the electric field effect induce local perturbation of the real and imaginary part of the refractive index Δn_j and Δk_j within each segment. The thermally induced change Δn_j is calculated from the temperature profile across the chip depth; $\Delta n_j = \mathrm{d}n/\mathrm{d}T\Delta T_j$, where ΔT_j is the temperature increase in the j-th segment. The free-carrier induced change in the refractive index is computed using the classical and modified Drude model[22,31] and the electric field dependence is according to[22].

The complex refractive index $\bar{n}_j$ and the wave impedance $\bar{Z}_{w,j}$ for a TEM (transverse electromagnetic) wave propagating perpendicular to the segments can be expressed by;

$$\bar{n}_j = n_j - ik_j \tag{A1}$$

$$n_j = n_0 + \Delta n_j \tag{A2}$$

$$k_j = k_0 + \Delta k_j \tag{A3}$$

$$\bar{Z}_{w,j} = \sqrt{\frac{\mu_0 \mu_r}{\epsilon_0}} \cdot \frac{1}{\bar{n}_j},\ j = 1, \ldots, n_y \tag{A4}$$

where n_0 is the pure silicon refractive index and k_0 the extinction coefficient at room temperature, the μ_0 and ϵ_0 are the permeability and the permittivity of vacuum, respectively, and $\mu_r = 1$ is the relative permeability of silicon. Since for the wavelength of the laser beam of $\lambda = 1.31\ \mu$m the extinction coefficient is negligibly small[23–25], we may set $k_0 = 0$.

Application of the transmission line theory gives for the load impedance $\bar{Z}_{c,1}$, of the first silicon layer;

$$\bar{Z}_{c,1} = \bar{Z}_{ox} \cdot \frac{\bar{Z}_{poly} + \bar{Z}_{ox} \cdot \tanh(\bar{\gamma}_{ox} t_{ox})}{\bar{Z}_{ox} + \bar{Z}_{poly} \cdot \tanh(\bar{\gamma}_{ox} t_{ox})}, \tag{A5}$$

where $\bar{\gamma}_{ox}$ and t_{ox} are the gate oxide wave number and the gate oxide thickness, $\bar{Z}_{ox}$ and $\bar{Z}_{poly}$ are the wave impedance of the gate oxide and the polysilicon gate, respectively.

The load impedance $\bar{Z}_{c,j}$ of silicon layer j is;

$$\bar{Z}_{c,j} = \bar{Z}_{w,j} \cdot \frac{\bar{Z}_{c,j-1} + \bar{Z}_{w,j} \cdot \tanh(\bar{\gamma}_j \Delta y_j)}{\bar{Z}_{w,j} + \bar{Z}_{c,j-1} \cdot \tanh(\bar{\gamma}_j \Delta y_j)}, \qquad (A6)$$

where $\bar{Z}_{c,j-1}$ is the load impedance of preceding layer $j-1$, and the wave number γ_j for each segment is written as;

$$\bar{\gamma}_j = \frac{2\pi}{\lambda} \cdot [k_j + i \cdot (n_0 + \Delta n_j)]. \qquad (A7)$$

Denoting $\bar{Z}_C$ the total wave impedance at the bottom of the considered silicon region and $\bar{Z}_W$ the wave impedance of the medium surrounding the silicon (air, etc.), the complex reflection coefficient ρ for the laser beam propagating through the substrate is calculated as;

$$\bar{\rho}(t) = \frac{\bar{Z}_C - \bar{Z}_W}{\bar{Z}_C + \bar{Z}_W}. \qquad (A8)$$

In measurements, the transient phase signal represents the phase change between two conditions in the device (e.g., between heating $V_G \neq 0$ V and no heating $V_G = 0$ V). In modeling, the phase signal is derived from the reflection coefficients $\rho(t)$ for the active (e.g. heat dissipation, inversion conditions) and ρ_{ref} for the inactive device operation state, respectively;

$$\Delta\phi(t) = \arg[\bar{\rho}(t)] - \arg[\bar{\rho}_{ref}]. \qquad (A9)$$

In the geometric optic approximation the phase signal is simply given by a discretization of eqn (3);

$$\Delta\phi(t) = 2\frac{2\pi}{\lambda} \sum_{j=1}^{n_y} \Delta n_j(t) \cdot \Delta y_j \qquad (A10)$$