Solid-State Electronics 125 (2016) 118–124

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Effect of barrier recess on transport and electrostatic interface properties of GaN-based normally-off and normally-on metal oxide semiconductor heterostructure field effect transistors

M. Capriotti [a,*], E. Bahat Treidel [b], C. Fleury [a], O. Bethge [a], C. Ostermaier [c], M. Rigato [a], S.L.C. Lancaster [a], F. Brunner [b], H. Detz [a], O. Hilt [b], J. Würfl [b], D. Pogany [a], G. Strasser [a]

[a] Vienna University of Technology, Floragasse 7, A-1040 Vienna, Austria
[b] Ferdinand-Braun-Institut, Gustav Kirchhoff Sraße 4, D-12489 Berlin, Germany
[c] Infineon Technologies Austria AG, Siemensstraße 2, A-9500 Villach, Austria

ARTICLE INFO

Article history:
Available online 18 July 2016

The review of this paper was arranged by Jurriaan Schmitz

ABSTRACT

We perform a comprehensive electrical transport and physical characterization of metal oxide semiconductor heterostructure field effect transistors with ZrO_2 gate dielectrics, having partially (referred here as MOS-HFET) and fully (here called true-MOS-FET) recessed GaN/AlGaN/GaN barrier, giving normally-on and normally-off behavior, respectively. The mobility of the MOS-HFETs decreases with the proximity of the Coulomb scattering centers, situated at the ZrO_2/AlGaN interface. The effect of the etching procedure and ZrO_2 deposition on the formation of the interfacial charges, N_{int}, is evaluated by X-ray Photoelectron Spectroscopy and by fitting the threshold voltage values to numerical model. For the both device types, the extracted value of N_{int} lies within 15% around 2.8×10^{13} cm^{-2}, which is of the order of polarization charge, showing that our low-damage three step etching procedure does not introduce extra interface states.

1. Introduction

III-N based power devices are promising candidates for the post silicon power electronics market. For efficient and safe power switching, reliable normally-off operation is required [1]. Several normally-off device concepts have been proposed, for example: p-type gate, fluorine implantation and barrier recessed Metal Oxide Semiconductor Heterostructure Field Effect Transistors "MOS-HFETs" [2–4]. These concepts are all based on the local depletion of the 2DEG in the gate region. Among all, MOS-HFETs are particularly attractive because of the inclusion of an insulator layer between the gate metal and III-N layers, effectively reducing the gate leakage current I_g and extending the maximum gate voltage overdrive V_{over} [5]. The carrier mobility of these devices is high due to separation of the 2DEG and scattering centers [6]. However the inclusion of an insulating layer introduces unwanted features, such as a recoverable threshold voltage V_{th} drift toward positive values under forward biasing and a stable negative V_{th} shift that is proportional to the dielectric layer thickness t_{diel}, due to positive charges at the AlGaN/dielectric interface [7–11]. The latter hinders other efforts to obtain a positive V_{th} with MOS-HFETs. This negative shift can be partially reduced using high-k dielectrics, such as ZrO_2, but additional strategies are needed to further increase V_{th}. On the other hand, although theoretical models for the III-N barrier thickness scaling of V_{th} [12] and channel mobility exist [6], there is a lack of experimental barrier scaling studies in MOS-HFETs in gate-recessed devices, which take into account the effect of the barrier etching.

One of the most promising approaches consists of the full recess of the III-N barrier layer below the gate contact prior to oxide deposition. In contrast to partially recessed MOS-HFETs, in the full barrier recess approach the electron channel below the gate is formed directly at the III-N/dielectric interface, similar to a True Metal Oxide Semiconductor (MOS) Field Effect Transistor. The "True-MOS" approach grants higher threshold voltages, while preserving most of the advantages of the conventional MOS-HFETs [13–16]. Although high performance True-MOS have been recently demonstrated, this device concept still suffers from a strong decrease in the maximum output current $I_{d,max}$ compared to equivalent MOS-HFET structures. This is mainly due to a strong increase in the channel resistance R_{ch}. The electron mobility considerably drops beneath the gate, due to the loss of the two-dimensional

* Corresponding author at: Infineon Technologies Austria AG, Siemensstraße 2, A-9500 Villach, Austria.
E-mail address: mattia.capriotti@infineon.com (M. Capriotti).

http://dx.doi.org/10.1016/j.sse.2016.07.009
0038-1101/

electron gas (2DEG) at the AlGaN/GaN heterojunction [17]. We have recently presented threshold voltage, V_{th}, and fixed interface charge, N_{int}, analysis in fully recessed True-MOS GaN FET device exhibiting positive threshold voltage and compared its characteristics to Schottky barrier gate HFET device and MOS-HFET device with additional ZrO_2 gate dielectrics, both prepared on the same heterostructure material [18].

In this contribution, we complete and enhance our previous work by additional analysis of MOS-HFET devices with partially recessed GaN/AlGaN barrier providing thus a comprehensive picture of these devices in respect to III-N barrier thickness scaling, i.e. from non-recessed, via partially-recessed MOS-HFETs, up to fully recessed True-MOS. In addition to electrostatic analysis (i.e. V_{th} and fixed interface charge) [8–10] of conventional short channel FETs, we also investigate the carrier mobility for different gate recess conditions using long channel FET structures. The quality of the etching process obtained by N_{it} and mobility analysis is correlated with X-ray photoemission spectroscopy (XPS). Finally we present dynamic IV analysis (DIVA) of the fabricated devices.

2. Materials and devices

The heterostructure we used for the device processing and III-N etching calibration was grown on 4 in. n-type SiC substrate by metalorganic chemical vapor deposition and was composed of: 50 nm AlN nucleation layer, 1.2 μm Fe-doped GaN buffer, 820 nm GaN channel, 10 nm $Al_{0.25}Ga_{0.75}N$ barrier plus 6 nm of n^+ $Al_{0.25}Ga_{0.75}N$ $\sim 4 \times 10^{18}$ cm^{-3} and a 5 nm n^+ GaN $\sim 5 \times 10^{18}$ cm^{-3} capping layer. We produced four types of device (see Fig. 1): (1) standard MOS-HFET with no barrier recess, called MOS, (2) MOS-HFET with 7 nm deep partial recess of the barrier layer, called MOS 7, (3) MOS-HFET with 11 nm deep partial recess of the barrier layer, called MOS 11 and (4) True-MOS with full AlGaN barrier recess. In order to add consistency to the study, we processed the samples on the same epitaxial wafer which we diced in 1×1 cm^2 samples. The dies underwent the same processing sequence and the only difference was the gate recess depth. The inter device insulation was achieved by mesa definition. The alloyed ohmic contacts were composed of Ti/Al/Ni/Au. Contact resistance R_c and sheet resistance R_{sheet} as evaluated by transmission line measurements were 0.7 Ω/mm and 726 Ω/□ respectively. The devices were passivated with 100 nm of plasma enhanced chemical vapor deposited SiN_x. The gate trenches were defined by electron beam lithography on a Poly(methyl methacrylate) (PMMA) photoresist mask in order to obtain sub micrometer gate features. The etching was performed with an inductively coupled reactive ion etching (RIE) system in three steps: first the SiN_x passivation was opened with SF_6-based plasma; subsequently the GaN cap was etched through the same photoresist mask with a $SF_6/SiCl_4$ gas mixture in order to obtain a slanted profile in the SiN_x and GaN cap and to remove the native oxide layer which is often considered as the origin of the etch delay in III-N Cl-based dry-etching [19,20]; finally, the AlGaN layer was recessed with a Cl-based inductively coupled plasma (ICP). The final etching of the III-N material is of crucial importance for the device performance, thus we optimized the recipe in order to achieve low DC bias and minimize ion damage. A $SiCl_4$-based plasma was powered by 15 W RF and 215 W ICP. The DC bias measured during the etching process was ~10 V. The process calibration was performed on etching test structures trough a PMMA mask and by measuring the profile of the produced trench by atomic force microscopy (AFM) as shown in Fig. 2. We obtained a linear etching rate of 5 nm/min through both the $Al_{0.25}Ga_{0.75}N$ and GaN layers (see Fig. 2d). The gate trench profiles of the actual devices were also investigated by AFM. The recess depth into the barrier layer is considered to start from the "wings" of the slanted gate profile (see Fig. 2b). We experienced a constant increase in roughness σ_{rms} in the bottom of the gate trench with an increase of the etching time (see Table 1). The etched surface was cleaned in hot diluted HCl (10 min at 70 °C, H_2O:HCl → 2:1) in order to remove the native oxide and to prepare the surface for gate oxide deposition. As final step a Γ-shaped Ni/Au gate metallization was evaporated to close the gate stack. A scanning electron micrograph cross-section of the gate stack is shown in Fig. 2c, showing a slanted shape of the gate.

3. Results and discussion

3.1. XPS analysis

XPS performed on the surface of equivalent GaN and AlGaN reference samples after surface preparation revealed very low oxygen content close to the detection limit of the technique (1×10^{19} - atoms cm^{-3} or 0.1 atom%). Subsequently, 35 nm of ZrO_2 were deposited by ALD at 200 °C; tetrakis(diethylamido)zirconium(IV)

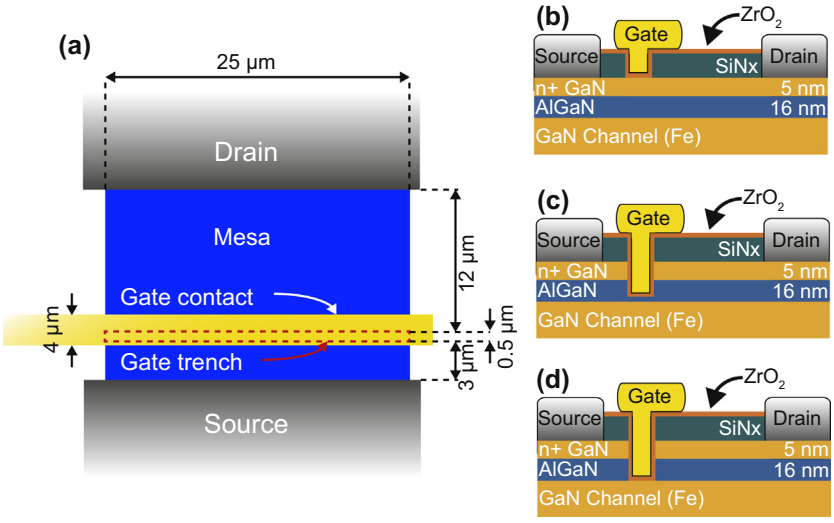

Fig. 1. (a) Schematic top view with dimensions of the devices presented in this contribution. Cross-section of the three device types, where (b) is the standard MOS-HFET, (c) is the partially recessed MOS-HFET and (d) is the fully recessed True-MOS.

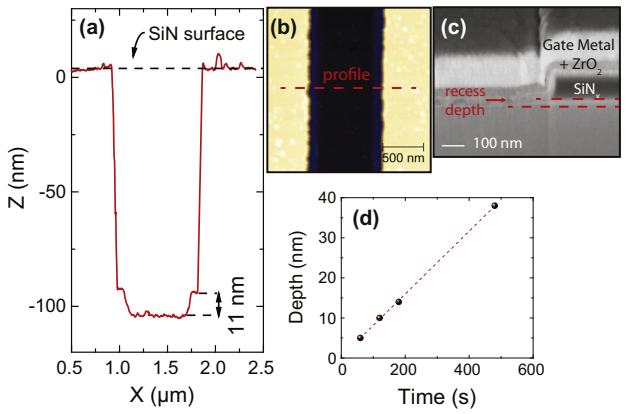

Fig. 2. (a) Extracted AFM profile of a gate trench in a MOS11 device, the recess depth in the AlGaN was extracted starting from the wings of the slanted gate profile. (b) AFM micrograph of a gate trench from a MOS11 device. (c) SEM micrograph of the gate stack cross-section showing recessed area. The cross-section was obtained by Focus Ion Beam cutting. (d) III-N etching calibration curve. The extracted etching rate is 5 nm/min.

$(ZrNEt_2)_4$ and H_2O were used as precursors. The impact of etching and oxide deposition were analyzed by XPS on dummy samples, which underwent the same etching procedure and HCl cleaning used for the gate trench opening. As shown in Fig. 3a and b, the Ga 3d core level recorded after etching/cleaning and before oxide deposition in the GaN and AlGaN states (20.2 eV and 20 eV) are in good agreement with the expected literature values for HCl treated surfaces [21,22]. The deposition of the ZrO_2 layer introduces a distinct GaO_x/ GaON state with a core-level shift of 0.7–0.8 eV observed in both ZrO_2/GaN and ZrO_2/AlGaN interfaces [21,22] which is not present in the just etched surfaces. The etching procedure does not alter the chemical properties of the initial surface within the sensitivity of the XPS technique. On the other hand, the ALD deposition induces the partial oxidation of the III-N layer which is considered as the main source of N_{int} [9].

3.2. DC IV characterization

The samples were characterized under direct current DC conditions with a Keithley 4200 semiconductor parameter analyzer. We extracted V_{th} from the transfer characteristics by extrapolation from the linear regime of the drain current I_d versus the gate voltage V_g (Fig. 4a). Since the MOS-HFET devices are affected by positive V_{th} drift under forward bias ΔV_{th} [6], we acquired the transfer IVs on virgin devices in a limited V_g range ($V_g \sim V_{th} - 1$ to $V_g = 2$ V) in order to limit ΔV_{th} to less than 100 mV. We report in Table 1 the mean V_{th} for each sample. The True-MOS devices exhibit a positive V_{th} of 1.25 V despite the thick ZrO_2 gate insulator. This confirms that the combination of full barrier recess and a high-k oxide is an effective approach for reducing the negative V_{th} shift. As expected upon decreasing the barrier thickness t_b, V_{th} shifts toward positive voltages [17]. We evaluated ΔV_{th} for all the samples from the forward/backward hysteresis of bidirectional

Table 1
Structural and main electrical properties of the studied devices. Legende/remarks: Recess depth is the depth of the etching in the GaN cap/AlGaN barrier, σ_{rms} is the root mean square roughness measured in the bottom of the gate trench after the dry etching, V_{th} is the threshold voltage, $\Delta V_{th,max}$ and ΔD_{it} are the maximum V_{th} shift observed for the defined stress condition and the density of active trap states related to $\Delta V_{th,max}$, $g_{m,max}$ is the maximum transconductance, $I_{d,max}$ the maximum output current for $V_{over} = 4$ V, N_{int} the extracted density of fixed positive charge at the ZrO_2/(Al)GaN interface and μ_{max} is the maximum measured mobility. The studied devices have the gate to drain spacing of 12 μm.

Recess depth (nm)	σ_{rms} (nm)	V_{th} (V)	$\Delta V_{th,max}$ (mV) @ $V_g = 4$ V	ΔD_{it} (cm^{-2}) @ $V_g = 4$ V	$g_{m,max}$ (S/mm)	$I_{d,max}$ (A/mm)	N_{int} (cm^{-2})	μ_{max} (cm^2/V s)
Non-recessed	1	−3.0	47	1.9×10^{11}	0.17	0.54	2.8×10^{13}	1618
7	1.3	−2.0	53	1.4×10^{11}	0.20	0.58	3.1×10^{13}	1446
11	1.7	−0.8	34	2.1×10^{11}	0.23	0.62	2.7×10^{13}	1333
Full recess (~22 nm)	2.4	+1.3	207	8.2×10^{11}	0.14	0.27	2.4×10^{13}	165

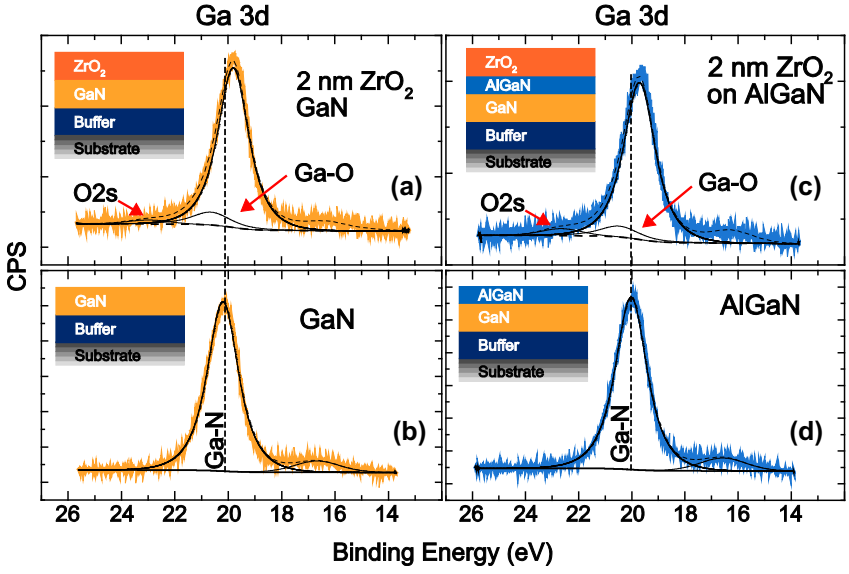

Fig. 3. XPS spectra of the Ga 3d core level. The spectra were acquired on etched and HCl-pretreated pure GaN, AlGaN (b and d) and on the respective interfaces with ZrO_2 (a and c). The ZrO_2 layers were deposited by ALD in the same condition used for MOS-HFETs and True-MOS. The thickness of the deposited oxide layer was ~2 nm. The samples on which the spectra were acquired are shown in the schematic drawings on the left side of each spectrum.

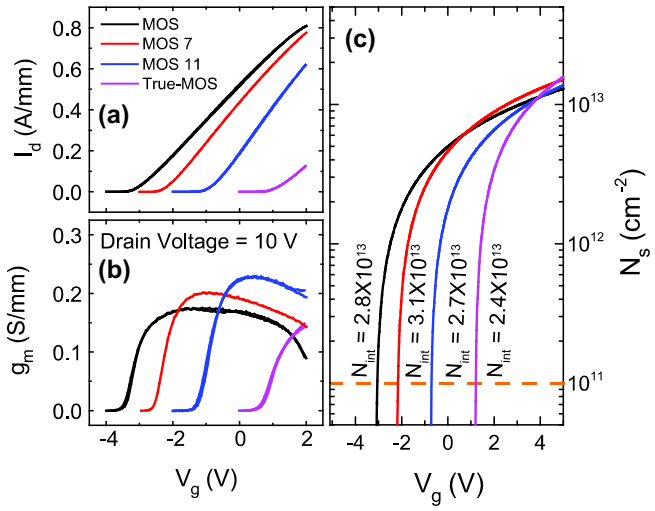

Fig. 4. (a) Measured bidirectional transfer characteristics used for the V_{th} extraction. (b) Transconductance extracted from (a); gate to drain spacing was 12 μm. (c) Simulated 2DEG concentration N_s, as function of V_g with indicated fitting values of N_{int} for each device. V_{th} is extracted for $N_s = 1 \times 10^{11}$.

transfers characteristics acquired at a constant V_g sweeping rate (0.2 V/s) and in the V_g interval from $V_{th} - 1$ to 4 V. The ΔV_{th} for the applied stress condition is $\ll$500 mV and the corresponding density ΔD_{it} of the active traps connected to the V_{th} drift, extracted according to Ref. [23], is below 10^{12} cm^{-2} (see Table 1). The transconductance g_m peak is inversely proportional to t_b, as expected (see Table 1 and Fig. 4b). The True-MOS exhibits a smaller g_m peak due to mobility degradation in the gate region (see below). The output characteristics are displayed for fixed gate overdrive voltage $V_{over} = V_g - V_{th}$ starting from $V_{over} = -1$ V to $V_{over} = 4$ V (Fig. 5). The maximum output currents for $V_{over} = 4$ V are listed in Table 1.

3.3. Dynamic IV characterization

The pulsed IV characterization has been performed in double pulse configuration with a DIVA system at controlled temperature of 17 °C. We compared R_{on} in various pulsed conditions with quiescent points in the pulse off-state ($V_g = 0$, $V_d = 0$) and ($V_g = V_{th} - 2$ V, $V_d = 30$, 50, 64 V). The V_g value in the pulse on-state was +3 V and the pulse durations 0.2 μs, 2 μs and 20 μs with respective off-state periods of 500 μs, 2 ms and 2 ms. The comparisons of pulse IV curves for the (0, 0) and ($V_{th} - 2$, 64) quiescent points and pulse duration of 0.2 μs for all the studied devices are shown in Fig. 6. The IV curves with the quiescent point ($V_g = 0$, $V_d = 0$) represent a "reference" condition. Such a pulsed IV was preferred to be taken as a reference rather than the DC IV curve, due to negligible self-heating effect in the former. The curves with the quiescent point ($V_{th} - 2$ V, 64 V) represent switching from an off-state condition in a power device to the on-state and both gate lag and drain-lag effects are involved. Here we call IV curves recorded with quiescent point $V_g = V_{th} - 2$ V and above mentioned V_d values as under "stress" condition. The device on-resistance related to the reference $R_{on,ref}$ and stress $R_{on,s}$ conditions were extracted from the linear region of the I_d vs V_d characteristics (Fig. 6). Fig. 7 summarizes the ratio $R_{on,s}/R_{on,ref}$ for all the tested devices in terms of contour plots where horizontal axis is drain stress quiescent bias and vertical axis the pulse duration. The maximum R_{on} increase after stress is comparable for the MOS, MOS 7 and MOS 11 and limited to 8% (see Fig. 7). The True-MOS is affected by more severe collapse, with a maximum R_{on} increase of 30%. The full recess of the barrier thus leads to a degradation of the dynamic properties of the True-MOS device. On the other hand we do not observe clear performance degradation in partially recessed devices compared to the standard MOS. The main degradation thus happens when the GaN/oxide interface is in direct contact with the electron channel and it is probably related to the interface state - induced enhancement of the electrical field at the gate edge [24]. Further improvement is thus needed in order to solve the collapse issue

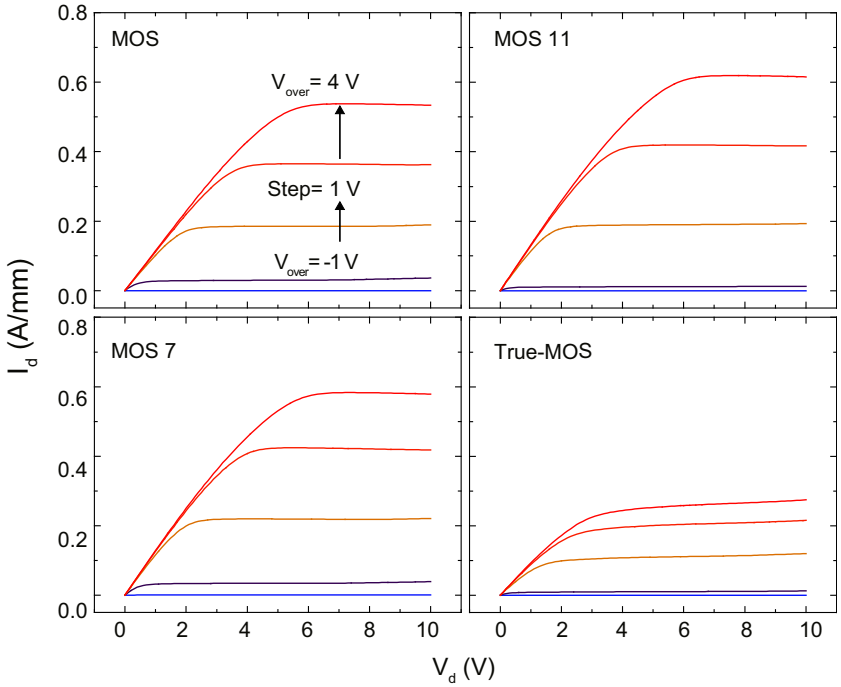

Fig. 5. Typical measured output characteristics of the four studied devices (gate to drain spacing was 12 μm). All the output IVs were acquired at V_{over} equal to −1, 0, 1, 2, 3 and 4 V. $I_{d,max}$ was extracted at $V_{over} = 4$ V. It has to be mentioned that $I_{d,max}$ extracted at high positive V_g might be affected by artifacts due to V_{th} instability. Thus the $I_{d,max}$ cannot be fully compared between the four samples.

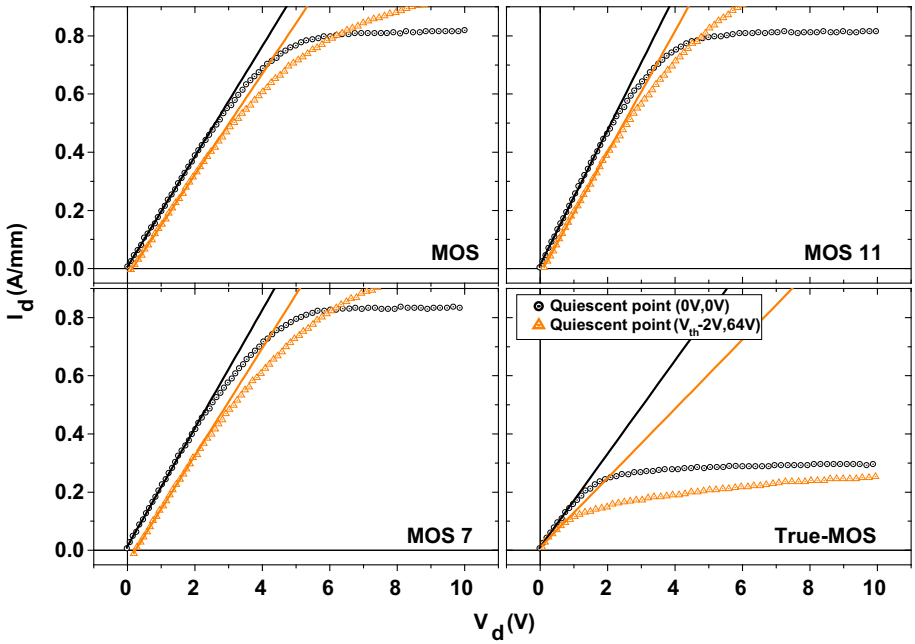

Fig. 6. Dynamic IV measurements of the analyzed devices with following quiescent points: (V_g = 0V, V_d = 0V) - "reference" and (V_g = V_{th} − 2 V, V_d = 64 V) - "stress" conditions. The pulse duration during on-state was 200 ns (V_g = 3 V). The R_{on} values were calculated from the linear part of the IVs (i.e. $V_d < V_g$). The slope lines related to extraction of $R_{on,s}$ and $R_{on,ref}$ are indicated. The gate to drain separation of the measured devices was L_{gd} = 4 μm.

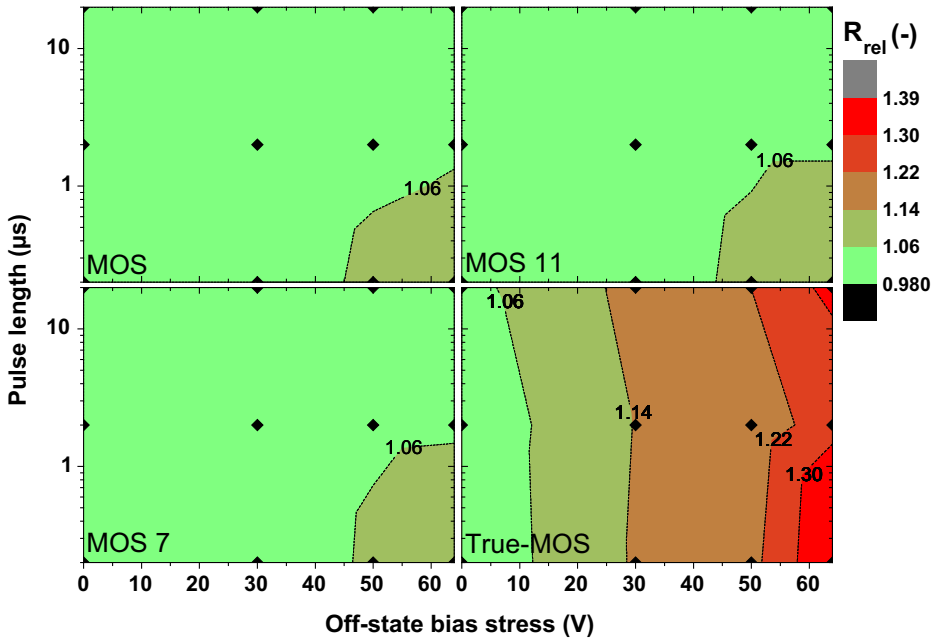

Fig. 7. 2D maps of the $R_{on,s}/R_{on,ref}$ ratio for all the device designs as a function of drain stress quiescent bias (horizontal axes) and pulse duration (vertical axes). The solid black symbols are measurement points. The gate to drain separation of the measured devices was L_{gd} = 4 μm.

in the True-MOS. Nevertheless a full treatment of the device dynamics is beyond the scope of this contribution and will be studied in deep in future works.

3.4. Fixed interface charge determination

The fixed charge density at the III-N/oxide interface N_{int} was extracted from the fitting of V_{th} values for each gate stack to a model using Gregory Snider's Schrödinger-Poisson simulator, see Table 1 [25]. The parameters for the simulations were taken from Refs. [26,27]. In Fig. 4c we present the simulated electron density in the 2DEG N_s as a function of V_g. We extracted an average N_{int} of 2.8 × 10^{13} cm^{-2} which is of the same order as the GaN polarization charge and is close to what was found in literature [8–11]. The True-MOS exhibits the lowest N_{int} (N_{int} = 2.4 × 10^{13}). Since we did not observe a direct correlation between N_{int} and barrier etching duration, we suggest that the etching is not inducing surface pinning and N_{int} solely depends on the polarization properties of the barrier/buffer layers [12]. In True-MOS technology, such a high concentration of positive interface charges in close contact with

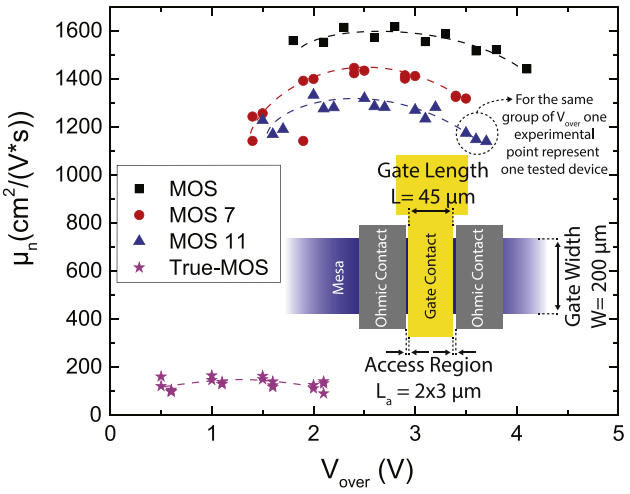

Fig. 8. Extracted electron mobility μ at various V_{over} in Fat-FET configuration at room temperature. The dashed lines are meant as a "guide for the eyes". Inset: schematic representation with physical dimension of the Fat-FET devices used for the mobility extractions.

the electron channel will increase Coulomb scattering due to ionized impurities (CSII) which is known to reduce electron mobility in III–V HFETs structures [6,17,28].

3.5. Mobility analysis

The electron mobility μ_n in the etched channel of MOS-HFETs, was extracted from devices with large gate length, $L = 45$ µm, called "Fat"-FET, which were processed together with the standard devices on the same die. The device layout and dimensions are shown in the insert of Fig. 8. In such a device, the total on resistance R_{on} given by: $R_{on} = R_c + R_{ac} + R_{ch}$ can be simplified to $R_{on} = R_{ch}$, where R_{ac} and R_{ch} is the access and channel resistance, respectively. Under such conditions we can extract the channel mobility by applying [29]:

$$\frac{dI_d}{dV_d} = \mu_n \frac{C_g * V_{over}}{L^2} \quad (1)$$

where C_g is the geometrical gate capacitance. Eq. (1) is valid in the linear region of the output characteristics, thus we applied a linear fit for the drain voltages in the range $V_d \ll V_{over}$ [29]. The extracted mobility *vs.* V_{over} is given in Fig. 8 (see also Table 1). The mobility drop observed in the MOS samples can be related to the increase of CSII due to N_{int} for which the relaxation time τ is inversely proportional to the barrier/spacing layer thickness [28]. The observed dependence of μ_n vs V_{over}, 2DEG concentration N_s, N_{int} and t_b has been reported by Hung et al. who observed that the dominating scattering mechanism for thin barrier devices and up to N_s - $\sim 5 \times 10^{12}$ cm^{-2} is the remote Coulomb scattering [6]. Thus, according to the numerical simulation shown in Fig. 4c, CSII is limiting the mobility up to $V_{over} = 3$ V. After this limit, other mechanisms like interface roughness and optical phonons start to have a non-negligible effect [6,28].

4. Conclusion

In conclusion, the etching recipe developed for the barrier recess shows a good linearity over a large range of etching times. Moreover after etching and oxide deposition we do not observe surface pinning of the III-N surface due to a strong increase of N_{int} and ΔD_{it}. Nevertheless, the channel mobility is strongly influenced by the presence of those interface states and their relative distance to the electron channel, as underlined by our experiment. The surface analysis performed by XPS suggests that a variety of chemical bonds can contribute to N_{int} and ΔD_{it}, and that they are formed mainly during the ALD process of ZrO_2. This represents further challenges for the implementation of oxides in III-N based normally-off technology and more effort needs to be spent in the direction of understanding the chemical properties of the III-N/dielectric interface during the dielectric deposition, as well as in finding better III-N surface passivation techniques for the subsequent ALD process and in finding more appropriate types of metal oxides. On the other hand this study suggests that a well-designed barrier etching does not necessarily introduce new interface states and recess-based technologies can be successfully implemented for the production of normally-off devices.

Acknowledgement

This work was performed in the frame of the European Project HiPoSwitch Grant agreement no. 287602.

References

[1] Uemoto Y, Hikita M, Ueno H, Matsuo H, Ishida H, Yanagihara M, et al. Gate injection transistor (GIT): a normally-off AlGaN/GaN power transistor using conductivity modulation. IEEE Trans Electron Devices 2007;54:3393–9.
[2] Hilt O, Knauer A, Brunner F, Bahat-Treidel E, Würfl J. Normally-off AlGaN/GaN HFET with p-type Ga gate and AlGaN buffer. In: 22nd International symposium on power semiconductor devices IC's (ISPSD), June. p. 347–50.
[3] Cai Y, Zhou Y, Chen KJ, Lau KM. High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment. IEEE Electron Device Lett 2005;26(7):435–7.
[4] Saito JW, Takada Y, Kuraguchi M, Tsuda K, Omura I. Recessed-gate structure approach toward normally off high-voltage AlGaN/GaN HEMT for power electronics applications. IEEE Trans Electron Devices 2006;53(2):356–62.
[5] Khan M, Hu X, Sumin G, Lunev A, Yang J, Gaska R, et al. AlGaN/GaN metal oxide semiconductor heterostructure field effect transistor. IEEE Electron Device Lett 2000;21:63–5.
[6] Hung T-H, Esposto M, Rajan S. Interfacial charge effects on electron transport in III-Nitride metal insulator semiconductor transistors. Appl Phys Lett 2011;99(16):162104.
[7] Lagger P, Ostermaier C, Pobegen G, Pogany D. Towards understanding the origin of threshold voltage instability of AlGaN/GaN MIS-HEMTs. In: IEEE international electron devices meeting (IEDM), 10–13 Dec. p. 13.1.1–4.
[8] Alexewicz A, Ostermaier C, Henkel C, Bethge O, Carlin J-F, Lugani L, et al. Explanation of threshold voltage scaling in enhancement-mode InAlN/AlN/GaN metal oxide semiconductor high electron mobility transistors on Si substrates. Thin Solid Films 2012;520(19):6230–2.
[9] Esposto M, Krishnamoorthy S, Nath DN, Bajaj S, Hung TH, Rajan S. Electrical properties of atomic layer deposited aluminum oxide on gallium nitride. Appl Phys Lett 2011;99(13):162104.
[10] Capriotti M, Alexewicz A, Fleury C, Gavagnin M, Bethge O, Visalli D, et al. Fixed interface charges between AlGaN barrier and gate stack composed of in situ grown SiN and Al_2O_3 in AlGaN/GaN high electron mobility transistors with normally off capability. Appl Phys Lett 2014;104(11):113502.
[11] Tapajna M, Kuzmik J. A comprehensive analytical model for threshold voltage calculation in GaN based metal-oxide-semiconductor high-electron mobility transistors. Appl Phys Lett 2012;100(11):113509.
[12] Ibbetson JP, Fini PT, Ness KD, DenBaars SP, Speck JS, Mishra UK, et al. Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors. Appl Phys Lett 2000;77(2):250–2.
[13] Wang Y, Wang M, Xie B, Wen CP, Wang J, Hao Y, et al. High-performance normally-off Al_2O_3/GaN MOSFET using a wet etching-based gate recess technique. IEEE Electron Device Lett 2013;34(11):1370–2.
[14] Xu Z, Wang J, Liu J, Jin C, Cai Y, Yang Z, et al. Demonstration of normally-off recess-gated AlGaN/GaN MOSFET using GaN cap layer as recess mask. IEEE Electron Device Lett 2014;35(12):1197–9.
[15] Xu Z, Wang J, Liu Y, Cai J, Liu J, Wang M, et al. Fabrication of Normally Off AlGaN/GaN MOSFET Using a Self-Terminating Gate Recess Etching Technique. IEEE Electron Device Lett 2013;34(7):855–7.
[16] Xu Z, Wang J, Cai Y, Liu J, Jin C, Yang Z, et al. Demonstration of normally-off recess-gated AlGaN/GaN MOSFET using GaN cap layer as recess mask. IEEE Electron Device Lett 2014;35(12):1197–9.
[17] Choi H-S. Mobility degradation effect to Hooge's constant in recessed-gate Al_2O_3/AlGaN/GaN MIS power transistors. IEEE Electron Device Lett 2014;35(6):624–6.
[18] Capriotti M, Bahat-Treidel E, Fleury C, Bethge O, Rigato M, Lancaster SLC, et al. E-mode AlGaN/GaN True-MOS, with high-k ZrO_2 gate insulator. In: 45th European solid state device research conference (ESSDERC), 14–18 Sept. p. 60–3.

[19] Bahat-Treidel E, Hilt O, Zhytnytska R, Wentzel A, Meliani C, Würfl J, et al. Fast-switching GaN-based lateral power Schottky barrier diodes with low onset voltage and strong reverse blocking. IEEE Electron Device Lett 2012;33(3):357–9.
[20] Buttari D, Chini A, Palacios T, Coffie R, Shen L, Xing H, et al. Origin of etch delay time in Cl_2 dry etching of AlGaN/GaN structures. Appl Phys Lett 2003;83(23):4779–81.
[21] Ye G, Wang H, Arulkumaran S, Ng GI, Li Y, Liu ZH, et al. Band alignment between GaN and ZrO_2 formed by atomic layer deposition. Appl Phys Lett 2014;105(2):022106.
[22] Ye G, Wang H, Ng SLG, Ji R, Arulkumaran S, Ng GI, et al. Impact of post-deposition annealing on interfacial chemical bonding states between AlGaN and ZrO_2 grown by atomic layer deposition. Appl Phys Lett 2015;106(9):091603.
[23] Lagger P, Steinschifter P, Reiner M, Stadtmuller M, Denifl G, Naumann A, et al. Role of the dielectric for the charging dynamics of the dielectric/barrier interface in AlGaN/GaN based metal-insulator-semiconductor structures under forward gate bias stress. Appl Phys Lett 2014;105(3):033512.
[24] Bahat-Treidel E, Brunner F, Hilt O, Cho E, Wurfl J, Trankle G. AlGaN/GaN/GaN: C back-barrier HFETs with breakdown voltage of over 1 kV and low $R_{on\times A}$. IEEE Trans Electron Devices 2010;57(11):3050–8.
[25] Snider G. Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556. http://www3.nd.edu/gsnider/.
[26] Robertson J, Falabretti B. Band offsets of high K gate oxides on III–V semiconductors. J Appl Phys 2006;100(1):014111.
[27] Ambacher O, Majewski J, Miskys C, Link A, Hermann M, Eickhoff M, et al. J Phys: Condens Matter 2002;14:3399.
[28] Antoszewski J, Gracey M, Dell JM, Faraone L, Fisher TA, Parish G, et al. Scattering mechanisms limiting two-dimensional electron gas mobility in $Al_{0.25}Ga_{0.75}N$/GaN modulation-doped field-effect transistors. J Appl Phys 2000;87(8):3900–4.
[29] Sze SM, Ng KK. Physics of semiconductor devices. 3rd ed. Wiley; 2006.